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An Efficient High Voltage Level Shifter using Coupling Capacitor for a High Side Buck Converter

Kwang-Su Seong†

Abstract – We propose an efficient high voltage level shifter for a high side Buck converter driving a light-emitting diode (LED) lamp. The proposed circuit is comprised of a low voltage pulse width modulation (PWM) signal driver, a coupling capacitor, a resistor, and a diode. The proposed method uses a property of a PWM signal. The property is that the signal repeatedly transits between a low and high level at a certain frequency. A low voltage PWM signal is boosted to a high voltage PWM signal through a coupling capacitor using the property of the PWM signal, and the boosted high voltage PWM signal drives a p-channel metal oxide semiconductor (PMOS) transistor on the high side Buck converter. Experimental results show that the proposed level shifter boosts a low voltage (0 to 20 V) PWM signal at 125 kHz to a high voltage (370 to 380 V) PWM signal with a duty ratio of up to 0.9941.

Keywords: Level shifter, High side buck converter, Coupling capacitor, DC distribution, LED lighting

1. Introduction

Direct current (DC) power distribution is an effective solution considering the properties of DC-preferred loads. Many household appliances and office machines such as digital TVs, computers, facsimiles, copy machines, and solid-state lighting are DC-preferred loads. DC distribution has no alternating current (AC) losses and no reactive power issues [1, 2]. DC distribution also helps eliminate the power factor correction (PFC) stages in the appliances and machines [2].

Energy management in smart buildings with DC distribution that supplies power to DC electrical appliances such as lighting has recently attracted increasing interest from the research community [3]. Integrated lighting controls for demand-side energy management in a building can significantly improve energy efficiency, and enhance occupant comfort and satisfaction with the built environment [3]. In [4], a DC-level dimmer supplies variable DC voltage to ballasts powering light emitting diode (LED) lamps, as shown in Fig. 1(a). The DC-level dimmer sets its output voltage according to a dimming level, and ballasts adjust the brightness of their LED lamps according to the level of the DC voltage. The simplicity of this configuration, which requires no communication lines between the dimmer and ballasts, is a strong point. But this system is not appropriate for implementing a smart lighting system due to the lack of a bidirectional communication channel between the dimmer and the ballasts. In [3, 5], wireless or wired communication is applied to an

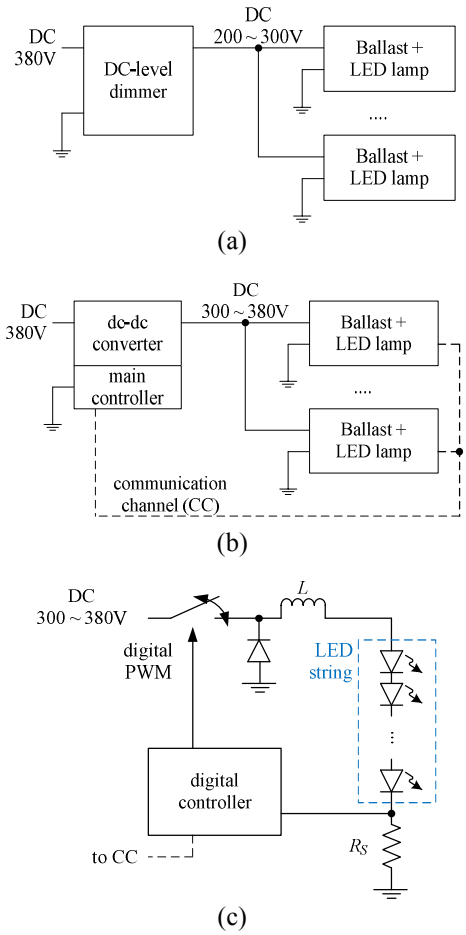

Fig. 1. (a) DC-level dimming system [4], (b) smart lighting system with variable DC voltage and dedicated communication channel, and (c) high side Buck converter.

† Corresponding Author: Dept. of Electronic Engineering, Yeungnam University, Korea. (kssung@ynu.ac.kr)
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intelligent smart lighting system. Fig. 1(b) shows a communication channel between the main controller and ballasts. The main controller can control the dimming level of the lamps through a communication channel, and supply optimal DC voltage to the ballasts using the information collected from the ballasts. The system shown in Fig. 1(b) was used in this study.

A conventional 20 W LED tube that is retrofittable for a fluorescent tube uses 132 LEDs when 0.2 W LEDs are used. In the LED tube, 12 LED strings are connected in parallel, with 11 LEDs connected in series in an LED string [6, 7]. There are deviations of the currents among the 12 LED strings connected in parallel, which gives deviations of the light intensities of the strings [7]. In this study, we adopted a high side Buck converter as shown in Fig. 1(c). The converter drives an LED string where 100 LEDs are connected in series. In this case, the turn-on voltage of the LED string is about 300 V. As the LEDs are connected in series, the current flowing into each LED is the same, and the intensity of each LED is the same.

There are two options to implement the switch in Fig. 1(c). One is to use an NMOS transistor, and the other is to use a PMOS transistor. An NMOS transistor is appropriate for a high-power and high-efficiency Buck converter because the on-resistance of the transistor is lower than that of a PMOS transistor. However, the driving circuit for the NMOS transistor is more complex than that for the PMOS transistor because the source voltage of the NMOS transistor is not fixed [8, 9]. The on-resistance of a PMOS transistor is relatively high compared with that of an NMOS transistor, but the driving circuit for the PMOS transistor is relatively simple compared with that for the NMOS transistor because the source of the PMOS transistor is connected to a constant voltage. Thus, a PMOS transistor is appropriate for a low-power and low-cost Buck converter, especially when the output current of the converter is low. In this study, we chose the PMOS transistor because the Buck converter drives a 20 W LED lamp, and the output current of the converter is less than 100 mA.

In a Buck converter, the current flowing into an LED string can be controlled to reach a target by increasing the duty ratio of a pulse width modulation (PWM) control signal while appropriately decreasing the input voltage of the converter if the input voltage is controllable. In this case, the efficiency of the Buck converter can be increased. The high side Buck converter shown in Fig. 1(c) can exactly measure and control the current flowing into an LED string even if the input voltage is widely changed [10]. However, this structure requires a high side switch. Therefore, we must convert a low voltage PWM signal into a high voltage PWM signal. Many high voltage level shifter circuits have been proposed. The previous works were usually implemented using high voltage semi-conductor process technology. The manufacturing cost of a level shifter usually increases as the target voltage of the level shifter is increased. Thus, the previous works are not appropriate for application in a low cost ballast circuit driving an LED sting when the target voltage of the level shifter is high. The previous works are described in Section 2.

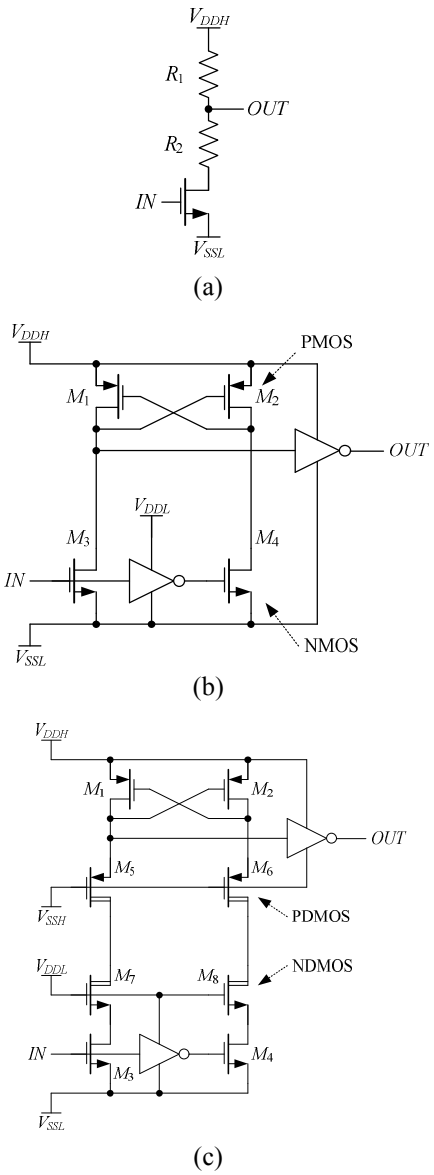
We propose an efficient high voltage level shifter circuit for a high side Buck converter that drives an LED string. The proposed method uses the property of a PWM signal that repeatedly transits between a low and high level at a certain frequency. The circuit boosts a low voltage PWM signal to a high voltage PWM signal through a coupling capacitor using the property of the PWM signal. The high voltage PWM signal drives a p-channel metal oxide semiconductor (PMOS) transistor on the high side Buck converter. Although the proposed circuit consists of a low voltage PWM signal driver, a coupling capacitor, a resistor, and a diode, the circuit can provide enough high voltage PWM signal to drive the PMOS transistor. Experimental results show that the proposed level shifter was successfully applied to the high side Buck converter with an input voltage of 380 V, and boosts the low voltage (0 to 20 V) PWM signal at a frequency of 125 kHz to a high voltage (370 to 380 V) PWM signal with a duty ratio of up to 0.9941.

The remainder of this paper is organized as follows. Section 2 describes previous works. Section 3 explains the proposed circuit and its behavior. Section 4 describes our experimental results. Our conclusions are given in Section 5.

2. Previous Works

Fig. 2(a) shows a simple level shifter whose output is determined by the ratio of the two resistors and V_{DDH}. The level shifter consumes static power when the input is high level, and the output driving capability is low due to the two resistors. This type of level shifter is usually used in low cost and low V_{DDH} applications.

Fig. 2(b) shows a latch-type complementary MOS (CMOS) level shifter. The circuit has a cross-coupled PMOS latch on the top, and converts a low voltage input signal to a high voltage output signal by driving two n-channel MOS (NMOS) transistors on the bottom [11]. The level shifter has no static power consumption and a high driving capability, and can be integrated into a micro-controller unit (MCU) and other controllers based on CMOS semiconductor process technology. In a CMOS process technology, the maximum allowed source to gate voltage and source to drain voltage of PMOS are less than two times of V_{DDL}, respectively. This level shifter circuit is limited in its ability to increase voltage V_{DDH} because the voltage between the source and the gate of the PMOS can reach to V_{DDH}, and the voltage between the source and the drain of the PMOS can also reach to V_{DDH}. Improved versions of this type of level shifter have been reported, wherein V_{DDH} is about two to five times higher than V_{DDL}



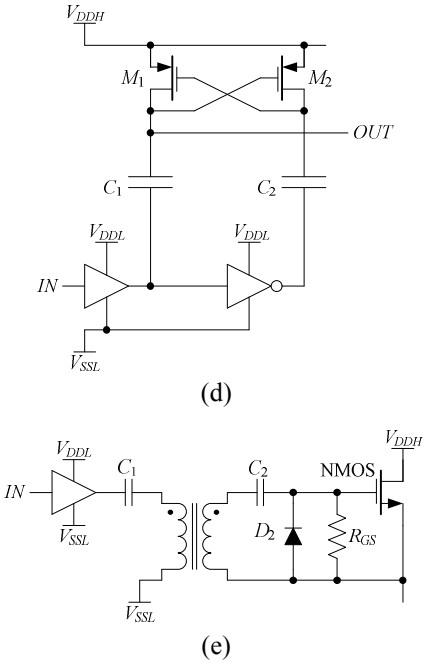


Fig. 2. (a) Simple level shifter; (b) latch-type CMOS level shifter; (c) DMOS cascade high voltage level shifter; (d) high voltage level shifter using coupling capacitors, and (e) pulse transformer coupled gate driver with DC restore circuit.

[12, 13].

Fig. 2(c) shows a high voltage version of Fig. 2(b) that uses a drain-extended MOS (DMOS). The structure of a DMOS is similar to that of a MOS except the drain of the DMOS is extended. The maximum allowed voltage between the gate and the source of the DMOS is the same as that of a conventional MOS, but high voltage can be applied across the drain and the source of the DMOS. In Fig. 2(c), two n-channel DMOS (NDMOS) devices protect NMOS M_3 and M_4. In the same way, two p-channel DMOS (PDMOS) devices protect PMOS M_1 and M_2, thus M_1 and M_2 are placed between V_{SSH} and V_{DDH} [11, 14]. Many improved versions of the level shifter shown in Fig. 2(b) have been reported [11, 15, 16]. However, the manufacturing cost of a level shifter using DMOS semiconductor process technology is higher than that of the level shifter using CMOS semiconductor process technology. Furthermore, the level shifter based on DMOS technology is not appropriate for integration into an MCU and other controllers based on CMOS technology. Thus, this type of level shifter is used as a stand-alone off-chip device.

Fig. 2(d) shows a level shifter circuit using coupling capacitors, wherein the initialization circuit for the drain nodes of the two PMOS transistors is omitted. The level shifter is an appropriate way to increase V_{DDH}, because most of the value of V_{DDH} exists across the coupling capacitors. However, the level shifter requires an initialization circuit and a cross-coupled PMOS latch [8, 17]. Thus, the whole circuit of the level shifter in [8] was implemented on a single chip including two power switches (not shown in Fig. 2(d)), the initialization circuit, the cross-coupled PMOS transistors, and the coupling capacitors (several pF). In many semiconductor processes, high voltage capacitors can be constructed only with normal routing metals, requiring large silicon area to obtain reasonable capacitance values and increasing the manufacturing cost [11].

Fig. 2(e) shows a pulse transformer coupled gate driver with DC restore circuit. The advantages of the method are that it does not require isolated power supplies to drive the secondary-side NMOS transistor and maintains electrical isolation between the control and gate drive electronics. However, a problem can occur when a large transient drive current flowing in the inductive coils causes ringing. This can switch the gate on and off when not intended and damage the NMOS transistor. The transformer can deliver only AC signals with maintaining a volt-second balance, thus the transformer coupled gate driver needs a DC restore

circuit to increase duty cycle capability. Fig. 2(e) shows a commonly used DC restore circuit that consists of C_2 and D_2. The effective duty cycle range of the transformer coupled gate driver with the circuit is from 5 to 95% [18].

3. Proposed Level Shifter

Fig. 3 shows the proposed level shifter circuit that consists of a low voltage pulse width modulation (PWM) signal driver, a coupling capacitor C_c, a resistor R_1, and a diode D_1. Capacitance C_g is the equivalent gate capacitance of the PMOS transistor. During the power-on period, the gate voltage of the PMOS is charged to V_{DDH} through resistor R_1. If the voltage of the PWM control signal $v_c(t)$ changes from V_{DDL} to zero, the gate voltage changes from V_{DDH} to $V_{DDH}-(C_c/C_A)V_{DDL}$ and is then continuously increased due to the current flowing through R_1, where $C_A = C_c + C_g$. Then, if the voltage of $v_c(t)$ changes from zero to V_{DDL}, the gate voltage changes to $V_{DDH} + V_D$ and then slightly decreases toward V_{DDH} due to the voltage difference across resistor R_1, where V_D is the forward bias voltage of the diode.

Fig. 4(a) shows the timing of the control signal $v_c(t)$, whose duration is T and duty ratio is T_1 / T. When the control signal shown in Fig. 4(a) is applied to the proposed circuit in Fig. 3, the voltage of the gate and the voltage difference between the gate and the source of the PMOS are as shown in Figs. 4(b) and (c), respectively. As $0 \le T_1 < T$, the maximum value of T_1 goes toward T. Eq. (1) can be obtained by applying Kirchhoff's current law (KCL) to the gate node, where v_G is the gate voltage of the PMOS.

$$C_c \frac{d\left(v_G(t)-v_c(t)\right)}{dt} + C_g \frac{dv_G(t)}{dt} = \frac{V_{DDH}-v_G(t)}{R_1} \tag{1}$$

When the control signal $v_c(t)$ transits from V_{DDL} to zero at $t = 0$ as shown in Fig. 4(a) (i.e., $v_c(t) = V_{DDL}\,u(-t)$), the gate voltage at $t = 0^+$ becomes $v_G(t=0^+) = V_{DDH} + V_D - \left(C_c / C_A\right)V_{DDL}$ and the solution of Eq. (1) is given by Eq. (2) for $0 \le t < T_1$, where $\tau = R_1 C_A$ and $C_A = C_c + C_g$.

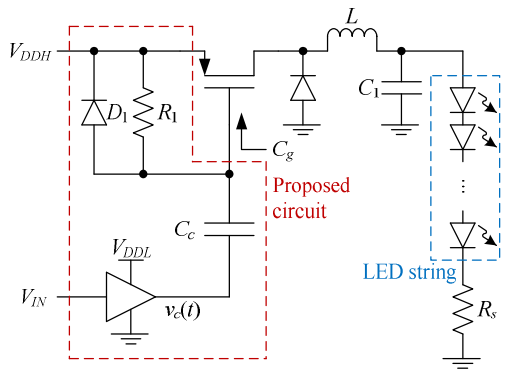


Fig. 3. Proposed level shifter circuit.

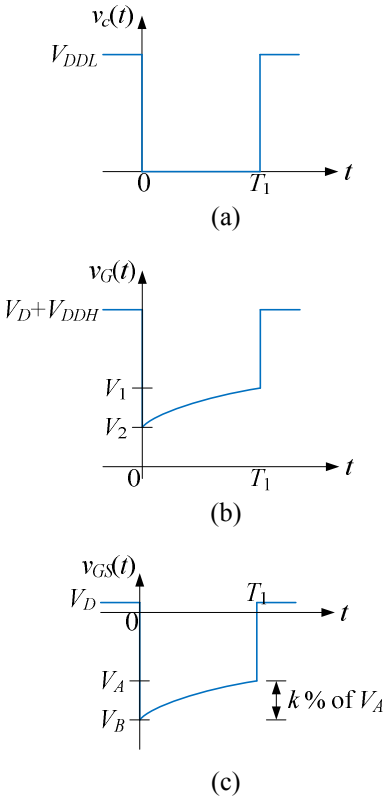


Fig. 4. (a) Low voltage PWM control signal $v_c(t)$, (b) the gate voltage of the PMOS, and (c) the voltage difference between the gate and the source of the PMOS, where k is defined as the deviation ratio.

$$v_G(t) = V_{DDH} + \left(V_D - (C_c / C_A)V_{DDL}\right)e^{-t/\tau} \tag{2}$$

Thus, the voltages of V_1, V_2, V_A, and V_B in Fig. 4 are expressed as Eqs. (3), (4), (5), and (6), respectively:

$$V_1 = V_{DDH} + \left(V_D - (C_c / C_A)V_{DDL}\right)e^{-T_1/\tau} \tag{3}$$

$$V_2 = V_{DDH} + V_D - (C_c / C_A)V_{DDL} \tag{4}$$

$$V_A = \left(V_D - (C_c / C_A)V_{DDL}\right)e^{-T_1/\tau} \tag{5}$$

$$V_B = V_D - (C_c / C_A)V_{DDL} \tag{6}$$

We define the deviation ratio k of the gate voltage as Eq. (7), which is depicted in Fig. 4(c). By applying Eqs. (5) and (6) to Eq. (7), we obtain Eqs. (8) and (9). Eq. (9) shows that the time constant of the proposed circuit depends on the deviation ratio k.

$$k = \left(V_B - V_A\right)/V_A \tag{7}$$

$$e^{-T_1/\tau} = \left(1+k\right)^{-1} \tag{8}$$

$$\tau = T_1 / \ln\left(1+k\right) \tag{9}$$

In a PMOS transistor, V_T means the threshold voltage at which the channel of the transistor starts to be created. $V_{GS(TYP)}$ means a typical turn-on voltage of the transistor, at

which the transistor is in a sufficiently turn-on state. The manufacturer of the transistor usually uses $V_{GS(TYP)}$ to represent the performance of the transistor on the data sheet. $V_{GS(MIN)}$ is the minimum allowed voltage of V_{GS} that can be applied to the transistor. The relation among the three voltages is given by $V_{GS(MIN)} < V_{GS(TYP)} < V_T < 0$. In Eq. (5), if we set $V_A = V_{GS(TYP)}$, then we can obtain Eq. (10):

$$V_{GS(TYP)} = \left(V_D - (C_c / C_A)V_{DDL}\right)e^{-T_1/\tau} \tag{10}$$

By using Eqs. (8) and (10), we can obtain the capacitance of C_c as shown by Eq. (11). We can also obtain the resistance of R_1 as given by Eq. (12) by using Eqs. (9) and (11). Thus,

$$C_c = \frac{V_D - (1+k)V_{GS(TYP)}}{V_{DDL} - V_D + (1+k)V_{GS(TYP)}}C_g \tag{11}$$

$$R_1 = \frac{1}{\ln(1+k)}\left(\frac{V_{DDL} - V_D + (1+k)V_{GS(TYP)}}{V_{DDL}}\right)\frac{T_1}{C_g} \tag{12}$$

Now, we calculate the power consumption of R_1 and D_1. From Eqs. (2) and (6), the voltage difference between the source and the gate of the PMOS transistor is expressed as $v_{SG}(t) = -V_B e^{-t/\tau}$ in $0 \le t < T_1$. Thus, the average power consumption P_{R1} of resistor R_1 is expressed as Eq. (13).

$$\begin{aligned} P_{R1} &= \frac{1}{T}\int_0^{T_1}\frac{v_{SG}^2(t)}{R_1}dt = \frac{V_B^2\tau}{2TR_1}\left(1-e^{-2T_1/\tau}\right) \\ &= \frac{1}{2T}C_A V_B^2\left(1-e^{-2T_1/\tau}\right) < \frac{1}{2T}C_A V_B^2\left(1-e^{-2T/\tau}\right) \\ &< \frac{1}{2T}C_A V_B^2\frac{2T}{\tau} = \frac{V_B^2}{R_1} \end{aligned} \tag{13}$$

The diode D_1 can be approximated as a piecewise-linear model, as shown in Fig. 5. As the diode is turned on during $T_1 \le t < T$, the average power consumption P_{D1} of the diode is expressed as Eq. (14).

$$\begin{aligned} P_{D1} &= \frac{1}{T}\int_{T_1}^{T}\left(V_D i_d(t) + r_d i_d^2(t)\right)dt \\ &= \frac{1}{T}\int_0^{T-T_1}\left(V_D i_d(t+T_1) + r_d i_d^2(t+T_1)\right)dt \end{aligned} \tag{14}$$

By applying KCL to the gate node, we can express the gate node voltage as Eq. (15), where $\tau_d = C_A r_d$. We assume that the current flowing through R_1 is negligible because the voltage difference across the resistor is about V_D when the diode is turned on.

$$v_G(t+T_1) = V_D + V_{DDH} + \left(V_A - V_B\right)e^{-t/\tau_d} \tag{15}$$

Thus, the diode current $i_d(t + T_1)$ is expressed as Eq. (16).

$$i_d(t+T_1) = \frac{\left(V_A - V_B\right)}{r_d}e^{-t/\tau_d} \tag{16}$$

The voltage difference $V_A - V_B$ is due to the current flowing through R_1 during $0 \le t < T_1$, and is expressed as Eq. (17).

$$\begin{aligned} V_A - V_B &= \frac{1}{C_A}\int_0^{T_1} i_{R1}(t)dt < \frac{1}{C_A}\int_0^{T_1} -\frac{V_B}{R_1}dt \\ &= -\frac{V_B}{\tau}T_1 < -V_B\frac{T}{\tau} \end{aligned} \tag{17}$$

Now, we can solve Eq. (14) by applying Eqs. (16) and (17) to Eq. (14). The solution is expressed as Eq. (18).

$$\begin{aligned} P_{D1} &= \frac{1}{T}C_A V_D\left(V_A - V_B\right)\left(1-e^{-(T-T_1)/\tau_d}\right) \\ &\quad + \frac{1}{2T}C_A\left(V_A - V_B\right)^2\left(1-e^{-2(T-T_1)/\tau_d}\right) \\ &< \frac{1}{T}C_A V_D\left(V_A - V_B\right) + \frac{1}{2T}C_A\left(V_A - V_B\right)^2 \\ &< -\frac{V_D V_B}{R_1} + \frac{V_B^2}{2R_1}\frac{T}{\tau} \end{aligned} \tag{18}$$

The PWM signal driver also consumes power because it drives a capacitive load C_L, where $C_L \approx C_c C_g / (C_c + C_g)$ if R_1 is large enough for its effect on the circuit to be negligible. If $\left(V_A - V_B\right)/\left(-V_B\right) << 1$ is satisfied in Fig. 4(c), we can say the resistor gives little effect on the circuit. Because $(V_A - V_B)$ is expressed as Eq. (17), $\left(V_A - V_B\right)/\left(-V_B\right) < T/\tau$ is satisfied, and we can use $T / \tau << 1$ instead of $\left(V_A - V_B\right)/\left(-V_B\right) << 1$. Thus the power consumption of the driver is expressed as Eq. (19) if $T / \tau << 1$. On the other hand, C_L is expressed as $C_L \approx C_c$ if $T / \tau >> 1$.

$$P_{PWM} = C_L V_{DDL}^2 f \approx \frac{C_c C_g}{C_A}V_{DDL}^2 f \tag{19}$$

During the power-on period, the PMOS transistor should

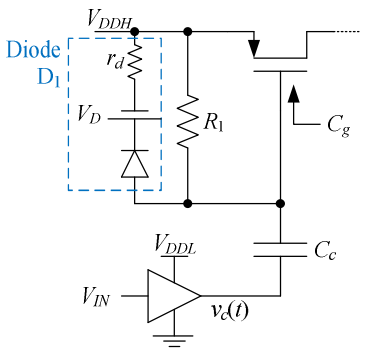


Fig. 5. Approximation of diode D_1 with piecewise-linear model.

be turned off. To satisfy this condition, the voltage between the gate and the source of the PMOS transistor should be larger than V_T; i.e., $v_{GS}(t) > V_T$. In Fig. 1(b), if the output voltage of the DC-DC converter is programmable, the converter can also control the rise time of the output voltage. In this case, we can turn the PMOS off during the power-on period. Now, we will explain a necessary condition to turn off the PMOS during the power-on period if the output voltage of the DC-DC converter is not programmable.

Fig. 6 shows the timing diagram of supply voltage $v_{DDH}(t)$ during the power-on period where V_{DDH} is the steady-state value of the supply voltage and t_r is the rising time of the supply voltage. In this analysis, we assumed that the voltage of the control signal $v_c(t)$ is zero during the power-on period. By applying KCL to the gate node of the PMOS, we obtain Eq. (20):

$$\frac{dv_G(t)}{dt}+\frac{v_G(t)}{\tau}=\frac{v_{DDH}(t)}{\tau} \tag{20}$$

In the power-on period (i.e., $t \le t_r$), the supply voltage is expressed as $v_{DDH}(t)=(V_{DDH}/t_r)t$. Thus, the voltage of the gate node during the power-on period is expressed as Eq. (21) by solving Eq. (20):

$$\begin{aligned} v_G(t) &= \frac{\tau}{t_r}V_{DDH}\left(e^{-t/\tau}-1\right)+\frac{V_{DDH}}{t_r}t \\ &= \frac{\tau}{t_r}V_{DDH}\left(e^{-t/\tau}-1\right)+v_{DDH}(t) \end{aligned} \tag{21}$$

Thus, $v_{GS}(t)$ is expressed as Eq. (22) using Eq. (21):

$$v_{GS}(t)=\frac{\tau}{t_r}V_{DDH}\left(e^{-t/\tau}-1\right) \tag{22}$$

Eq. (22) has minimum value when $t = t_r$ for $t \le t_r$. Thus, $v_{GS}(t_r)$ should be larger than V_T; i.e., Eq. (23) should be satisfied in order to turn off the PMOS transistor during the power-on period.

$$\frac{\tau}{t_r}V_{DDH}\left(e^{-t_r/\tau}-1\right)>V_T \tag{23}$$

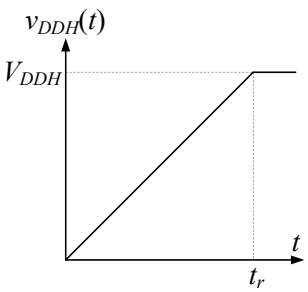


Fig. 6. Supply voltage during the power-on period.

We can obtain the approximate rise time t_r that satisfies Eq. (23). If t_r/τ has large value, $e^{-t_r/\tau}$ becomes very small compared to 1, and Eq. (23) is arranged as follows:

$$t_r > -\frac{V_{DDH}}{V_T}\tau \tag{24}$$

Eq. (24) can be arranged as $\frac{t_r}{\tau} > -\frac{V_{DDH}}{V_T}$, and $\frac{t_r}{\tau} > 126.7$ if V_{DDH}=380 V and V_T=–3 V. Thus, the assumption that t_r/τ has a large value and $e^{-t_r/\tau}$ becomes significantly small compared to 1 is valid if V_{DDH} is relatively high compared to $-V_T$. Eq. (24) is arranged as Eq. (25) using Eq. (9). During the power-on period, Eq. (25) should be satisfied in order to turn off the PMOS transistor:

$$t_r > -\frac{V_{DDH}}{V_T}\frac{T_1}{\ln(1+k)} \tag{25}$$

In the analysis of the proposed circuit, we used parameter T_1. The range of T_1 is $0 \le T_1 < T$, and the maximum value of T_1 goes toward T. Thus T is used instead of T_1 when designing the proposed circuit, i.e., T is used instead of T_1 when determining the values of resistor R_1 and the coupling capacitor C_c. If the frequency of the PWM signal is 125 kHz (T = 8 μs), V_{DDH} is 380 V, V_T is –3 V, C_g is 0.55 nF, k is 10%, $V_{GS(TYP)}$ is –10 V, V_{DDL} is 20 V, and V_D is 0.7 V, then we can obtain C_c = 0.78 nF and R_1 = 63.3 KΩ by using Eqs. (11) and (12). From Eq. (13) and (18), the power consumption of the resistor R_1 and that of the diode D_1 are expressed as P_{R1} < 1.92 mW and P_{D1} < 0.21 mW, respectively. The time constant (τ = 84.2 us) is about 10 times larger than the duration (T = 8 us), thus we can use Eq. (19) to calculate the power consumption of the PWM signal driver as $P_{PWM} \approx$ 16.1 mW. P_{PWM} is a major part of the total power consumption of the proposed circuit, and the sum of P_{R1} and P_{D1} represents only about 12 % of the total power consumption. The rise time of the high voltage $v_{DDH}(t)$ during the power-on period should be greater than 10.6 ms based on Eq. (25). Fig. 7 shows the

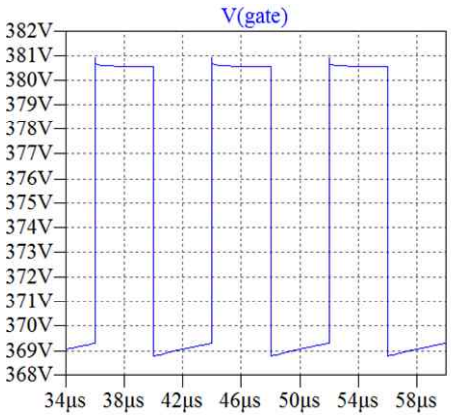


Fig. 7. Simulation results of the voltage of the gate node.

simulation results of the proposed circuit using the parameters selected above when the duty ratio is 0.5. The wave form of the voltage of the gate node is quite similar to the wave form shown in Fig. 4(b).

Until now, we assumed that a resistor and capacitor have fixed values, but the values vary with the temperature and tolerance. We set the error rates of the resistance and capacitance as p and q, respectively. When the resistance R_1 and capacitance C_c are respectively changed to $R_1(1+p)$ and $C_c(1+q)$, the deviation ratio k is also changed according to Eq. (26) that is derived from Eq. (9), where $\tau' = (1+p)R_1\left(C_g + (1+q)C_c\right) = (1+p)\left(\tau + qR_1C_c\right)$.

$$k = e^{T/\tau'} - 1 \tag{26}$$

Table 1 shows the variation of k when p and q are within ±20% using T = 8 μs, R_1 = 63.3 KΩ, C_g = 0.55 nF, and C_c = 0.78 nF. The values of the parameters were used in the previous design example. When there are no errors in the resistance and capacitance, (i.e., $p = q = 0\%$), the deviation ratio k is 10% that is the same as the value set in the previous example. In this case, $V_{GS}(t) < V_{GS(TYP)}$ is satisfied in $0 \le t < T$. When k is less than 10%, (i.e., $\tau' > \tau$), the voltage of the gate node is slowly charged compared with the case of k =10%. In this case, $V_{GS}(t) < V_{GS(TYP)}$ is also satisfied in $0 \le t < T$. However, the voltage of the gate node is rapidly charged when k > 10% compared with k = 10%, because $\tau' < \tau$. In this case, there are some ranges where $V_{GS}(t) < V_{GS(TYP)}$ is not satisfied and the on-resistance of the PMOS transistor is increased. We need a new design guideline that ensures the proposed circuit works correctly even though k is varied, i.e., we have to choose R_1 and C_c such that the time constant is larger than τ in the worst case.

Table 1. Variation of k with change of p and q

p \ q	-20%	-10%	0%	10%	20%
-20%	14.5%	13.5%	12.7%	11.9%	11.2%
-10%	12.8%	11.9%	11.2%	10.5%	9.9%
0%	11.4%	10.7%	10.0%	9.4%	8.9%
10%	10.3%	9.6%	9.1%	8.5%	8.1%
20%	9.4%	8.8%	8.3%	7.8%	7.4%

Now, we set R_1' as the adjusted resistance of R_1. If p is within $\pm p_{MAX}$, then $R_1'(1 - p_{MAX}) = R_1$ should be satisfied to ensure $R_1' \ge R_1$. Thus, R_1' is expressed as Eq. (27).

$$R_1' = R_1 / (1 - p_{MAX}) \tag{27}$$

In the same way, we can obtain the adjusted capacitance C_c' as Eq. (28), where q is within $\pm q_{MAX}$.

$$C_c' = C_c / (1 - q_{MAX}) \tag{28}$$

The adjusted resistance R_1' and capacitance C_c' are used instead of R_1 and C_c.

4. Experiments

The proposed level shifter was applied to the high side Buck converter as shown in Fig. 3, where an inductor L of 82 mH and a capacitor C_1 of 0.5 μF are used, and a Fairchild FQD2P40 PMOS transistor is selected. The specification of the PMOS is as follows: the maximum gate capacitance $C_{g(max)}$ = 0.55 nF, the maximum threshold voltage $V_{T(max)}$ = –3 V, the minimum threshold voltage $V_{T(min)}$ = –5 V, the typical turn-on voltage $V_{GS(TYP)}$ = –10 V, and the minimum allowed gate-to-source voltage $V_{GS(MIN)}$ = –30 V. In this design, we set the parameter k = 10%, V_{DDH} = 380 V, and V_{DDL} = 20 V. With these parameters, the capacitance C_c and the resistance R_1 were determined to be C_c = 0.78 nF and R_1 = 63.3 kΩ as described in Section 3. The resistor used in this experiment has a tolerance of ±1% and temperature coefficient of ±100 ppm/°C, so we set the maximum error rate of the resistor as p_{MAX} = 2%. The capacitor used in this experiment (ECWU type from Panasonic) has a tolerance of ±5% and capacitance variation of ±1% in the range of -30 °C – 80 °C, so we set the maximum error rate of the capacitor as q_{MAX} = 6%. The adjusted capacitance and resistance from Eq. (28) and (27) are C_c' = 0.83 nF and R_1' = 64.6 KΩ, respectively. In this experiment, we selected available capacitor and resistor as C_c' = 1 nF and R_1' = 68 kΩ. In this case, the voltages of V_A and V_B were calculated to be V_A = –11.3 V and V_B = –12.2 V based on Eqs. (5) and (6), respectively.

Fig. 8 shows the experimental configuration. An N5752A high voltage power supply (Agilent Technology) was used to generate 380 V, and IWS-S5552 LEDs (Itswell) were used in the LED string where 100 LEDs are

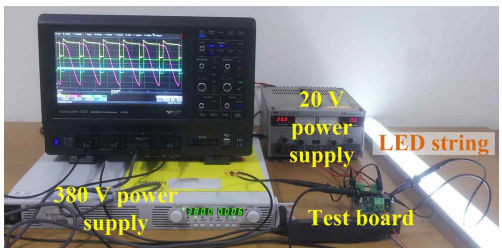


Fig. 8. Experimental configuration.

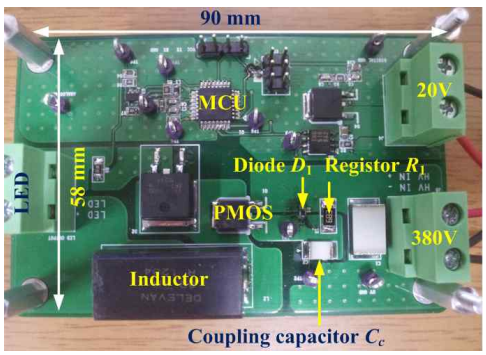


Fig. 9. Implementation of the proposed circuit.

connected in series. Fig. 9 shows the implemented circuit board whose size is 90 mm × 58 mm.

In the first experiment, we measured the level-shifted high voltage PWM signal without connecting the LED string; i.e., the current flowing into the LED string was zero, and the drain node was floated. Fig. 10 shows the voltage of the PWM control signal $v_c(t)$ and the voltage of the gate node signal that is the level-shifted high voltage PWM signal. The frequency of the control signal is 125 kHz and the duty ratio of the signal is 0.762.

The theoretical voltage of V_1 is 368.5 V from Eq. (3). Our experimental results show that V_1 is 367.4 V (Fig. 10). There is a voltage difference of 1.1 V between the theoretical voltage and the experimental voltage. When a MOS transistor operates in linear mode, C_{gs} and C_{gd} have the same capacitance of $C_{g(max)}$ / 2 if the source and the drain are connected at the same potential [19]. In this experiment, the PMOS transistor was operated in linear mode when the transistor was in the turn-on state, but C_{gd} was less than $C_{g(max)}$ / 2 because the drain node was floated. Thus, the gate capacitance was less than $C_{g(max)}$, which gave a lower value of V_1 than the theoretical voltage.

In the second experiment, we measured the level-shifted PWM signal with the connecting LED string. Fig. 11 shows the voltage of the gate node that was measured under the same conditions as the first experiment, except for the connecting LED string. In Fig. 11, V_1 is 368.5 V,

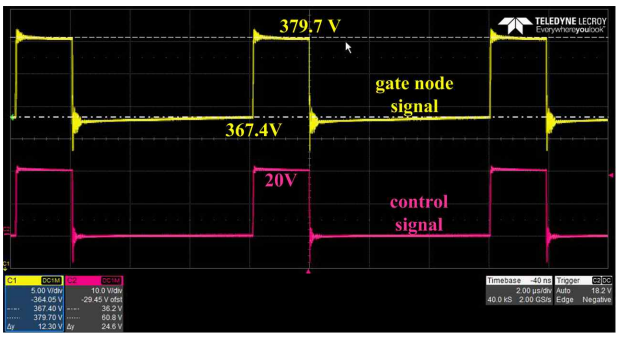


Fig. 10. Low voltage PWM signal and level-shifted high voltage PWM signal without connecting LED string.

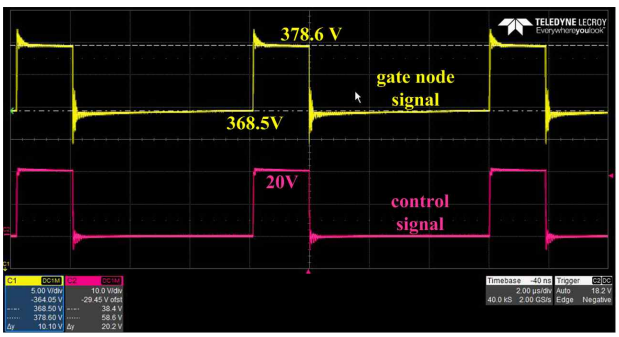


Fig. 11. Low voltage PWM signal and level-shifted high voltage PWM signal with connecting LED string.

which is the same as the theoretical value calculated by using Eq. (3). The voltage V_A = –11.5 V ($V_A = V_1 - V_{DDH}$) was lower than $V_{GS(TYP)}$. Thus, the PMOS transistor was in a sufficiently turn-on state at low level of the gate node voltage.

When the control signal was increased from 0 to 20 V, the voltage of the gate node became 381 V, which is about V_{DDH} plus V_D. Then, the voltage of the gate node decreased by more than the expected value and became 378.6 V. The phenomenon is due to the voltage change of the PMOS drain node from 380 to 0 V with the small capacitance of several pF between the gate and the drain when the PMOS transistor is turned off. However, the lowest voltage of the gate node is 378.6 V at high level, and this gives V_{GS} = –1.4 V, which is higher than the worst-case threshold voltage $V_{T(max)}$ = –3 V. Thus, the PMOS transistor kept the turn-off state at high level of the gate node voltage. This phenomenon can be reduced by connecting one or two diodes with diode D_1 in series, or by increasing the capacitance of C_c. Fig. 12 shows the current of the LED string, which is about 80 mA.

The proposed method uses the property of a PWM signal, which transits between a low and high level repeatedly at a frequency. Theoretically, the proposed circuit can work in $0 \le T_1 < T$. In the third experiment, we measured the maximum duty ratio wherein the proposed circuit works correctly. We then define that $V_{A(with)} = V_A$ when the LED string is connected, and $V_{A(without)} = V_A$ when the LED string is not connected. If $V_{A(with)} \le V_{GS(TYP)}$ is satisfied, the circuit works correctly at the duty ratio because the PMOS transistor is sufficiently switched on for $0 \le t < T_1$ and off for $T_1 \le t < T$. However, it is quite difficult to increase the duty ratio in the high side Buck converter when the LED string is connected, because the current flowing into the LED string is exponentially increased as the duty ratio is increased.

In this experiment, we used $V_{A(without)}$ instead of $V_{A(with)}$. However, there is a voltage difference between $V_{A(with)}$ and $V_{A(without)}$, and the difference is 1.1 V at a duty ratio of 0.762 from the first and second experiments shown in Figs. 10 and 11; i.e., $V_{A(with)} = V_{A(without)} + 1.1$ V. By considering the voltage difference, we approximately determined that the proposed circuit works correctly at the given duty ratio if

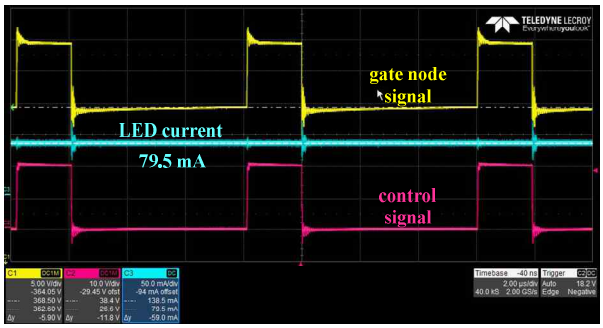


Fig. 12. Current flowing into the LED string.

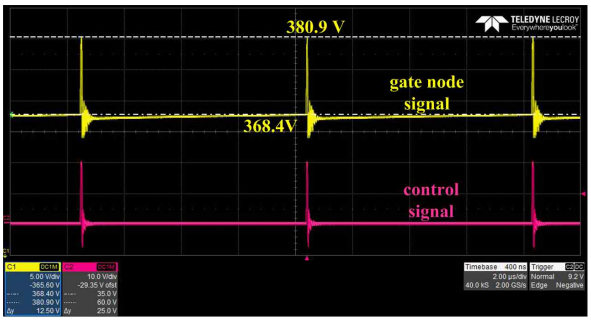


Fig. 13. High voltage PWM signal without the connecting LED string at a duty ratio of 0.9941.

$V_{A(without)}+1.1 \leq V_{GS(TYP)}$ is satisfied. Fig. 13 shows the high voltage PWM signal at a duty ratio of 0.9941. $V_{A(without)}$ is –11.6 V (=368.4–380 V) that satisfies $V_{A(without)} + 1.1 \leq V_{GS(TYP)}$. Thus, the proposed circuit works correctly at a duty ratio of 0.9941. However, $V_{A(without)}$ is –10.45 at a duty ratio of 0.9961, thus the proposed circuit does not work correctly at a duty ratio of 0.9961 because $V_{A(without)} + 1.1 \leq V_{GS(TYP)}$ is not satisfied. Thus, the proposed circuit works correctly up to a duty ratio of 0.9941.

Now we will compare the proposed method with the gate driver using pulse transformer in Fig. 2(e). The gate driver using pulse transformer addressed in Section 2 has the advantages that the driver can drive an NMOS transistor and it does not require isolated power supplies to drive the secondary-side NMOS transistor. However, the driver usually takes more components and requires the design of the transformer or at least the understanding of its operation and specification. The proposed method is very simple and easy to design, and works correctly up to a duty ratio of 99.5%, but the method is not applicable to an NMOS transistor. Another limitation of the proposed circuit is that the circuit may not work correctly if the frequency of the PWM signal applied to the circuit is lower than the target frequency.

5. Conclusion

We propose a high voltage level shifter using a coupling capacitor. Although the proposed circuit is a simple structure consisting of a low voltage PWM signal driver, a coupling capacitor, a resistor, and a diode, the proposed circuit can level a low voltage PWM signal up to high voltage PWM signal. The behavior of the level shifter was mathematically analyzed and a method to determine the capacitance of the coupling capacitor C_c and the resistance of the resistor R_1 is proposed. The proposed level shifter was applied to a high side Buck converter to drive the LED string. In the experiment, the input voltage of the converter was 380 V and the LED string consists of 100 LEDs connected in series. Our experimental results show that the proposed circuit converts a low voltage (0 to 20 V) PWM signal to a high voltage (370 to 380 V) PWM signal with a duty ratio of up to 0.9941.

Acknowledgements

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References

[1] G. S. Seo, K. C. Lee, and B. H. Cho, "A new DC anti-islanding technique of electrolytic capacitor-less photovoltaic interface in DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1632-1641, Apr. 2013.

[2] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential DC distribution systems – part one: high-density two-state topology," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1655-1666, Apr. 2013.

[3] Y. K. Tan, T. P. Huynh, and Z. Wang, "Smart personal sensor network control for energy saving in DC grid powered LED lighting system," *IEEE Trans. Smart Grid*, vol. 4, no. 2, pp. 669-676, Jun. 2013.

[4] G. S. Seo, B. H. Cho, and K. C. Lee, "DC level dimmable LED driver using DC distribution," in *Proc. ECCE*, 15-19 Sep. 2013, pp. 4650-4654.

[5] S. Matta and S. M. Mahmud, "An intelligent light control system for power saving," in *Proc. IECON*, 7-10 Nov. 2010, pp. 3316-3321.

[6] H. S. Jeong and C. K. Park, "A study on optical losses for tubular LED lamp's component," *J Korean Inst Illum Electr Install Eng*, vol. 25, no. 7, pp. 1-8, Jul. 2011.

[7] C. G. Yoon, H. K. Choi, J. Y. Park, Y. J. Song, K. W. Lee, and I. H. Jung, "Analysis tubular LED lamps location of the difference in brightness," in *Proc. Autumn Annual Conference of the Korean Institute of Illuminating and Electrical Installation Engineers*, 23 Nov. 2011, pp. 98-101.

[8] Z. Liu and H. Lee, "A 100V gate driver with sub-nanosecond delay capacitive-coupled level shifting and dynamic timing control for ZVS-based synchronous power converters," in *Proc. CICC*, 22-25 Sep. 2013, pp. 1-4.

[9] V. Javadian and S. Kaboli, "Reliability assessment of some high side MOSFET drivers for Buck converter," in *Proc. EPECS*, 2-4 Oct. 2013, pp. 1-6.

[10] I. H. Oh, "An analysis of current accuracies in peak and hysteretic current controlled power LED drivers," in *Proc. APEC*, 24-28 Feb. 2008, pp. 572-577.

[11] Y. Moghe, T. Lehmann, and T. Piessens, "Nano-

second delay floating high voltage level shifters in a 0.35 um HV-CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485-497, Feb. 2011.
[12] J. Liu, L. Deng, J. Zaho, and H. Liao, "A 1.8 V to 10 V CMOS level shifter for RFID transponders," in P*roc*. *ICSICT*, 1-4 Nov. 2010, pp. 491-493.
[13] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2V 0.13um CMOS," in *Proc*. *ICECS*, 10-13 Dec. 2006, pp. 668-671.
[14] B. Choi, "Enhancement of current driving capability in data driver ICs for plasma display panels," *IEEE Trans. Consumer Electron.*, vol. 55, no. 3, pp. 992-997, Aug. 2009.
[15] M. Wendt, L. Thoma, B. Wicht, and D. Schmitt-Landsiedel, "A configurable high-side/low-side driver with fast and equalized switching delay," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1617-1625, Jul. 2008.
[16] T. Lehmann, "Design of fast low-power floating high-voltage level-shifters," *Electronics letters*, vol. 50, no. 3, pp. 202-204, Jan. 2014.
[17] S. C. Tan and X. W. Sun, "Low power CMOS level shifters by bootstrapping technique," *Electronics letters*, vol. 38, no. 16, pp. 876-878, Aug. 2002.
[18] M. H. Rashid, Power electronics handbook: devices, circuits, and applications handbook. 3rd ed., Burlington, MA, USA: Butterworth-Heinemann, 2011, pp. 557-558.
[19] N. Weste and D. Harris, CMOS VLSI Design: A circuits and systems perspective. 3rd ed., Boston, MA, USA: Pearson Education, 2005, pp. 75-80.

Kwang-Su Seong He received the B.S. degree in electronic engineering from Hanyang University, Seoul, Korea in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1992 and 1997, respectively. He is currently an Associate Professor with the Department of Electronic Engineering, Yengnam University, Gyeongbuk, Korea. His current research interests include capacitive sensors, MCU design, and wireless power transmission for mobile devices.