J Electr Eng Technol.2016; 11(1): 100-108
http://dx.doi.org/10.5370/JEET.2016.11.1.100

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Simple High Efficiency Full-Bridge DC-DC Converter using a Series Resonant Capacitor

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Abstract – This paper presents a simple high efficiency full-bridge DC-DC converter using a series resonant capacitor. The proposed converter achieves the zero voltage switching of the primary switches under a wide range of load conditions and reduces the high circulating current in the freewheeling mode using the leakage resonant inductance and the series resonant capacitor. Thus, the proposed converter overcomes the drawbacks of the conventional full-bridge DC-DC converter and improves its overall system efficiency. Its structure is simplified by using the leakage inductance of the transformer as the resonant inductance and omitting the DC output filter inductance. Also it can operate over a wide range of input voltages. In this paper, the operational principle, analysis and design example are described in detail. Finally, the experimental results from a 650W (24V/27A) prototype are demonstrated to confirm the operation, validity and features of the proposed converter.

Keywords: Soft switching, Full-bridge converter, Circulating current, Leakage resonant inductance, Series resonant capacitor

1. Introduction

Generally, in order to minimize the total size of pulse-width modulation (PWM) converters, their switching frequency is increased. However, increasing the switching frequency causes a substantial increase in the switching losses, which causes the converter efficiency to be deteriorated. Therefore, the switching losses of the converter must be minimized when it operates with a high switching frequency [1, 2].

Recently, various types of converter topologies and control techniques have been proposed for high frequency power conversion to reduce the switching losses in conventional PWM converters. Among them, the full-bridge zero voltage switching (ZVS) DC-DC converter combines and utilizes the benefits of both the ZVS quasi-resonant converter and PWM technique, while avoiding their major drawbacks. Therefore, the full-bridge ZVS DC-DC converter has been deemed the most desirable for many applications. This type of converter is controlled by the phase-shift method and achieves ZVS using the resonance between the switch parasitic capacitor and resonant inductor without any additional resonant components. As a result, the switching losses are reduced and the current stresses become relatively low. In addition, because the converter operates with a fixed frequency, the design optimization of the converter circuit is easily attainable [3-5].

However, there are a few serious disadvantages to the conventional full-bridge ZVS DC-DC converter, such as its narrow ZVS range, effective turn-on duty loss, and load-dependent DC characteristics. Because the conventional full-bridge DC-DC converter achieves ZVS over its entire load range using the resonant inductor energy to discharge the parasitic capacitance of the primary switches, a very large resonant inductance is needed to ensure ZVS under light loads. However, this large resonant inductance causes a large freewheeling current under the rating load condition, which causes the conduction losses and current/voltage stresses of the primary switches to increase and induces turn-off switching losses. Also, the converter exhibits the ring phenomenon due to the parasitic capacitor of the secondary rectification diode and the resonant inductance, which leads to switching losses and switching noise. These are the major drawbacks of the conventional full-bridge DC-DC converter.

Therefore, many methods of overcoming these drawbacks have been proposed [6-11]. In one such method, passive auxiliary circuits of parallel type are connected to both legs of the conventional full-bridge converter to achieve the ZVS of the primary switches over the entire load range [6]. However, the current flowing through the auxiliary circuits increases the conduction loss and decreases the power conversion efficiency under heavy loads. To solve this problem, adaptive auxiliary circuits and their associated control techniques are introduced to reduce the conduction loss and large turn-on duty loss under heavy load conditions [7-9]. This provides a partial solution to the problem of [6], but results in an expensive and bulky system. In another method, a series boost capacitor is inserted and the pulse-frequency-modulation (PFM) method is applied to reduce the freewheeling current at the converter primary and ripple current in the output inductor [10].

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Received: January 12, 2015; Accepted: July 26, 2015

However, this technique is difficult for the design optimization of the magnetic components, due to the variation in the switching frequency resulting from the PFM operation of the converter [9, 11]. In [12], an auxiliary circuit with an active switch in the converter secondary side is added, and another auxiliary circuit with a third auxiliary winding of the main transformer is suggested in [13] and [14] for the zero current switching (ZCS) of the lagging leg. In [15] and [16], a blocking capacitor, saturable inductor and some auxiliary components are inserted and utilized in the converter primary side to decrease the freewheeling current. However, the use of auxiliary circuits with an active switch or third auxiliary winding in [12-14] makes the converters expensive and bulky, and the saturable inductor in [15] and [16] causes heat problems.

Generally, it is reasonable for an output filter inductor to be utilized to reduce the current stress on both sides of the transformer of a DC-DC converter operating at a low output voltage and high output current [17]. However, this causes large power losses, such as core and conduction losses and makes the DC-DC converter bulky and expensive. In addition, a very large circulating energy is needed to achieve the ZVS operation of the converter switches. To resolve these problems, the full-bridge LLC resonant converter is frequently used, which has many good characteristics, such as its simple structure, excellent ZVS operation, and the low voltage stress of main power switches [18, 19]. However, this converter also has problems, such as a higher current stress and larger conduction loss on both sides of the transformer.

In this paper, to resolve the above problems, a simple high efficiency full-bridge DC-DC converter using a series resonant capacitor is proposed. The proposed converter uses a leakage resonant inductance and a series resonant capacitor for the ZVS operation of the main switches and the reduction of the high circulating current in freewheeling mode. Thus, the proposed converter resolves the problems of the conventional full-bridge DC-DC converter and improves its overall system efficiency. Since the proposed converter uses the leakage inductance of the transformer as the resonant inductance and does not have any DC output filter inductance, its structure is simplified. Moreover, it operates over a wide range of input voltages. In this paper, the operational principle, analysis and a design example of the proposed converter are explained in detail. The experimental results from an implemented prototype based on the analysis and design example are provided to show the operation, validity and features of the proposed converter.

2. Operational Principles

Figs. 1 and 2 show the circuit diagram and theoretical operating waveforms in the steady state of the proposed

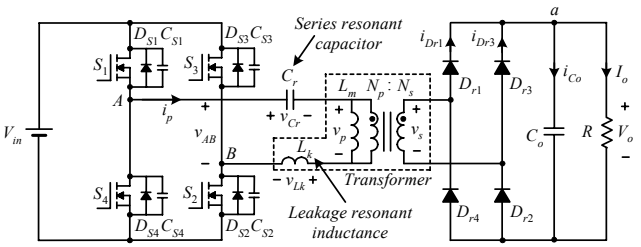


Fig. 1. The circuit diagram of the proposed full-bridge DC-DC converter

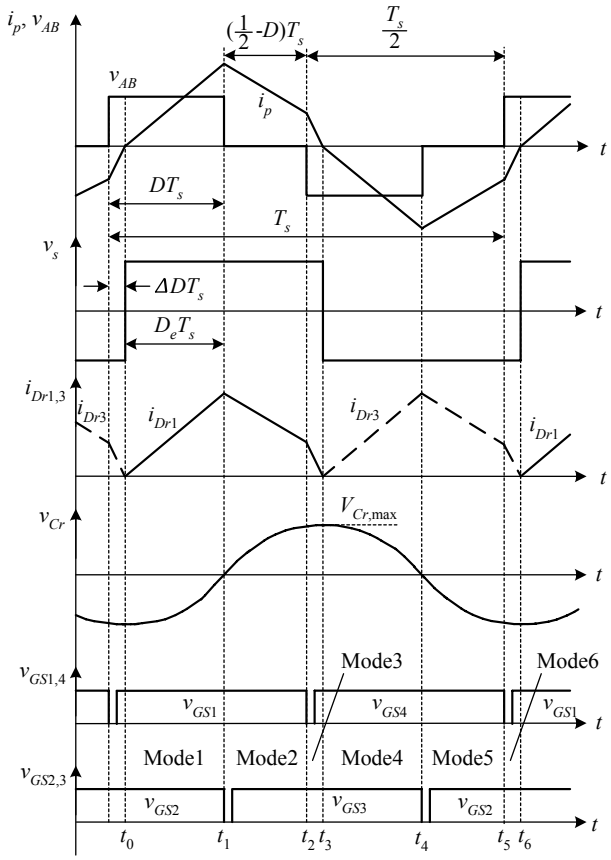


Fig. 2. The theoretical operating waveforms of the proposed converter in the steady state

full-bridge DC-DC converter, respectively. The proposed converter is controlled using the phase-shift method. The proposed converter uses the leakage inductance L_k of the transformer and the series capacitor C_r for the ZVS operation of the main switches and reduction of the high circulating current and does not have a DC output filter inductance. The leakage inductance L_k is much smaller than the magnetizing inductance L_m and is used as the resonant inductance; the series capacitor C_r is used as the resonant capacitance, which is simply inserted into the primary structure of the conventional full-bridge converter. Thus, the converter has a simple structure and its overall system efficiency is improved.

However, the proposed converter differs from the LLC resonant converter, because the magnetizing inductance is

much larger than the resonant inductance, which is the leakage inductance in the proposed converter. The LLC converter should operate in a wide switching frequency range to satisfy the wide input voltage requirement, which makes the optimized design of the transformer difficult. Also, the LLC converter regulates the DC output voltage by varying the switching frequency, which is an obstacle in terms of the controllability for load variation. Therefore, a large transformer core is needed, resulting in a large core loss and low power density in the nominal state. However, because the LLC converter with a wide input voltage range must have a small magnetizing inductance to obtain a high peak gain, large conduction losses arise in the converter primary side. Thus, the LLC converter can achieve high efficiency and high power density only if operating at around the resonant frequency, resulting in a very narrow input voltage range and limited output voltage regulation capability [20-22].

However, the proposed converter achieves the regulation of the DC output voltage using the phase-shift method with the fixed switching frequency. Therefore, the optimized design of the transformer and the control for the output load variation are straightforward and the input voltage range of the proposed converter is wide. Furthermore, the proposed converter easily achieves the ZVS of all the primary switches in a wide load range and reduces the primary conduction loss using the phase-shift method and the resonant circuit network (L_k–C_r). Thus, the proposed converter easily achieves high efficiency. Because the proposed converter utilizes the leakage inductance L_k as the resonant inductance, its structure is simple. The proposed converter has low voltage stress on the secondary rectifier diodes because there is no output filter and no reverse recovery, and it can more easily implement the over current protection function compared with the LLC converter of varied switching frequency.

As shown in Fig. 2, each switching period can be subdivided into six modes and the equivalent circuits of each mode are shown in Fig. 3. The switches of each leg are turned on and off alternately with a 50%-constant duty ratio and the legs are controlled by the phase-shift method. The phase difference between the two legs determines the duty ratio, as shown in Fig. 2.

In order to illustrate the steady state operation of each mode, the following assumptions are made:

1) Switches S_1~S_4 are ideal except for the antiparallel diodes D_{S1}~D_{S4} and the parasitic capacitors C_{S1}~C_{S4} of each switch.
2) The secondary full-bridge rectifier diodes D_{r1}~D_{r4} are ideal and the junction capacitances of each rectifier diode are ignored.
3) The transformer is an ideal transformer with turn ratio

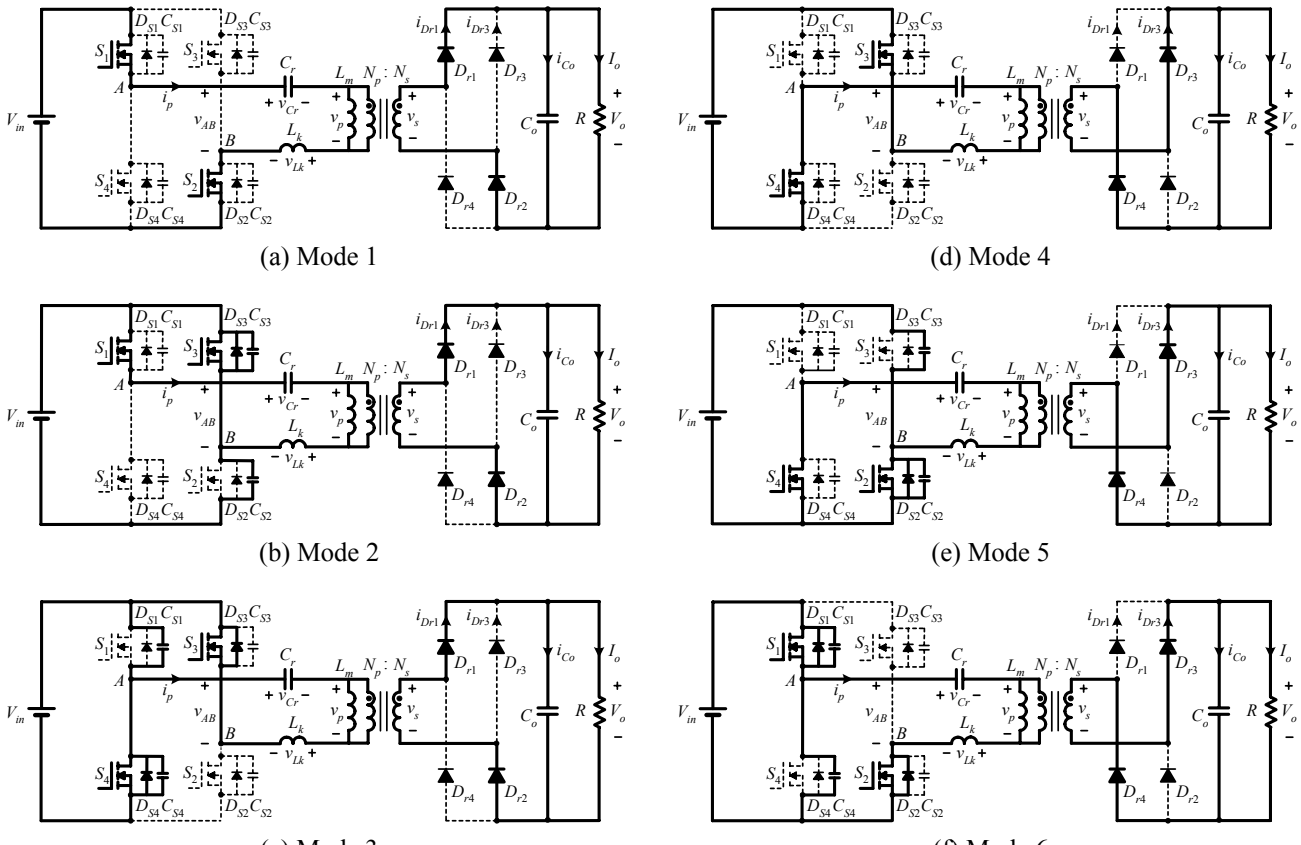


Fig. 3. The equivalent circuits of each mode of the proposed converter

n ($=N_s/N_p$) including the magnetizing inductance L_m and the leakage inductance L_k.

4) Because the DC output capacitance C_o is very large, the DC output voltage V_o is constant.

It is assumed that before time $t=t_0$, the primary switches S_1 and S_2 are initially turned on with ZVS operation. The detailed mode analysis of the proposed converter is as follows:

Mode 1 [t_0~t_1]: The primary switches S_1 and S_2 are in the on state at time $t=t_0$. The transformer transfers the input power to the output side through the primary switches S_1 and S_2 and the secondary diodes D_{r1} and D_{r2}. This mode is the powering mode. Because the current in each secondary diode is commutated instantaneously and completely at time $t=t_0$, the secondary diodes D_{r1} and D_{r2} are conducting, and the other secondary diodes D_{r3} and D_{r4} are turned off. Being inversely proportional to the transformer turn ratio n, the secondary output voltage V_o is reflected on the primary side of transformer. Therefore, the primary voltage equation of the converter is given as follows:

$$L_k \frac{di_p}{dt} + \frac{V_o}{n} + v_{Cr} = V_{in} \tag{1}$$

Then, the primary current i_p is calculated as follows:

$$i_p = \frac{V_{in} - V_o / n - v_{Cr}}{L_k}(t - t_0) \tag{2}$$

The series resonant capacitor voltage v_{Cr} is nonlinearly charged by the primary current i_p as follows:

$$v_{Cr} = \frac{1}{C_r}\int i_p dt \tag{3}$$

In this mode, because the series resonant capacitor voltage v_{Cr} is negative, as shown in Fig. 2, the average value of the transformer primary voltage v_p ($=V_{in}-v_{Lk}-v_{Cr}$) increases and, thus, the voltage conversion ratio of the proposed converter also increases.

When switch S_2 is turned off at time $t=t_1$, mode 1 ends.

Mode 2 [t_1~t_2]: After switch S_2 is turned off at time $t=t_1$, the primary current i_p charges the parasitic capacitor C_{S2} of switch S_2 and discharges the parasitic capacitor C_{S3} of switch S_3. When the drain-source voltage of switch S_3 reaches zero, the primary current i_p flows through the antiparallel diode D_{S3} of switch S_3. After the dead time, switch S_3 is turned on at zero voltage. The energy stored in the leakage resonant inductance L_k in mode 1 discharges through the secondary rectifier diodes D_{r1} and D_{r2} toward the output in this mode. Being inversely proportional to the transformer turn ratio n, the secondary output voltage V_o is reflected on the primary side of transformer. Therefore, the primary voltage equation of the converter is given as follows:

$$L_k \frac{di_p}{dt} + \frac{V_o}{n} + v_{Cr} = 0 \tag{4}$$

Then, the primary current i_p is calculated as follows:

$$i_p = -\frac{V_o / n + v_{Cr}}{L_k}(t - t_1) + i_p(t_1) \tag{5}$$

where $i_p(t_1)$ is the primary current at time $t=t_1$.

This mode is the freewheeling mode. As shown in Fig. 2 and (5), the slope of the primary current i_p is negative, which is steeper than that of the conventional full-bridge DC-DC converter. This is due to the inserted series resonant capacitor C_r. Thus, the circulating energy afforded by the freewheeling current becomes smaller compared with that of the conventional full-bridge converter. However, in order to ensure the ZVS operation of the lagging leg switches (S_2 and S_3) and minimize their conduction loss, the series resonant capacitor C_r must be designed properly.

When switch S_1 turns off at time $t=t_2$, mode 2 ends.

Mode 3 [t_2~t_3]: This mode is the regeneration mode. After switch S_1 is turned off at time $t=t_2$, the primary current i_p charges the parasitic capacitor C_{S1} of switch S_1 and discharges the parasitic capacitor C_{S4} of switch S_4. When the drain-source voltage of switch S_4 reaches zero, the primary current i_p flows through the antiparallel diode D_{S4} of switch S_4. After the dead time, switch S_4 is turned on at zero voltage. Therefore, the primary voltage equation of the converter is given as follows:

$$L_k \frac{di_p}{dt} + \frac{V_o}{n} + v_{Cr} = -V_{in} \tag{6}$$

Then the primary current i_p is calculated as follows:

$$i_p = -\frac{V_{in} + V_o / n + v_{Cr}}{L_k}(t - t_2) + i_p(t_2) \tag{7}$$

where $i_p(t_2)$ is a primary current at time $t=t_2$.

The series resonant capacitor voltage v_{Cr} is nearly maximum ($v_{Cr} \fallingdotseq V_{Cr,\max}$) in this mode. Due to the series resonant capacitor voltage v_{Cr}, the current i_p decreases more steeply than that of the conventional full-bridge converter. At time $t=t_3$, the series resonant capacitor voltage v_{Cr} becomes the maximum voltage $V_{Cr,\max}$, the secondary diode currents i_{Dr1} and i_{Dr3} are commutated instantaneously, and mode 3 ends.

Modes 4~6 [t_4~t_6]: As shown in Fig. 3(d)-(f), the operations of these modes are the same as the previous modes except for the fact that each operating MOSFET/diode and the primary current direction are opposite. Therefore, the explanation of these modes is omitted. At the end of mode 6, time $t=t_6$, one operation period is

completed and the operation of the converter is repeated.

3. Analysis and Design Example

The analysis and design example of the proposed converter are presented in this section. To validate the characteristics of the proposed converter, a prototype converter is designed with the following specifications:

- DC input voltage: V_{in}=255~375V
- DC output voltage / maximum output current: V_o=24V / I_o=27A
- Maximum output power: $P_{o,\max}$=650W
- Switching frequency: f_s=100kHz

The DC input voltage of the prototype converter is generated from the sinusoidal AC input voltage through a full-bridge diode rectifier and a filter capacitor for smoothing the DC input voltage. The AC input voltage range for the generation of the DC input voltage specification is v_{AC}=180~265V and the rating DC input voltage is V_{in}= 311V when the AC input voltage is v_{AC}=220V.

In order to calculate the turn ratio n of the transformer of the proposed converter, the voltage conversion ratio of the converter is calculated simply by applying the volt-second balance rule to the leakage resonant inductance as follows:

$$V_o = nD_eV_{in} \tag{8}$$

where D_e is the effective duty ratio of the proposed converter and is defined as the difference between the overall duty ratio D and the duty ratio loss ΔD (D_e=D-ΔD). The duty ratio D is set to D=0.5, the maximum duty ratio, when the DC input voltage is minimum (V_{in}=255V). At this time, if the effective duty ratio D_e is set to D_e=0.4, which is 80% of the maximum duty ratio, as the nominal effective duty, the turn ratio n is calculated from (8) and selected as n=0.2.

From the peak primary current $I_{p,pk}$, the leakage inductance L_k is determined. If the Kirchhoff Current Law is applied to the secondary upper node 'a' of the proposed converter in Fig. 1, the average of the current equation during the switching period T_s is obtained as follows:

$$I_{Dr1} + I_{Dr3} = I_o \tag{9}$$

where I_{Dr1} and I_{Dr3} are the averages of the secondary diode currents i_{Dr1} and i_{Dr3}, respectively, the average current of i_{Co} is canceled by the ampere-second balance rule and I_o is the constant DC output current. Because i_{Dr1}=i_p/n and i_{Dr3}= $|i_p|/n$, (9) is rewritten as follows:

$$\frac{2}{T_s}\int_0^{\frac{T_s}{2}} \frac{i_p}{n}dt = I_o \tag{10}$$

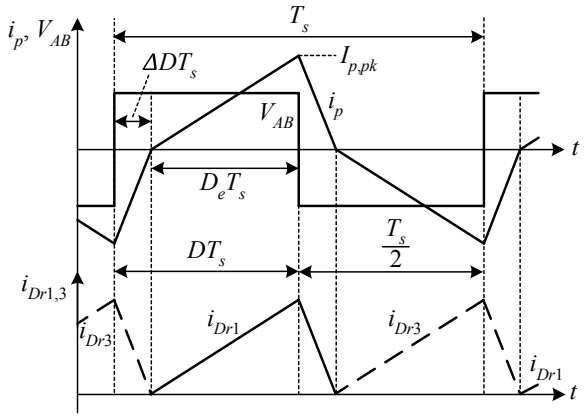


Fig. 4. The theoretical waveforms of the primary voltage and current and secondary current of the proposed converter, when the DC input voltage is minimum

However, when the DC input voltage is minimum, the theoretical waveforms of the primary voltage and current and secondary current of the proposed converter become as shown in Fig. 4. Therefore, the peak primary current $I_{p,pk}$ is obtained from Fig. 4 and (10) as follows:

$$I_{p,pk} = 2nI_o \tag{11}$$

Therefore, the peak primary current $I_{p,pk}$=$i_p(t_1)$ afforded by the given specifications is calculated as $I_{p,pk}$=10.8A. Also, the peak primary current $I_{p,pk}$=$i_p(t_1)$ is obtained from (2) as follows:

$$I_{p,pk} = i_p(t_1) = \frac{1}{L_k}\left(V_{in} - \frac{V_o}{n} - v_{Cr}(t_1)\right)D_eT_s \tag{12}$$

where the series resonant capacitor voltage $v_{Cr}(t_1)$ at time t=t_1 is ignored for convenience of the design, because it is a negligibly small value compared to the other voltage V_{in}− V_o/n. Then, from the calculated peak primary current and (12), the leakage inductance L_k is obtained as follows:

$$L_k = \frac{1}{I_{p,pk}}\left(V_{in} - \frac{V_o}{n}\right)D_eT_s \tag{13}$$

Therefore, the leakage inductance L_k of the prototype converter is calculated as L_k =50μH. The leakage resonant inductance L_k is realized on the transformer of the prototype converter by adjusting its core air-gap. The transformer of the prototype converter is realized using a core PQ5050 from TDK. Thus, the inductance L_k is adjusted to L_k=49μH (≒50μH).

The series resonant capacitance C_r can be calculated from the maximum voltage $V_{Cr,\max}$ of the series resonant capacitor C_r of mode 1 or 3. $V_{Cr,\max}$ is approximated and obtained from the ripple voltage Δv_{Cr} of the series resonant

capacitor C_r from (3) and (11) as follows:

$$V_{Cr,\max} = \frac{1}{2}\Delta v_{Cr} = \frac{1}{2}\cdot\frac{1}{2}\cdot\frac{I_{p,pk}}{C_r}\cdot\frac{T_s}{2} = \frac{nI_o \cdot T_s}{4C_r} \quad (14)$$

where I_o is the load current at the maximum power $P_{o,\max}$. Therefore, the series resonant capacitance C_r is deduced from (14) as follows:

$$C_r = \frac{nI_o \cdot T_s}{4V_{Cr,\max}} \quad (15)$$

However, in order for the slope of the primary current i_p to become positive from Fig. 2 and (2), $V_{Cr,\max}$ must satisfy the following relation:

$$V_{in} - \frac{V_o}{n} > v_{Cr} \approx V_{Cr,\max} \quad (16)$$

The series resonant capacitance C_r is calculated from (15). Since $V_{Cr,\max}$ must be sufficiently smaller than the voltage $V_{in}-V_o/n$, $V_{Cr,\max}$ is set to $V_{Cr,\max}$=67.5V, which is one half of the voltage $V_{in}-V_o/n$, when the input voltage is minimum, and is a margin value considering the converter design. Therefore C_r is calculated and determined to be C_r=0.2μF.

However, as the maximum series resonant capacitor voltage increases, the slope of the primary current i_p becomes steeper. Then, the circulating current is reduced and, thus, the conduction loss is also reduced. Also, because the primary current i_p is a function of the series resonant capacitor voltage v_{Cr}, the slope of i_p is actually determined by the magnitude of $V_{Cr,\max}$ as shown in (5) of mode 2. And because the primary current $i_p(t_2)$ at time $t=t_2$ must be positive to ensure the ZVS of the lagging leg switches, from (5), (14) and (16) the series resonant capacitance C_r must satisfy the following condition:

$$C_r > \frac{nI_o \cdot T_s}{4\left[\frac{L_k I_{p,pk}}{\left(\frac{1}{2}-D\right)T_s} - \frac{V_o}{n}\right]} \quad (17)$$

where $I_{p,pk}=i_p(t_1)$ is the peak primary current calculated by means of (12) with the realized leakage inductance value (L_k=49μH), and the duty ratio D can be induced from (5), (7), (8), Fig. 2 and $D=D_e+\Delta D$ as follows:

$$D = \left(1-\frac{V_{mode2}}{V_{mode3}}\right)^{-1}\left(\frac{V_o}{nV_{in}} - \frac{V_{mode2}}{2V_{mode3}} + \frac{L_k \cdot I_{p,pk}}{V_{mode3}\cdot T_s}\right) \quad (18)$$

$$V_{mode2} = \frac{V_o}{n} + V_{Cr,\max} \quad (19)$$

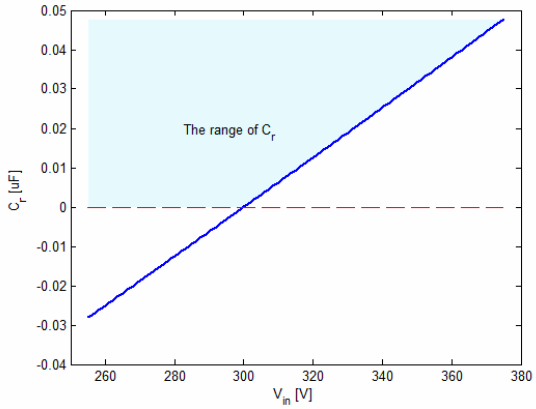


Fig. 5. The range of series resonant capacitance C_r for each calculated parameter

$$V_{mode3} = V_{in} + \frac{V_o}{n} + V_{Cr,\max} \quad (20)$$

Next, in order to verify the range of series resonant capacitance C_r for each calculated parameter, the range graph is plotted using (17), as shown in Fig. 5. Then, it is confirmed that the determined capacitance C_r value is reasonable.

4. Experimental Results

The prototype of the proposed converter was implemented based on the designed parameters given in Section 3. The prototype converter is controlled by a UC3879, which is a full-bridge phase-shift controller from Unitrode. Fig. 6 shows the simplified control block diagram of the prototype of the proposed converter, where the feedback, dead-time generator and internal protect circuits are omitted. The experimental waveforms of the proposed converter in Figs. 7-10 are obtained under the specifications of Section 3, where the labels of the current and voltage are the same as those in Fig. 6.

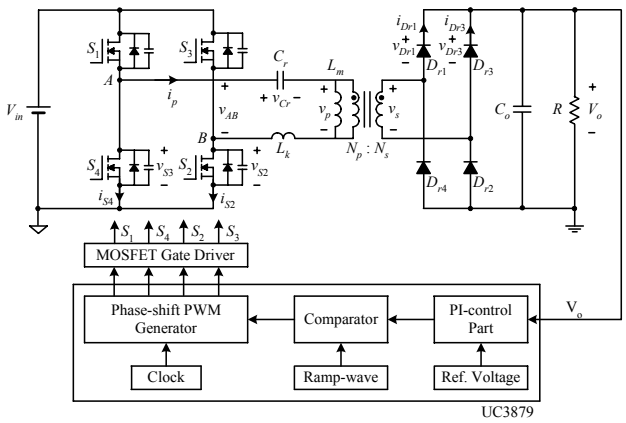


Fig. 6. The simplified control block diagram of the prototype of proposed converter

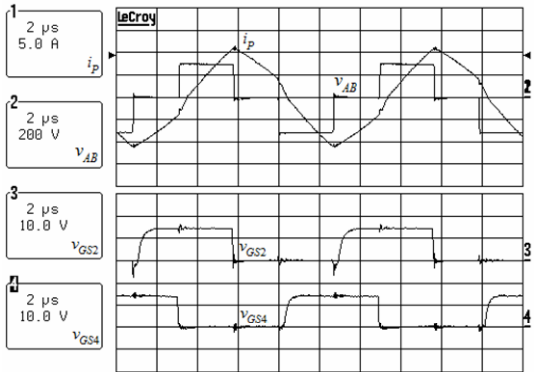


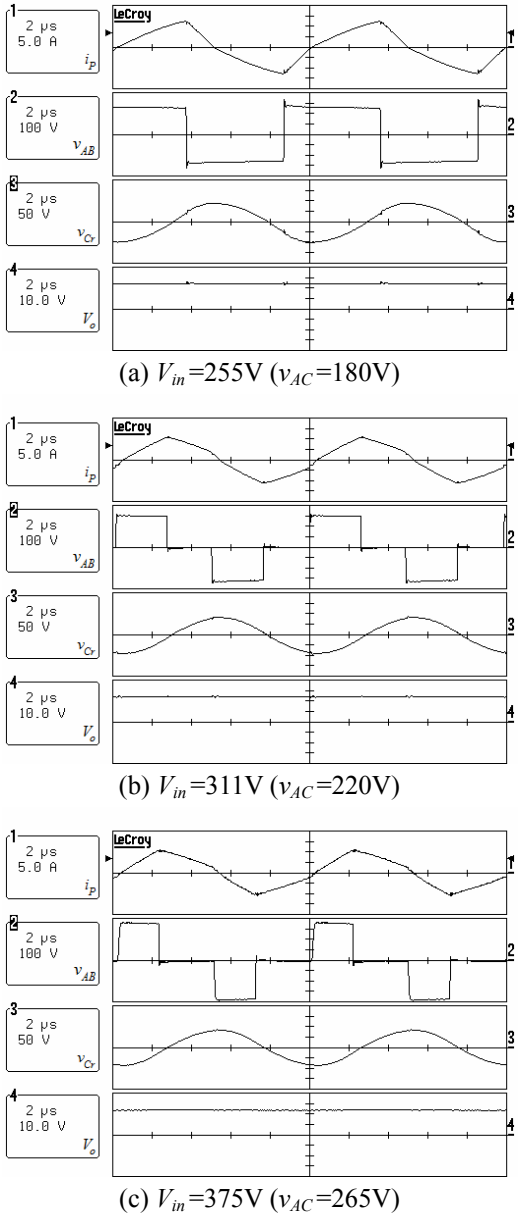
Fig. 7. The experimental waveforms of the primary voltage and current and the gate-source voltages of the primary switches of the proposed converter at the rating input voltage and the maximum output power

Fig. 7 shows the experimental waveforms of the primary voltage v_{AB} and current i_p and the gate-source voltages v_{GS2} and v_{GS4} of the primary switches S_2 and S_4 of the proposed converter at the rating input voltage V_{in}=311V and the maximum output power $P_{o,\max}$. Fig. 8 shows the experimental waveforms of the primary voltage v_{AB} and current i_p, series resonant capacitor voltage v_{Cr} and DC output voltage V_o of the proposed converter at the maximum output power $P_{o,\max}$ under each input voltage condition. The experimental waveforms of Figs. 7 and 8 show that the switches of the proposed converter operate with ZVS and that the DC output voltage is correctly controlled over the entire range of input voltages, and confirm that the theoretical explanation, analysis and prototype design of the converter proposed in this paper are correct.

Fig. 9 shows the experimental waveforms of the voltages v_{Dr1} and v_{Dr3} and currents i_{Dr1} and i_{Dr3} of the secondary diodes D_{r1} and D_{r3}, respectively, at the rating input voltage and maximum output power. These waveforms show that the secondary diodes of the proposed converter can turn-on and turn-off softly. This is due to the fact that the parasitic resonance has less effect on the secondary diode rectifier of the proposed converter than that of the conventional full-bridge converter.

Fig. 10 shows the experimental waveforms of the turn-on voltage v_{S2} and current i_{S2} of switch S_2 in the lagging leg when the proposed converter operates under light load conditions (about 5% of maximum load), which shows that the ZVS operation range of the proposed converter can be extended to very light loads.

These results are derived from the fact that the leakage inductance of the transformer is used as the resonant inductance and the series resonant capacitor is simply inserted into the primary structure of the conventional full-bridge converter. The series resonant capacitor makes the proposed converter use the leakage resonant inductance effectively in the discharging process of the parasitic capacitor of the lagging leg switches and reduces the



(a) V_{in}=255V (v_{AC}=180V)

(b) V_{in}=311V (v_{AC}=220V)

(c) V_{in}=375V (v_{AC}=265V)

Fig. 8. The experimental waveforms of the primary voltage and current, series resonant capacitor voltage and DC output voltage of the proposed converter at the maximum output power under each input voltage condition

circulation energy. Thus, the overall system efficiency of the proposed converter is improved.

Fig. 11 shows the efficiency comparison graph of the proposed and conventional converters, from which it can be concluded that the efficiency of the proposed converter is improved compared with that of the conventional one. The conventional converter used in this comparison is one implemented with the same specifications as the prototype of the proposed converter, but with only the separate resonant inductor and without the series resonant capacitor. The maximum efficiency of the proposed converter is 95% under the given specifications. The efficiency is

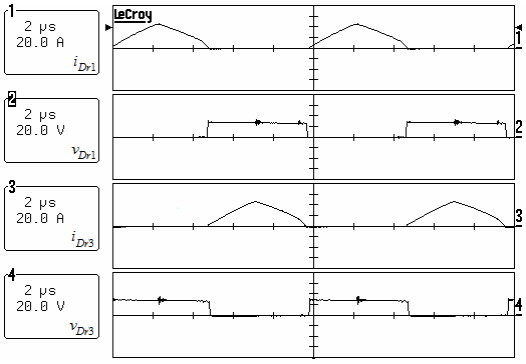


Fig. 9. The experimental waveforms of the voltages and currents of the secondary diodes at the rating input voltage and maximum output power

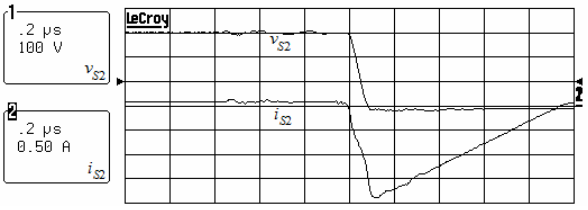


Fig. 10. The experimental waveforms of the turn-on voltage and current of the switch in the lagging leg when the proposed converter operates under light load conditions

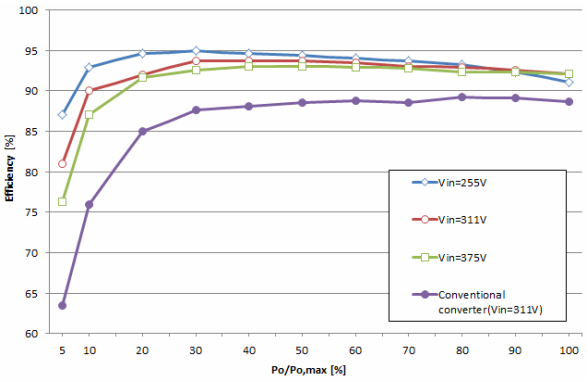


Fig. 11. The efficiency comparison graph of the proposed and conventional converters

measured using a Yokogawa WT500 power analyzer in this experiment.

5. Conclusion

In this paper, a simple high efficiency full-bridge DC-DC converter using a series resonant capacitor was proposed. The proposed converter achieves the ZVS of the converter primary switches and reduces the circulation current using the leakage resonant inductance that is implemented on the transformer and the series resonant capacitor that is simply inserted into the primary structure of the conventional full-bridge converter. The proposed converter does not use the secondary DC output filter inductance. Thus, its structure is simpler and its total efficiency is improved simply. The proposed converter overcomes the drawbacks of the conventional full-bridge converter, namely its large conduction loss and low efficiency. Also, the proposed converter can operate over a wide range of input voltages. In this paper, the operational principle, analysis and design example of the proposed converter were explained in detail. Finally, the experimental results from a prototype were shown to confirm the operation, validity and features of the proposed converter.

Acknowledgements

This work was supported by the Soonchunhyang University Research Fund.

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