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Zero-Voltage-Transition Synchronous DC–DC Converters with Coupled Inductors

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Abstract

A new family of zero-voltage-transition converters with synchronous rectification is introduced in this study. Soft switching condition for all the converter operating points is provided in the proposed converters. The reverse recovery losses of the rectifier switch body diode are also eliminated. In comparison with the main switch voltage stress, the auxiliary switch voltage stress is reduced significantly. The auxiliary switch does not need the floating gate drive. The auxiliary inductor is coupled with the main converter inductor, and the leakage inductor is used as the resonance inductor. Thus, all inductors of the proposed converter can be implemented on a single core. The other features of the proposed converters include no extra voltage and current stresses on the main converter semiconductor elements. Theoretical analysis for a synchronous buck converter is presented in detail, and the validity of the theoretical analysis is justified with the experimental results of a prototype buck converter with 180 W and 80 V to 30 V.

Key words: Coupled inductors, Synchronous converters, Synchronous rectifier, Zero voltage switching

I. INTRODUCTION

Synchronous rectification is widely applied in low-voltage converters to improve power conversion efficiency. In the synchronous converters, a power switch with on-resistances in order of milliohms, namely, synchronous rectifier (SR) switch, is used instead of a diode. Thus, conduction losses are reduced given that the forward voltage drop of the diodes is noticeable at low-output voltages [1]-[3]. The main drawback of the synchronous converters is the reverse recovery losses of the low-speed SR switch body diode. Before the main switch turns on instantly, the SR switch is turned off and its body diode conducts for a short time. Hence, the reverse recovery time of the SR switch body diode occurs when the main switch is turned on, thereby causing a large current spike in the main switch [4]. This problem significantly contributes in increasing switching losses and EMI. The high-frequency power conversion is also limited. However, high-operating frequency is desirable to achieve high power density by reducing the converter reactive components size [5], [6]. Soft-switching techniques are employed to resolve these problems.

Among the soft-switching techniques, zero-voltage-transition (ZVT) technique is widely used in many converters because of common features, such as low circulating current, retaining PWM operation, and wide load soft-switching range [7]-[10]. In general, ZVT technique provides zero-current switching (ZCS) condition for the converter main diode at turn-off and zero-voltage switching (ZVS) condition for the main switch through an additional auxiliary switch and some passive elements. Consequently, ZVT technique decreases the switching losses and EMI. The reverse recovery losses of the SR switch body diode losses can also be reduced significantly by applying ZVT techniques to the synchronous converters. In [1], [2], [11]-[13], ZVT technique is applied to the synchronous converters to improve efficiency and to overcome the SR reverse recovery problem. However, the converter of [11] suffers from numerous auxiliary elements. In [11], [12], the voltage stress on the auxiliary switch is equal to or higher than the main switch voltage stress. Given that the auxiliary switch in ZVT converters is turned on under ZCS condition, increased voltage stress results in increased capacitive turn-on losses. In

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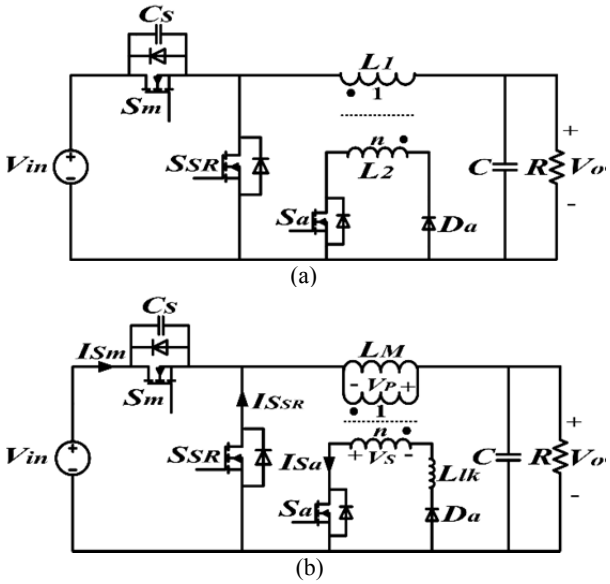


Fig. 1. Proposed ZVT synchronous buck converter and its equivalent circuit. (a) Proposed converter. (b) Equivalent circuit.

conventional power switches, low-voltage switches also benefit from the low value of on-resistance $R_{D(on)}$, thereby resulting in low conduction losses. In the ZVT synchronous converters of [1], [2], [13], the voltage stress on the auxiliary switch is reduced to approximately half of the main switch voltage stress. The reverse recovery losses of the SR switch body diode are totally eliminated. However, the auxiliary switch in [1], [2], [11]-[13] needs a floating gate drive because the source terminal of the auxiliary switch is not in common with the input voltage source ground, thereby resulting in complexity of the gate drive circuit. The other ZVT technique is applied in [14]-[18] where coupled inductors are used. In [14]-[17], the auxiliary inductor is coupled with the main converter inductor, and the leakage inductor is used as the resonance inductor. Thus, all converter inductors are implemented on a single core, thereby resulting in significant reduction of the converter size. However, using a coupled inductor in [14]-[17] results in increased auxiliary switch voltage stress. In [17], the auxiliary switch is also turned off under a hard switching condition. In [18], a separate core is needed for the coupled inductor, thereby resulting in too many auxiliary elements. The auxiliary switch in [14]-[18] needs floating gate drive circuit.

In this study, a new family of nonisolated synchronous converter is introduced. In the proposed converters, the advantages of the ZVT converters of [13]-[17] are achieved. The SR diode reverse recovery losses are completely eliminated by applying the idea of [13], and soft switching condition is provided for the whole converter operating region without any extra voltage and current stresses on the main and SR switches. In this study, the analytical work is conducted to design properly the converter for the whole converter operation region. The auxiliary inductor is also coupled with the main converter inductor. All the converter inductors are also implemented on a single core with the leakage inductor as the resonance inductor. In addition to these advantages, the voltage stress of the auxiliary switches, compared with the previously proposed ZVT converters, is reduced significantly, and the auxiliary switches do not need the floating gate drive circuit. Thus, low-voltage power switches with ultralow on-resistance ($R_{D(on)}$) are used. The turn-on capacitive losses of the auxiliary switch are also reduced.

The analysis and operation of the proposed ZVT synchronous buck converter are described in Section II. The design considerations and a design example are presented in Sections III and IV, respectively. The experimental results are shown in Section V to confirm the theoretical analysis. Finally, the auxiliary circuit is developed for the other nonisolated synchronous converters, as discussed in Section VI.

II. Circuit Description and Operation

The proposed ZVT synchronous buck converter is shown in Fig. 1(a). The main converter is composed of main switch S_m, SR switch S_{SR}, output filter inductor L_1 and output capacitor filter C. The auxiliary circuit is composed of auxiliary switch S_a, rectifying diode D_a, and inductor L_2, which is coupled with the main inductor L_1. The turn ratio of the coupled inductors L_1 and L_2 is n ($L_2 = n^2 L_1$). The auxiliary switch source terminal agrees with the input voltage source ground. Hence, the auxiliary circuit does not need the floating gate drive. Fig. 1(b) illustrates that the coupled inductors can be modeled as a combination of an ideal transformer with a corresponding turn ratio (n), magnetizing inductance (L_M), and a leakage inductance (L_{lk}). The magnetizing inductances L_M and L_{lk} are employed as the converter main inductor and resonance inductor, respectively. The converter has eight operating modes in a switching cycle. The equivalent circuits of each operating mode are shown in Fig. 2, where the current arrows refer to the actual direction of the current. The key waveforms of the converter are illustrated in Fig. 3. All elements are assumed ideal to simplify the converter analysis. The magnetizing inductor current and input voltage are also assumed constant in a switching cycle and equal to I_{LM} and V_{in}, respectively.

Prior to the first mode, S_{SR} is presumably conducting the magnetizing inductor current (I_{LM}), and all other semiconductor devices are off. No current presumably flows in the windings of the ideal transformer in the model. The voltages across the primary (V_p) and secondary (V_s) windings are V_o and nV_o, respectively.

Mode 1: ($t_0 - t_1$) This mode starts by turning the auxiliary switch S_a on. Thus, the secondary winding voltage of the ideal transformer (nV_o) placed across L_{lk} and S_a current starts

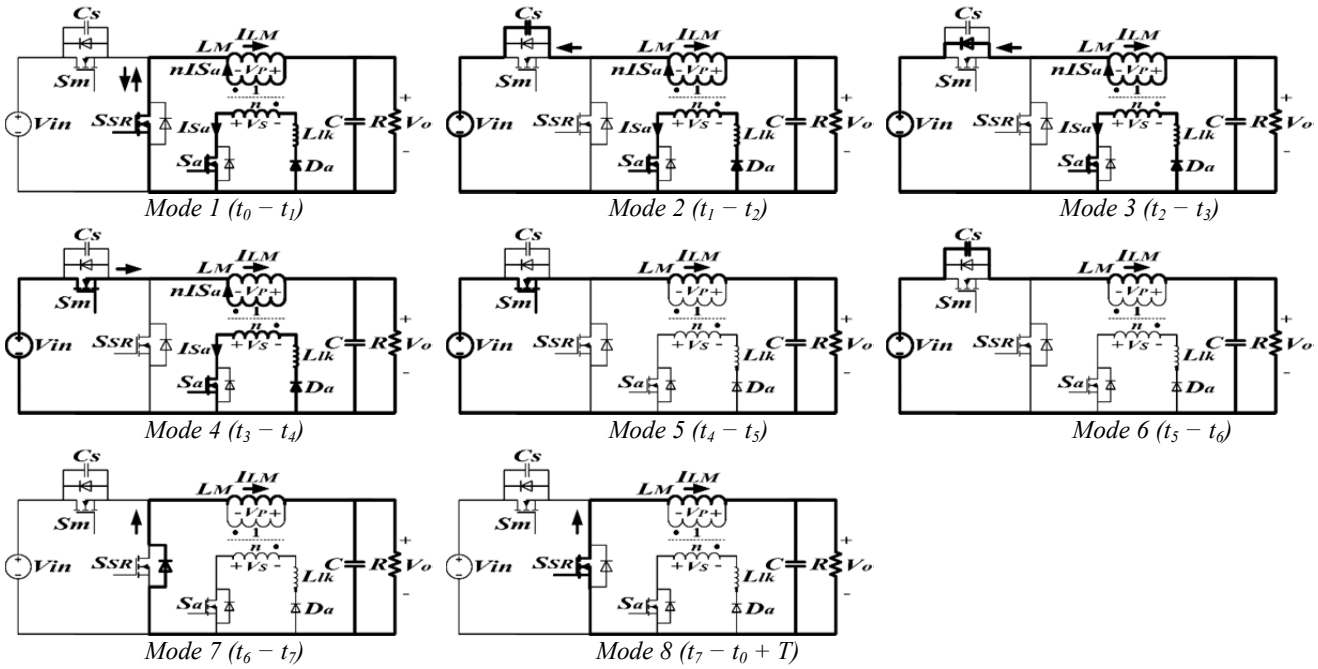


Fig. 2. Equivalent circuit for each operating mode of the proposed converter.

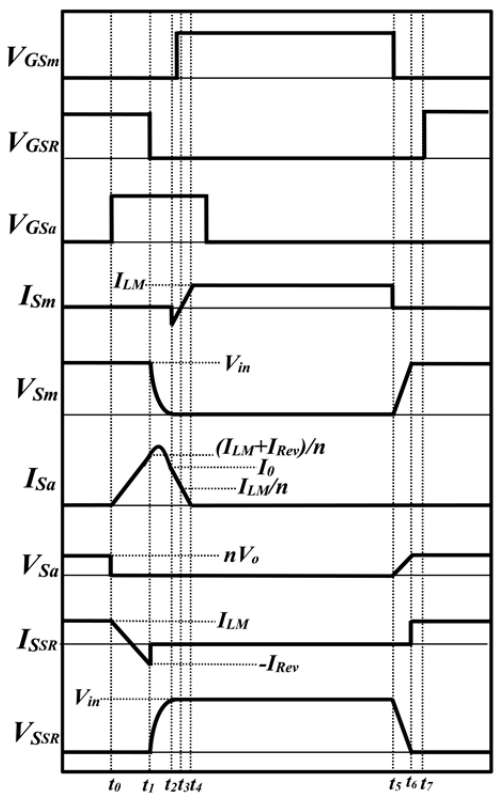


Fig. 3. Converter theoretical waveforms.

to increase linearly as follows:

$$I_{Sa} = \frac{nV_o}{L_{lk}}(t - t_0). \quad (1)$$

Given the series inductor L_{lk}, S_a is turned on under ZCS condition. During this mode, I_{Sa} enters the dotted terminal of the ideal transformer secondary windings. Thus, nI_{Sa} flows out of the dotted terminal of the primary side. Therefore, S_{SR} current equation is

$$I_{S_{SR}} = I_{LM} - \frac{n^2 V_o}{L_{lk}}(t - t_0). \quad (2)$$

In this mode, S_{SR} current decreases from I_{LM} to zero and then increases in the opposite direction for a short time through the S_{SR}. At the end of this mode, S_{SR} current is defined as $-I_{Rev}$. Consequently, S_a current is $(I_{LM} + I_{Rev}) / n$. The S_{SR} current is reduced through the SR switch S_{SR}. Hence, the reverse recovery of the S_{SR} body diode is prevented from occurring, and the diode reverse recovery losses are eliminated completely. The duration of this mode is

$$t_1 - t_0 = \frac{(I_{LM} + I_{\mathrm{Re}v})L_{lk}}{n^2 V_o}. \quad (3)$$

The value of I_{Rev} is effective in providing ZVS condition when the converter operates in operating duty cycles below 0.5. This point is discussed in the design consideration section.

Mode 2: ($t_1 - t_2$) In this mode, the SR switch S_{SR} is turned off, and a resonance starts between L_{lk} and C_S. Given the capacitor C_S, S_{SR} is turned off under ZVS condition. During this resonance, C_S discharges from V_{in} to zero to provide ZVS condition for S_m at turn-on. S_m voltage is

$$V_{Sm} = (V_{in} - V_o) + V_o \cos(\omega_0(t - t_1)) - I_{\mathrm{Re}v} Z_0 \sin(\omega_0(t - t_1)), \quad (4)$$

where

$$\omega_0 = \frac{n}{\sqrt{L_{lk} C_S}} \qquad Z_0 = \frac{\sqrt{\frac{L_{lk}}{C_S}}}{n}. \quad (5)$$

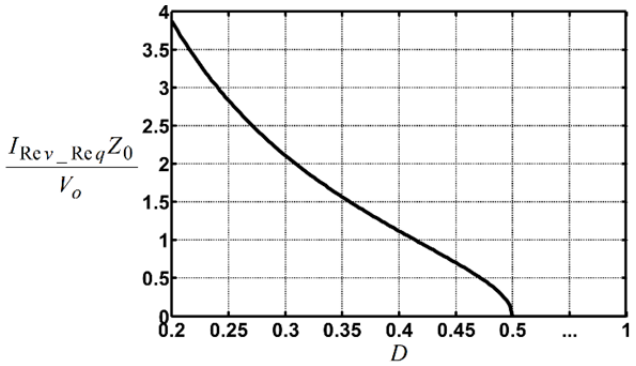


Fig. 4. Normalized value of I_{Rev_Req} versus D.

At the end of this mode, S_a current is I_0.

Mode 3: ($t_2 - t_3$) At t_2, the S_m body diode starts to conduct. Thus, the main switch S_m can be turned on under ZVS condition. In this mode, the voltage across the primary and secondary windings of the ideal transformer in the model are changed to $-(V_{in} - V_o)$ and $-n(V_{in} - V_o)$, respectively. Therefore, the negative voltage placed across L_{lk} and S_a currents starts to reduce linearly as follows:

$$I_{Sa} = I_0 - \frac{n(V_{in} - V_o)}{L_{lk}}(t - t_2). \quad (6)$$

Consequently, S_m current is

$$I_{Sm} = I_{LM} - nI_0 + \frac{n^2(V_{in} - V_o)}{L_{lk}}(t - t_2). \quad (7)$$

At the end of this mode, I_{Sm} and I_{Sa} currents reach zero and I_{LM}/n, respectively. The body diode of S_m is turned off under ZCS condition. The duration of this interval is

$$t_3 - t_2 = \frac{(nI_0 - I_{LM})L_{lk}}{n^2(V_{in} - V_o)}. \quad (8)$$

Mode 4: ($t_3 - t_4$) In this mode, S_a current reduces from I_{LM}/n to zero, and the rectifying diode D_a prevents the S_a current to follow in the opposite direction. Thus, the auxiliary switch of S_a can be turned off under ZCS condition. I_{Sm} increases from zero to I_{LM}. S_a and S_m current equations are as follows:

$$I_{Sa} = \frac{I_{LM}}{n} - \frac{n(V_{in} - V_o)}{L_{lk}}(t - t_3), \quad (9)$$

$$I_{Sm} = \frac{n^2(V_{in} - V_o)}{L_{lk}}(t - t_3). \quad (10)$$

The duration of this mode is

$$t_4 - t_3 = \frac{I_{LM}L_{lk}}{n^2(V_{in} - V_o)}. \quad (11)$$

Mode 5: ($t_4 - t_5$) In this mode, no current exists in the auxiliary circuit, and I_{LM} flows through the S_m. This mode is identical to a conventional PWM buck converter when the main switch is on and the main converter inductor (L_M) stores energy.

Mode 6: ($t_5 - t_6$) At t_5, the main switch S_m is turned off under ZVS condition because of the capacitor C_S. C_S is charged linearly by the magnetizing inductor current I_{LM} through turning S_m off. At the end of this mode, Cs is charged to V_{in}, and the S_{SR} body diode begins to conduct.

Mode 7: ($t_6 - t_7$) This operating mode is identical to a conventional PWM buck converter when the main switch is off and the stored energy in L_M flows to the output through the S_{SR} body diode.

Mode 8: ($t_7 - t_0 + T$) The SR switch S_{SR} can be turned on under ZVS condition by conducting the S_{SR} body diode. Thus, I_{LM} flows to the output through S_{SR}.

III. Design Considerations

The main synchronous buck converter is designed similar to a regular PWM buck converter. In the proposed converter, L_M is employed as the converter filter inductor. Thus, it is designed as the inductor filter in a conventional PWM buck converter.

As discussed in the previous section, in mode 1, the current of the SR switch is reduced to zero by the auxiliary circuit to eliminate the rectifying diode reverse recovery losses. This current also flows in the opposite direction for a short period. The final opposite current value of the SR switch is defined as I_{Rev}. Thus, reverse recovery losses are eliminated completely if I_{Rev} is equal or greater than zero. By contrast, the main switch voltage must be zero at the end of the operating mode 2 to achieve the ZVS condition for the main switches at turn-on. Thus, the following equation should be satisfied from Equ. (4):

$$(V_{in} - V_o) + V_o\cos(\omega_0(t - t_1)) - I_{Rev}Z_0\sin(\omega_0(t - t_1)) = 0. \quad (12)$$

In the buck converter, $V_o = V_{in}D$. Thus, Equation (12) is written as follows:

$$V_o\left(\frac{1}{D} - 1\right) + V_o\cos(\omega_0(t_2 - t_1)) - I_{Rev}Z_0\sin(\omega_0(t_2 - t_1)) = 0. \quad (13)$$

Equ. (13) shows that the value of I_{Rev} is effective in ZVS condition. The required value of I_{Rev} to achieve ZVS condition is defined as I_{Rev_Req}. According to Equ. (13), the normalized value of I_{Rev_Req} versus D is plotted in Fig. 4 [7]. Consequently, the ZVS condition of the main switch at turn-on and the elimination of the rectifying diode reverse recovery are provided simultaneously if the value of I_{Rev} is greater than I_{Rev_Req}. Thus, the following soft switching condition can be formulated:

$$I_{Rev} > I_{Rev\_Req}. \quad (14)$$

I_{Rev}, which satisfies the preceding condition, must be provided. I_{Rev} value is obtained from Equ. (3) as follows:

$$I_{Rev} = -I_{LM} + \frac{(t_1 - t_0)n^2V_o}{L_{lk}}, \quad (15)$$

where $(t_1 - t_0)$ is mode 1 duration time. Given that this time is the duration time between the auxiliary switch turn-on and the SR switch turn-off, adjusting this duration is feasible.

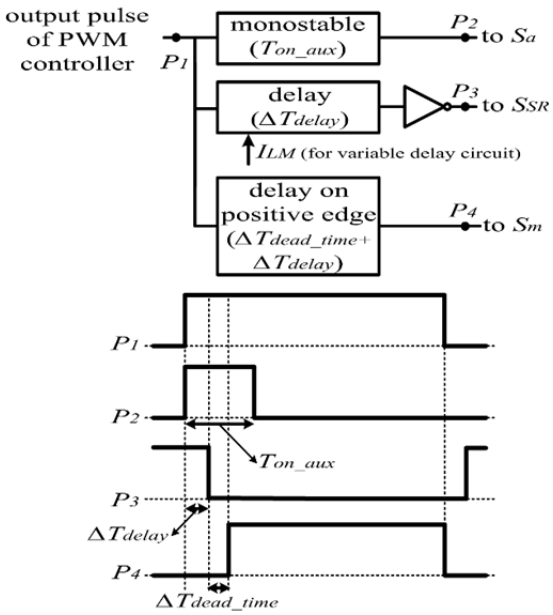


Fig. 5. Schematic of the interface circuit to adapt the output pulse of the PWM controller to the proposed converter.

Thus, the following soft switching condition is achieved from Equs. (14) and (15):

$$\Delta T_{delay} = (t_1 - t_0) > \frac{(I_{LM} + I_{\mathrm{Rev\_Req}})L_{lk}}{n^2 V_o}, \quad (16)$$

where ΔT_{delay} is the duration time between the auxiliary switch turn-on and the SR switch turn-off. Consequently, the ZVS condition of the main switch at turn-on and the elimination of the rectifying diode reverse recovery are provided by tuning ΔT_{delay} as formulated in Equ. (16). In Equ. (16), I_{Rev_Req} should be extracted for the minimum value of the duty cycle. Equ. (16) indicates that ΔT_{delay} value depends on the value of the main inductor current I_{LM}. In this case, a feedback of the converter current value and a variable delay circuit are essential. In a conventional PWM current mode controller, the current feedback of the converter current value is available. However, the value of ΔT_{delay} can be adjusted for the full load condition when the value of I_{LM} is at the maximum value to avoid complexity. Thus, the current feedback is not necessary, and a simple fixed value delay circuit can be applied. Additional circulating current at light loads can be obtained by applying the fixed value of ΔT_{delay}.

The turn-on period of the auxiliary switch T_{on_aux} should be sufficient, in which the auxiliary switch current can be reduced to zero, to achieve the ZCS condition for the auxiliary switch at turn-off. Thus, T_{on_aux} should be greater than the duration time of the operating modes 1, 2, 3, and 4. In this case, the duration time of mode 2 is estimated at one-quarter of the resonance period time, and the auxiliary switch current during mode 2 is assumed constant. Thus, the auxiliary switch turn-on period T_{on_aux} is obtained from Equs. (3), (5), (8), and (11) as follows:

$$T_{on\_aux} > \frac{(I_{LM} + I_{\mathrm{Rev\_Req}})L_{lk}}{n^2}\left(\frac{1}{V_o} + \frac{1}{V_{in} - V_o}\right) + \frac{\pi}{2\omega_0}. \quad (17)$$

Hence, the ZCS condition of the auxiliary switch at turn-off is provided by tuning T_{on_aux} as formulated in Equ. (17). I_{LM} and V_{in} should be designed for the full load and minimum values of the input voltage, respectively, to achieve ZCS condition at the worst case operating condition. I_{Rev_Req} should be extracted for the minimum value of the duty cycle, and ω_0 is obtained from Equ. (5).

Similar to other DC–DC PWM converters, the proposed converter employs the conventional controllers. The schematic of the interface circuit is presented in Fig. 5, where ΔT_{delay} and T_{on_aux} are obtained from

Equs. (16) and (17), to adapt the output pulse of a conventional PWM controller to the proposed converter, and ΔT_{dead_time} is the dead time between the conduction time of S_m and S_{SR} when the snubber capacitor is discharged. This time is set to the following one-quarter resonance period to guarantee that the main switch turns on when the snubber capacitor is discharged completely:

$$\Delta T_{dead\_time} = \frac{\pi}{2\omega_0}. \quad (18)$$

The capacitor C_S provides ZVS condition for the main and SR switches at turn-off instant. Therefore, its value can be selected similar to any snubber capacitor as follows [19]:

$$C_S > C_{S\_\min} = \frac{I_{sw} t_f}{2V_{sw}}, \quad (19)$$

where t_f is the switch current fall time, I_{SW} is the switch current before turn-off, and V_{SW} is the switch voltage after turn-off. Similarly, the inductor L_{lk} provides ZCS condition for the auxiliary switch at turn-on instant. Its value can be selected according to [19] as follows:

$$L_{lk} > L_{lk\_\min} = \frac{V_{sw} t_r}{I_{sw}}, \quad (20)$$

where t_r is the switch current rise time, I_{SW} is the switch current after turn-on, and V_{SW} is the switch voltage before turn-on. The obtained snubber values are the minimum values. In practice, the snubber values should be larger than the minimum values to guarantee soft switching. However, obtaining a large L_{lk} results in long transient modes, as observed in Equ. (17). Thus, conduction losses and limitations exist in duty cycle. According to Equ. (17), the following condition should be satisfied

$$\frac{(I_{LM} + I_{\mathrm{Rev\_Req}})L_{lk}}{n^2}\left(\frac{1}{V_o} + \frac{1}{V_{in} - V_o}\right) + \frac{\pi}{2\omega_0} < 0.2T, \quad (21)$$

where T is the converter switching period.

Finally, the values of n must be selected. The voltage stress on the auxiliary switch is equal to nV_o. Thus, a small selection of n results in small values of auxiliary switches voltage stress. However, a small value of n reduces L_{lk} value, which serves as the snubber inductor for the auxiliary switches. The

value of n can be selected in the range of 1/3 to 1/2.

IV. Design Example

A design example for the proposed converter is presented in this section. The design requirements are defined as follows:

- Output power (P) = 180 W;
- Input voltage (V_{in}) = 80 V;
- Output voltage (V_o) = 30 V;
- Operating frequency = 100 kHz.

A. Converter Component Selection

On the basis of the converter input data, the operating duty cycle (D) and the magnetizing inductor current (I_{LM}) are obtained as follows:

$$D = \frac{V_0}{V_{in}} = \frac{30V}{80V} = 0.375 ,$$

$$I_{LM} = \frac{P}{V_o} = \frac{180W}{30V} = 6A .$$

ΔI_{LM} is selected as 2 A to ensure that the converter operates in continuous conduction mode at load variation above 20% of full load. Thus, the main converter inductor (L_M) is designed as follows [19]:

$$L_M > \frac{V_o(1-D)}{\Delta I_{LM} f} = \frac{30V*(1-0.375)}{2A*100kHz} = 93.75\mu H .$$

The value of L_M is selected as

$$L_M = 100\mu H .$$

As discussed in the previous section, the value n is selected as

$$n = \frac{1}{2} .$$

Thus, the inductance of the secondary winding is obtained as

$$L_2 = n^2 L_M = (\frac{1}{2})^2 *100\mu H = 25\mu H .$$

For the main and SR switches, IRF540 (V_{DS}= 100 V, R_D(on) = 44 mΩ, t_f = 35 ns) is used. According to the converter input data and theoretical analysis, the auxiliary switch voltage stress is approximately 15 V (nV_o). For the auxiliary switch (S_a), IRF1404 (V_{DS} = 40 V, R_D(on) = 4 mΩ, t_r = 190 ns) is applied and BYV32 is used for the rectifying diode (D_a).
The values of C_S and L_{lk} are designed from Equs. (19) and (20) as

$$C_S > C_{S\_\min} = \frac{6A*35ns}{2*80V} = 1.31nF ,$$

$$L_{lk} > L_{lk\_\min} = \frac{15V*190ns}{12A} = 0.24\mu H .$$

The value of C_S is selected as

$$C_S = 10nF .$$

The approximate value of L_{lk} is obtained as

$$L_{lk} = 0.75\mu H .$$

B. Auxiliary Switch Timing Design

On the basis of the selected components, the values of Z_0 and ω_0 are obtained from Equ. (5) as

$$Z_0 = \frac{\sqrt{\frac{0.75\mu H}{10nF}}}{\frac{1}{2}} = 17.3\Omega ,$$

$$\omega_0 = \frac{\frac{1}{2}}{\sqrt{0.75\mu H * 10nF}} = 5.77*10^6 \frac{rad}{s} .$$

According to the discussions in the previous section and from Fig. 4, for D = 0.375, the normalized value of I_{Rev_Req} is

$$\frac{I_{Rev\_Req} Z_0}{V_o} = 1.33 .$$

Hence, the value of I_{Rev_Req} is

$$I_{Rev\_Req} = \frac{30V*1.33}{17.3\Omega} = 2.3A .$$

Thus, the values of ΔT_{delay} , T_{on_aux}, and ΔT_{dead_time} are obtained from Equs. (16) to (18) as

$$\Delta T_{delay} > \frac{(6A+2.3A)*0.75\mu H}{(\frac{1}{2})^2 *30V} = 0.83\mu s ,$$

$$T_{on\_aux} > [\frac{(6A+2.3A)*0.75\mu H}{(\frac{1}{2})^2}(\frac{1}{30V}+\frac{1}{80V-30V}) + \frac{\pi}{2*5.77*10^6 rad/s}] = 1.6\mu s ,$$

$$\Delta T_{dead\_time} = \frac{\pi}{2*5.77*10^6 rad/s} = 0.27\mu s .$$

These duration times are set at

$$\Delta T_{delay} = 1\mu s, T_{on\_aux} = 2.5\mu s, T_{dead\_time} = 0.3\mu s .$$

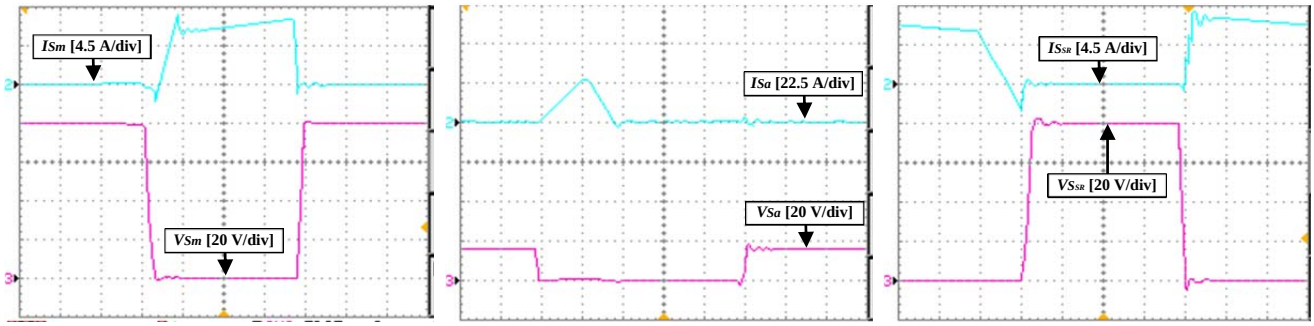
As discussed in the previous section, the fixed value of ΔT_{delay} = 1 μs is applied to avoid complexity. Thus, the auxiliary circuit does not need the current feedback, and a simple fixed value delay circuit can be applied. On the basis of the selected component values, the condition of Equ. (21) is satisfied as follows:

$$1.6\mu s < 0.2*10\mu s .$$

Thus, the duration time of the transient modes is approximately 1.6 μs, which is lower than 20% of the converter switching period.

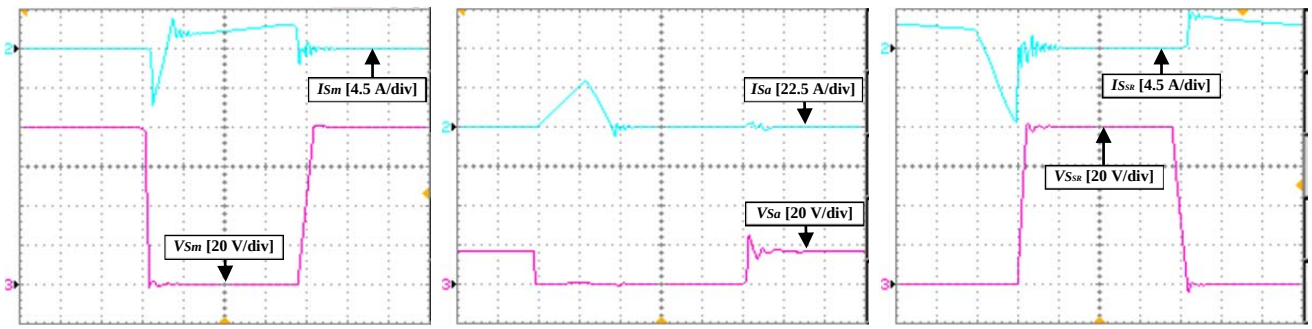
V. Experimental Results

A prototype of the proposed converter is implemented for the input data and the designed components presented in the previous section to verify the principle of operation. As discussed in the previous section, the auxiliary switch voltage stress is approximately 15 V (nV_o), which is approximately



(a) (b) (c)

Fig. 6. Experimental waveforms at full load (180 W): (top waveform) current and (bottom waveform) voltage of the (a) main switch S_m, (b) auxiliary switch S_a, and (c) SR switch S_{SR} (time scale is 1 μs/div.)



(a) (b) (c)

Fig. 7. Experimental waveforms at light load (35 W): (top waveform) current and (bottom waveform) voltage of the (a) main switch S_m, (b) auxiliary switch S_a, and (c) SR switch S_{SR} (time scale is 1 μs/div.)

20% of the main switch voltage stress. This point provides the use of a low-voltage power switch with low $R_{D(On)}$ for the auxiliary switch to reduce its conduction and capacitance turn-on losses. In the previous ZVT converters, the voltage stresses of the auxiliary switches compared with those of the main switch are approximately 120% in [14]-[16], 90% in [17], and 40% in [7], [13].

The experimental results at full load (180 W) and light load (35 W) are shown in Figs. 6 and 7, respectively. Before the main switch turn-on instant, the snubber capacitor is discharged completely. The ZVS condition at full load and light load is also provided for the main switch turn-on instant. This condition is achieved, given that ZVS at full load condition is the worst case scenario. The snubber capacitor provides ZVS condition for both main and SR switches at turn-off. No additional voltage stress exists on the main and SR switches voltage waveforms. The ZCS condition of the auxiliary switch is also achieved for both turn-on and turn-off instants.

The power loss at each component of the proposed converter in comparison to the regular hard switching converter and previously ZVT converters is presented in Table I to evaluate the power losses. The losses of all converters are estimated for a buck converter with the input data presented in the design example section. The average and root mean square values are extracted with the simulation results. Compared with the previous ZVT converters in [7], [17], [14]-[16], the proposed converter benefits from

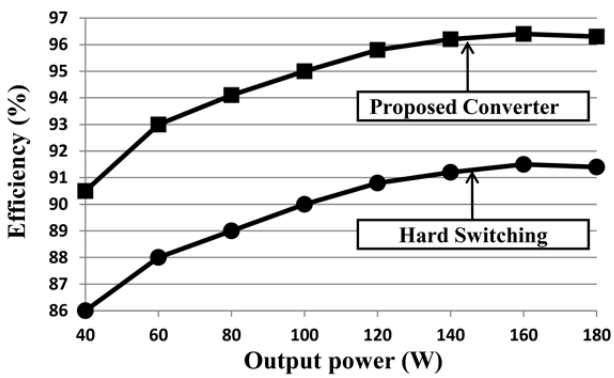


Fig. 8. Efficiency comparison of the proposed soft switching converter with its hard switching counterpart.

efficiency. In [7], a high-voltage switch with slow body diode should be applied as the SR switch, which increases the conduction losses, to achieve ZVS condition for the duty cycles below 0.5. In [17], hard switching of the auxiliary switch increases the losses. In [14]-[16], a power switch with high $R_{D(on)}$, which increases the conduction losses, should be applied because of the high-voltage stress of the auxiliary switch. Finally, unlike the converter in [13], the efficiency of the proposed converter is reduced by approximately 0.2%. However, compared with the converter in [13], the proposed converter benefits from a reduced volume caused by the implementation of all the converter inductors on a single core. Unlike the converters in [7], [13] and that of ZVT converters with coupled inductors in [17], [14]-[16], the gate drive

TABLE I

COMPARISON OF LOSSES IN THE PROPOSED CONVERTER, REGULAR HARD SWITCHING CONVERTER, AND PREVIOUS ZVT CONVERTERS

	Type of losses	Regular hard-switching converter	ZVT converter proposed in [7]	ZVT converter with coupled inductors proposed in [17]	ZVT converter with coupled inductors proposed in [14]-[16]	ZVT converter proposed in [13]	Proposed ZVT converter with coupled inductors
Auxiliary circuit losses	Auxiliary switch (S_a) conduction losses $R_{D(on)\_Sa}.(I_{rms\_Sa})^2$ [22]	N.A	0.3 (W)	0.7 (W)	1.4 (W)	0.3 (W)	0.1 W
	Auxiliary switch (S_a) turn-off losses $\frac{1}{2}.V_{Sa}.I_{Sa}.t_f.f$ [21]	N.A	Zero due to ZCS	1.8 (W)	Zero due to ZCS	Zero due to ZCS	Zero due to ZCS
	Auxiliary switch (S_a) turn-on capacitance losses $\frac{1}{2}.C_{oss\_Sa}.(V_{Sa})^2.f$ [21]	N.A	0.1 (W)	0.2 (W)	0.4 (W)	0.1 (W)	Almost zero
	Auxiliary diode (D_a) conduction losses $V_{F\_Da}.I_{avg\_Da}$ [21]	N.A	0.8 (W)	0.5 (W)	0.9 (W)	0.8 (W)	1.6 (W)
Main converter losses	Main switch (S_m) Switching Losses $\frac{1}{2}.V_{in}.I_o.(t_f+t_r).f$ [22]	1.7 (W)	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS
	Main switch (S_m) turn-on capacitance losses $\frac{1}{2}.C_{oss\_Sa}.(V_{in})^2.f$ [21]	0.2 (W)	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS
	SR switch (S_{SR}) diode reverse recovery losses $V_{in}.(Q_{rr}+t_{rr}I_o).f$ [20]	9.6 (W)	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS	Zero due to ZVS
	S_m and S_{SR} conduction losses $R_{D(on)\_Sm}.(I_{rms\_Sm})^2 + R_{D(on)\_S_{SR}}.(I_{rms\_S_{SR}})^2$ [22]	1.6 (W)	4 (W)	1.6 (W)	1.6 (W)	1.6 (W)	1.6 (W)
	Other losses (losses of gate drive circuit, control circuit, …)	2 (W)	2 (W)	2 (W)	2 (W)	2 (W)	2 (W)
	Total auxiliary circuit losses	N.A	1.2 (W)	3.1 (W)	2.7 (W)	1.2 (W)	1.7 (W)
	Total converter losses	15.1 (W)	7.2 (W)	6.7 (W)	6.3 (W)	4.8 (W)	5.3 (W)
	Total converter Efficiency	91.6%	96%	96.2%	96.5 %	97.3%	97.1%

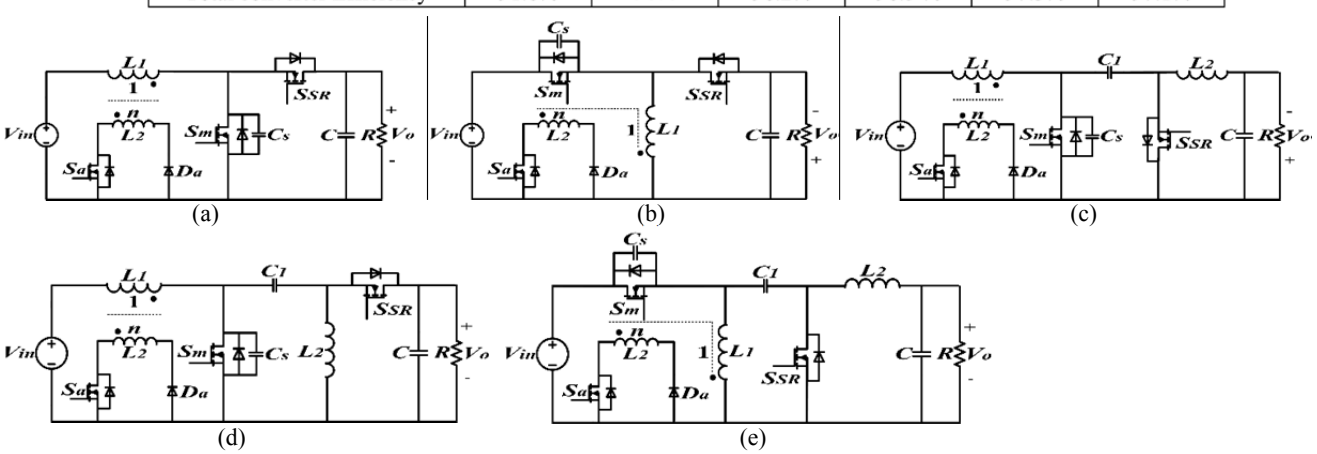


Fig. 9. Other family members of the proposed converter: (a) boost, (b) buck/boost, (c) cuk, (d) SEPIC, and (e) Zeta.

circuit of the proposed converter is simple because the auxiliary switch does not need the floating gate drive circuit.

The converter efficiency curve is shown in Fig. 8. The efficiency of hard switching is for a regular synchronous buck converter with the same parameters with IRF540 as their switches.

VI. Other ZVT Synchronous Converters with Coupled Inductors

Similar to the synchronous buck, this ZVT technique can be applied to other nonisolated synchronous converters to improve their efficiency, as shown in Fig. 9. In all topology variations, the auxiliary switch source terminal agrees with the input voltage source ground. For other topologies, the theoretical operating modes are similar to the operation of the synchronous buck converter explained in Section II. Thus, further explanation is not given.

VII. Conclusion

A family of ZVT synchronous converters is introduced. Theoretical analysis for a synchronous buck converter is presented in detail. The theoretical analysis shows that the ZVS condition of the main switch at turn-on and the elimination of the rectifying diode reverse recovery are provided by tuning the duration time between the auxiliary switch turn-on and the synchronous rectifier switch turn-off as formulated. The ZCS condition for the auxiliary switches at both turn-on and turn-off instants is achieved. Consequently, high efficiency over a wide operating range is obtained. In addition, the auxiliary switches benefit from low-voltage stress (nV_o), and floating gate drive circuit is not necessary. To validate the theoretical analysis, a 180 W, 80 V to 30 V prototype of the converter at 100 kHz is implemented. The auxiliary voltage stress is approximately 20% of the main switch voltage stress. Other family members of the proposed converters are presented.

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