JPE 16-1-39

http://dx.doi.org/10.6113/JPE.2016.16.1.388
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Voltage Source Inverter Drive Using Error-compensated Pulse Width Modulation

Keng-Yuan Chen†, Jwu-Sheng Hu*, and Jau-Nan Lin*

†Dept. of Electrical Eng., Yuan-Ze University, Chung-Li, Taiwan
*Dept. of Electrical and Control Eng., National Chiao Tung University, Hsin-Chu, Taiwan

Abstract

An error-compensated pulse width modulator (ECPWM) is proposed to improve the baseband harmonic performance and the switching loss of voltage source inverters (VSIs). Selecting between harmonic distortion and switching loss is a design tradeoff in the conventional space vector pulse width modulation. In this work, an accumulated difference in produced and desired phase voltages is considered to adjust the reference signal. This mechanism can compensate for the voltage error in the previous carrier period. With error compensation every half-carrier period, the proposed ECPWM allows one-half reduction in carrier frequency without scarifying baseband harmonic distortion. The proposed modulator is applied to a three-phase VSI with R–L load and a motor-speed-control system for experiments. The measured efficiency and operating temperature of switches confirm the effectiveness of the proposed scheme.

Key words: Digital signal, Motor drive, Pulse-width modulation (PWM), Space-vector PWM, Voltage-source inverter

I. INTRODUCTION

Voltage source inverters (VSIs) are widely utilized in driving variable-speed alternating current motors. Sine-triangle pulse width modulation (PWM), space vector PWM (SVPWM), and discontinuous PWM (DPWM) are common real-time approaches to generate the driving signals for VSIs. Extensive discussions of these PWMs indicate that these PWMs can be unified by shifting efficient conducting time [1], changing modulation signals [2], or using different zero-vector distributions [3]. Therefore, a simple carrier-based implementation architecture can be used to have all the advantages of modulators, that is, simple implementation, extended linear modulation index, and 33% of switching number reduction.

Linear modulation range, implementation simplicity, power efficiency, and harmonic distortion are important factors in the control of VSIs. The tradeoff between switching loss and harmonic distortion remains a critical design issue. Several PWM techniques are discussed to reduce distortion given a fixed switching frequency [4]–[10]. For example, the extended-state observer-based control scheme [9] is proposed to reduce current harmonics. The interleaved PWM is suggested to reduce output current ripple [10]. The filtered PWM [6] is shown to attenuate baseband harmonics, especially for small modulation index reference. The novel selective harmonic elimination-based multi-module PWM [5], the multi-rate repetitive control PWM [7], the three-stage hybrid modulator [8], and the immune algorithm-based SVPWM [4] are applied to reduce voltage harmonic distortion.

A different effective time placement is used in a dual-inverter-fed open-end winding induction motor [11] to limit switching power loss. A modified finite-step predictive torque control is proposed in [12] to improve inverter loss by reducing switching frequency and calculation time. In [13], an adaptive feedback controller is developed to produce flux reference with optimized energy consumption of the induction motor. The modified phase disposition PWM is applied to a flying capacitor inverter for voltage balancing and efficiency improving [14].

A novel inverter topology is proposed to reduce switching loss and harmonic distortion [15]. The synchronized DPWM [16] is used in the application of a high-power, three-level VSI with lagging loads. Several novel DPWMs with double

Manuscript received Jun. 2, 2015; accepted Jul. 15, 2015
Recommended for publication by Associate Editor Jee-Hoon Jung.
†Corresponding Author: bettery33@gmail.com
Tel: +886-5-4638800, Fax: +886-3-4639355, Yuan-Ze University
*Dept. of Electrical and Control Eng., National Chiao Tung University, Taiwan

injections are analyzed in [17] to obtain minimum current harmonic or minimum switching loss. A feedback quantization modulator [18] is applied to a permanent-magnet synchronous motor (PMSM) drive system to show a 33% reduction in switching number in contrast to SVPWM in [19]. The minimum-switching-loss PWM proposed in [20] can reduce up to 36% of switching loss. However, the result in [17] shows that different switching strategies must be applied to achieve minimum distortion or minimum switching loss. The methods in [18], [20] involve complicated calculation to produce switching signals that will influence the applicability of modulators. In this work, a simple approach based on error compensation and asymmetric pulse width production is suggested to achieve 50% of switching number reduction without sacrificing baseband harmonic distortion.

Several different asymmetrical switching signal production methods have been proposed recently. For example, [21] produces random pulse-position-switching commands by adopting varying rising/falling slopes of triangular wave to reduce the carrier harmonic and acoustic noise of a motor drive. The asymmetrical pulse gives an additional degree of freedom when selective harmonic elimination [22] or bee colony optimization [23] is used. All the asymmetrical PWMs in [21]–[23] focus on declining harmonics only.

In this work, both baseband harmonic distortion and switching loss are considered. The simplest way to reduce switching loss is to reduce switching number, that is, to reduce carrier frequency. However, baseband harmonic distortion increases with reduced carrier frequency when the conventional SVPWM is applied. This study proposes an error-compensated pulse width modulator (ECPWM). Different references are applied for the rising and falling edges of the carrier by voltage error compensation at a rate of twice of the carrier frequency. This mechanism can greatly improve baseband harmonics and achieves a comparable performance by using only half of the switching frequency in contrast to SVPWM. Therefore, the ECPWM reduces switching loss by using a low carrier frequency without sacrificing baseband harmonic distortion.

In the simulation, a three-phase VSI with R–L load is built in PSIM. Comparisons of the phase voltages and the phase currents produced by SVPWM and the proposed modulator are shown. An experimental platform based on field-oriented control (FOC) is built to drive a PMSM to verify the reliability, applicability, and effectiveness of the proposed modulator. The switching number and harmonic distortion of the produced phase currents are illustrated. Closed-loop performances, such as motor speed and output torque, are also measured. Under the condition that the switching number of the proposed modulator is half that of SVPWM, the results indicate that the system efficiency and the operating temperature of power metal oxide semiconductor field-effect transistors (MOSFETs) are improved.

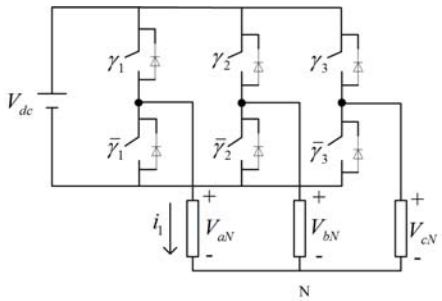


Fig. 1. Three-phase VSI topology.

The remainder of this paper is organized as follows: Section II provides the mathematical formulation of the proposed modulator and the mechanism of reference adjustment. Section II shows the system analysis. Sections III and IV present the simulations and experiments, respectively. Finally, Section V concludes this paper.

II. ECPWM

A. Objectives of Modulation

For the three-phase VSI system depicted in Fig. 1, the objective is to decide the on/off status of six switches to produce desired phase voltage on the load, $[V_{aN} \quad V_{bN} \quad V_{cN}]^T$. If the on (off) status of the upper switch is denoted as +1 (0), then the switching state of the three-phase VSI system can be represented by a switching vector, $[s_1 \quad s_2 \quad s_3]^T$, which has elements that belong to the set $\{0, 1\}$. Therefore, the instantaneous phase voltage (normalized to V_{dc}) can be obtained from Equ. (1).

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ s_3 \end{bmatrix} \tag{1}$$

By considering the duty ratios for each phase lag, we express the normalized mean voltage produced within each carrier cycle as Equ. (2) according to Equ. (1).

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} \overset{\Delta}{=} \mathbf{S}_c \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix}, \tag{2}$$

where $\alpha_1, \alpha_2, \alpha_3 \in [0 \quad 1]$ are the duty ratios for phase lags. Under analog implementation, the values of $\alpha_1, \alpha_2, \alpha_3$ can be selected arbitrarily within the range $[0 \quad 1]$. However, for the digital implementation with carrier frequency f_c and pulse bit resolution b-bit, the minimum pulse width that can be produced is $1/(f_c \times 2^b)$ s, and a master clock frequency of $(f_c \times 2^b)$ Hz is required. The produced duty ratios are limited to be integer multiples of 2^{-b}, that is, they must belong to the set $\{0, 1/2^b, 2/2^b, \cdots, (2^b-1)/2^b, 1\}$. Thus, voltage deviation

is unavoidable with a finite pulse width resolution. The voltage error, although small within each carrier period, will accumulate and induce considerable current harmonics [24]. Therefore, the objective of the switching signal generation is to decide the duty ratios $\alpha_1, \alpha_2, \alpha_3 \in [0 \quad 1]$ such that the accumulated voltage error is compensated for within every carrier period, that is, minimizing the difference in the desired and the produced voltage signals.

B. Error Compensation

For future reference, the input three-phase voltages, denoted as $\mathbf{r}(k)=[r_1(k) \quad r_2(k) \quad r_3(k)]^T$, are normalized with respect to direct current (DC)-link voltage V_{dc}. For a given duty ratio, $[\alpha_1(k) \ \alpha_2(k) \ \alpha_3(k)]^T$, the produced phase voltage is $\mathbf{S}_c[\alpha_1 \ \alpha_2 \ \alpha_3]^T$. Therefore, the difference between the reference input and the produced phase voltage is in the form

$$\mathbf{r}(k)-\mathbf{S}_c q_b\left\{\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}\right\}, \tag{3}$$

where $q_b\{y\}$ is the quantization that ensures y belongs to the set $\{0,1/2^b,2/2^b,\cdots,(2^b-1)/2^b,1\}$. To compensate for the error in Equ. (3), the duty ratio is adjusted according to minimizing the effect of accumulated error, $\mathbf{e}(k)$, which is the accumulated difference in the desired and the produced phase voltages, that is,

$$\mathbf{e}(k)=\mathbf{e}(k-1)+\mathbf{r}(k)-\mathbf{S}_c q_b\left\{\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}\right\}. \tag{4}$$

Therefore, the duty ratio is obtained by minimizing $\mathbf{e}(k)$ in Equ. (4). Equ. (4) implies that switching commands are influenced by input $\mathbf{r}(k)$ and previous error signal $\mathbf{e}(k-1)$. The duty ratio can be obtained accordingly by solving the matching problem given below.

$$\mathbf{d}(k)=\begin{bmatrix}2/3 & -1/3 & -1/3\\ -1/3 & 2/3 & -1/3\\ -1/3 & -1/3 & 2/3\end{bmatrix}\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}, \tag{5a}$$

$$\text{where } \mathbf{d}(k)=\mathbf{e}(k-1)+\mathbf{r}(k). \tag{5b}$$

C. Duty Ratios for Error Compensation

Eigenvalue decomposition is applied to find the duty ratios that satisfy Equ. (5), that is, Equ. (5a) is written as

$$\mathbf{d}(k)=[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]\begin{bmatrix}0 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]^T\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}, \tag{6}$$

where $\mathbf{v}_i, i=1,2,3$ are the eigenvectors of $\mathbf{S}_c$, and

$$[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]=\begin{bmatrix}-1/\sqrt{3} & 2/\sqrt{6} & 0\\ -1/\sqrt{3} & -1/\sqrt{6} & -1/\sqrt{2}\\ -1/\sqrt{3} & -1/\sqrt{6} & 1/\sqrt{2}\end{bmatrix}.$$

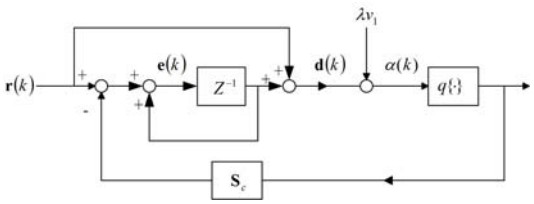


Fig. 2. Block diagram of quantization error compensation.

Given that the matrix $[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]$ is orthonormal, Equ. (6) can be written as

$$[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]^T\mathbf{d}(k)=\begin{bmatrix}0 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}[\mathbf{v}_1 \quad \mathbf{v}_2 \quad \mathbf{v}_3]^T\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}, \tag{7}$$

which implies that

$$\begin{bmatrix}\mathbf{v}_1^T\mathbf{d}(k)\\ \mathbf{v}_2^T\mathbf{d}(k)\\ \mathbf{v}_3^T\mathbf{d}(k)\end{bmatrix}=\begin{bmatrix}0\\ \mathbf{v}_2^T\mathbf{a}(k)\\ \mathbf{v}_3^T\mathbf{a}(k)\end{bmatrix}, \text{ where } \mathbf{a}(k)=\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}. \tag{8}$$

To have a solution in Equ. (8), the $\mathbf{v}_1^T\mathbf{d}(k)$ in the left-hand side of Equ. (8) must be zero. The equation $\mathbf{v}_1^T\mathbf{d}(k)=0$ is proven in Appendix A. Considering the matching equation in Equ. (9), $\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}=\mathbf{d}(k)$ is a solution regardless of the constraint $\alpha_i \in [0 \quad 1]$.

$$\mathbf{v}_2^T\mathbf{d}(k)=\mathbf{v}_2^T\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix} \textit{ and } \mathbf{v}_3^T\mathbf{d}(k)=\mathbf{v}_3^T\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix} \tag{9}$$

A modified solution, as shown in Equ. (10), can be applied to have feasible duty ratios. Given that $\mathbf{v}_2^T\mathbf{v}_1=0$ and $\mathbf{v}_3^T\mathbf{v}_1=0$, Equ. (9) still holds when the duty ratios in Equ. (10) are used.

$$\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix}=\mathbf{d}(k)+\lambda\mathbf{v}_1 \tag{10}$$

λ is a real number and is selected to ensure that the values of duty ratios α_i are feasible. One selection of λ is to set it to be $\sqrt{3}$ multiplied with the minimum value among the elements in $\mathbf{d}(k)$. The injection of λ will not influence the produced phase voltage when the y-connected load with an isolated neutral point is applied. The block diagram for quantization error compensation is shown in Fig. 2. The output $q\{\alpha(k)\}$ is the corresponding phase duties that are used to produce switching commands.

D. System Analysis

Proposition 1: Given a reference $\mathbf{r}=[r_1 \quad r_2 \quad r_3]^T$ satisfying $r_1+r_2+r_3=0$, the duty ratios produced by Equs. (10), (5b),

and (4) for a three-phase VSI can compensate for the voltage error of each phase.

[Proof] Considering the duty ratios produced for the present input $\mathbf{r}(k)$ and using Equs. (10) and (5b), duty ratios can be written as

$$\begin{bmatrix}\alpha_1(k)\\ \alpha_2(k)\\ \alpha_3(k)\end{bmatrix} = \mathbf{d}(k)+\lambda\mathbf{v}_1 = \mathbf{e}(k-1)+\mathbf{r}(k)+\lambda\mathbf{v}_1. \quad (11)$$

By substituting Equ. (11) into Equ. (4), we can write

$$\mathbf{e}(k) = \mathbf{e}(k-1)+\mathbf{r}(k)-\mathbf{S}_c q_b\{\mathbf{e}(k-1)+\mathbf{r}(k)+\lambda\mathbf{v}_1\}. \quad (12)$$

We define the error $\mathbf{\Delta}_b(k)$ as the difference between the desired and the produced duty ratios within a carrier period, namely,

$$\mathbf{\Delta}_b(k) = [\mathbf{e}(k-1)+\mathbf{r}(k)+\lambda\mathbf{v}_1]-[q_b\{\mathbf{e}(k-1)+\mathbf{r}(k)+\lambda\mathbf{v}_1\}]. \quad (13)$$

Equ. (12) can then be rewritten as Equ. (14), applying that $\mathbf{S}_c\mathbf{v}_1 = \mathbf{0}$, $\mathbf{S}_c\mathbf{e}(k) = \mathbf{e}(k)$, and $\mathbf{S}_c\mathbf{r}(k) = \mathbf{r}(k)$.

$$\begin{aligned}\mathbf{e}(k) &= \mathbf{e}(k-1)+\mathbf{r}(k)+\mathbf{S}_c(\mathbf{\Delta}_b(k)-[\mathbf{e}(k-1)+\mathbf{r}(k)+\lambda\mathbf{v}_1])\\ &= \mathbf{S}_c\mathbf{\Delta}_b(k)\end{aligned} \quad (14)$$

The right-hand side of Equ. (14) is the error mapping by the matrix $\mathbf{S}_c$. The voltage error appears on the Y-connected phases. Therefore, Equ. (14) implies that with the duty ratios produced by Equ. (10), the error signal $\mathbf{e}(k)$ is the voltage deviation on the phases. From Equ. (5b), this deviation is used to adjust the reference during the subsequent carrier period to produce duty ratios. Therefore, a single cycle is sufficient for the algorithm to cancel the voltage error. However, the voltage reference and the quantization error are not constant, that is, at any iteration, a residual voltage error exists. The phase voltage deviation produced during the previous carrier period is compensated for by applying one cycle delay tracking of the reference voltage, as shown in Equs. (10), (5b), and (4).

E. Asymmetric Pulse Production

The rate of error compensation is selected to be twice the carrier frequency to improve the quality of the produced phase voltage. In this setting, given a carrier frequency f_c, the reference, $\mathbf{r}(k_1)$, and the duty ratios, $[\alpha_1(k_1)\ \ \alpha_2(k_1)\ \ \alpha_3(k_1)]^T$, are updated at a rate $2f_c$, that is, the signals to be compared with triangular wave during rising and falling edges are different. k_1 corresponds to the index of period $1/(2f_c)$, whereas k corresponds to the index of period $1/f_c$.

Proposition 2: A three-phase VSI modulator with carrier frequency f_c can compensate for errors every half-carrier period for the regular sampled reference $\mathbf{r}(k_1) = [r_1(k_1)\ \ r_2(k_1)\ \ r_3(k_1)]^T$ (sampled at the frequency $2f_c$) when the duty ratio for each reference $\mathbf{r}(k_1)$ is selected as

$$\begin{bmatrix}\alpha_1(k_1)\\ \alpha_2(k_1)\\ \alpha_3(k_1)\end{bmatrix} = \mathbf{d}(k_1)+\lambda\begin{bmatrix}-1/\sqrt{3}\\ -1/\sqrt{3}\\ -1/\sqrt{3}\end{bmatrix} = \mathbf{d}(k_1)-\lambda_1\begin{bmatrix}1\\1\\1\end{bmatrix}, \quad (15)$$

where $\mathbf{d}(k_1) = \mathbf{e}(k_1-1)+\mathbf{r}(k_1)$, (16)

$$\mathbf{e}(k_1) = \mathbf{e}(k_1-1)+\mathbf{r}(k_1)-\mathbf{S}_c q_b\left\{\begin{bmatrix}\alpha_1(k_1)\\ \alpha_2(k_1)\\ \alpha_3(k_1)\end{bmatrix}\right\}, \quad (17)$$

and λ_1 is the minimum value among the elements in $\mathbf{d}(k)$.

[Proof] The error $\mathbf{\Delta}_b(k_1)$ is defined as the difference between the desired and the produced duty ratios during k_1-th half-carrier period, that is,

$$\begin{aligned}\mathbf{\Delta}_b(k_1) = &[\mathbf{e}(k_1-1)+\mathbf{r}(k_1)+\lambda\mathbf{v}_1]\\ &-[q_b\{\mathbf{e}(k_1-1)+\mathbf{r}(k_1)+\lambda\mathbf{v}_1\}].\end{aligned} \quad (18)$$

By substituting Equs. (15), (16), and (18) into Equ. (17), we can write

$$\begin{aligned}\mathbf{e}(k_1) &= \mathbf{e}(k_1-1)+\mathbf{r}(k_1)-\mathbf{S}_c q_b\{\mathbf{e}(k_1-1)+\mathbf{r}(k_1)+\lambda\mathbf{v}_1\}\\ &= [\mathbf{e}(k_1-1)+\mathbf{r}(k_1)]-\mathbf{S}_c(\mathbf{e}(k_1-1)+\mathbf{r}(k_1)-\mathbf{\Delta}_b(k_1)).\\ &= \mathbf{S}_c\mathbf{\Delta}_b(k_1)\end{aligned} \quad (19)$$

Equ. (19) states that the error signal, $\mathbf{e}(k_1)$, is the voltage deviation in the Y-connected load. This error signal is compensated for by adjusting the reference of the subsequent half-carrier period as [see Equ. (16)]

$$\mathbf{d}(k_1+1) = \mathbf{e}(k_1)+\mathbf{r}(k_1+1). \quad (20)$$

Therefore, the proposed three-phase VSI modulator can compensate for voltage errors every half-carrier period.

III. SIMULATION RESULTS

To confirm the effectiveness of the proposed ECPWM, the conventional SVPWM and the proposed ECPWM are implemented by visual C++, and the three-phase VSI with R–L load is built by PSIM. The resistance (inductance) of the load is 10 Ω (15 mH). The DC-link voltage is 15 V.

The 50 Hz sinusoidal wave with a normalized amplitude of 0.5 is sampled at 8 kHz and applied to the modulators (SVPWM and ECPWM) to produce gating signals. The carrier frequency of SVPWM (ECPWM) is set as 8 kHz (4 kHz), and the pulse bit resolution of both modulators is 10.

The gating signals for the first phase lag and the produced phase voltages/currents for both modulators are shown in Figs. 3 and 4. The phase voltages produced by the ECPWM and the SVPWM are comparable by using half of the switching number in the ECPWM. The frequency components of the produced phase voltage and the phase current are shown in Figs. 5–8 to analyze baseband harmonic distortion. The baseband harmonics of the voltage/current produced by the ECPWM are reduced by using only half of the switching frequency in contrast to those produced by the SVPWM.

For precise comparison, Table I (Table II) lists the voltage

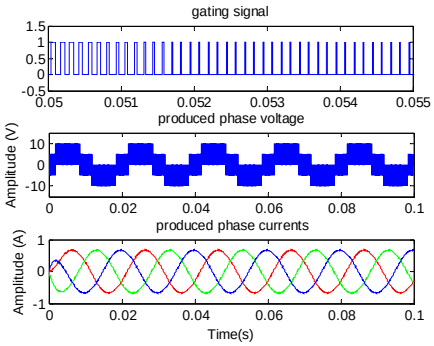


Fig. 3. Simulation results for the SVPWM (upper: gating signal for the first phase lag, middle: produced phase voltage, lower: produced phase currents).

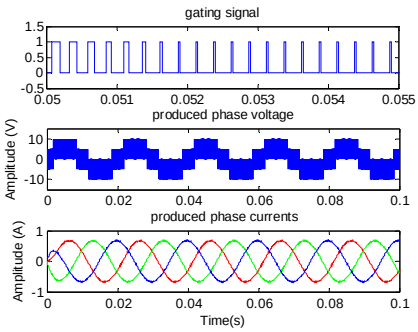


Fig. 4. Simulation results for the ECPWM (upper: gating signal for the first phase lag, middle: produced phase voltage, lower: produced phase currents).

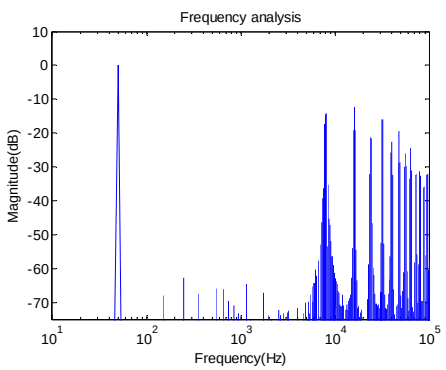


Fig. 5. Frequency analysis of the phase voltage produced by the SVPWM.

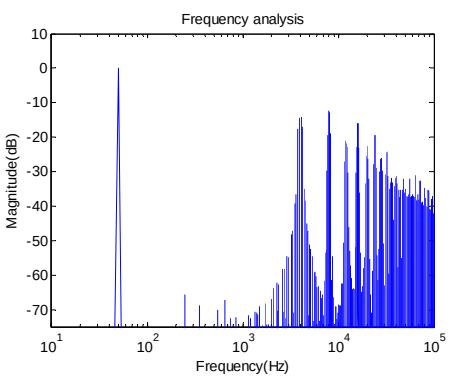


Fig. 6. Frequency analysis of the phase voltage produced by the ECPWM.

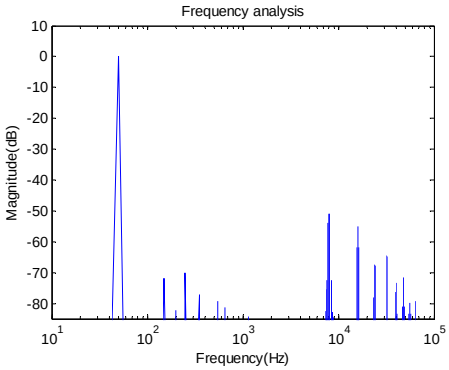


Fig. 7. Frequency analysis of the phase current produced by the SVPWM.

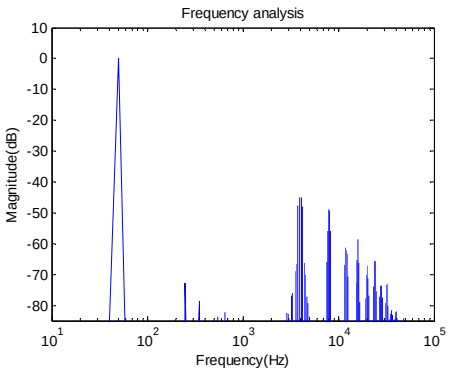


Fig. 8. Frequency analysis of the phase current produced by the ECPWM.

TABLE I
SIMULATION RESULT: HARMONIC ANALYSIS OF THE PRODUCED PHASE VOLTAGE

Modulator	Input frequency 50 Hz		
	Carrier frequency (Hz)	Harmonics within [0 1 k] Hz (%)	Harmonics within [0 3 k] Hz (%)
SVPWM	8 k	0.129	0.167
	4 k	0.132	0.402
ECPWM	4 k	0.095	0.370

TABLE II
SIMULATION RESULT: HARMONIC ANALYSIS OF THE PRODUCED PHASE CURRENT

Modulator	Input frequency 50 Hz		
	Carrier frequency (Hz)	Harmonics within [0 1 k] Hz (%)	Harmonics within [0 3 k] Hz (%)
SVPWM	8 k	0.047	0.047
	4 k	0.054	0.057
ECPWM	4 k	0.029	0.033

(current) harmonic distortion under different carrier frequencies. The voltage/current harmonics increase when the carrier frequency of the SVPWM is reduced. The ECPWM can reduce the baseband harmonic distortion under a low-carrier frequency setting by applying the error compensation mechanism. Among the three different

modulators in Table I/Table II, the harmonic distortion of the ECPWM is the lowest within [0 1 k] Hz. The compensation for the accumulated voltage error enhances the low-frequency performance.

IV. Experiments

Two experimental platforms are built to confirm the correctness and the feasibility of the proposed modulator. In the first part of this section, the experimental results for a three-phase VSI connected with a Y-type R–L load are shown. In the second part, a motor drive system using FOC is implemented. Both the SVPWM and the ECPWM are applied and compared. Results indicate that the proposed modulator can be applied directly to the FOC-based motor controller.

A. Experimental Results for VSI Drive

In the first experimental platform, six power MOSFETs (IRF640N) are used to build a three-phase VSI. The DC-link voltage is 15 V, and the output of the VSI is connected to a Y-type R–L load (R = 10 Ω, L = 15 mH). Both the proposed ECPWM and the conventional SVPWM are implemented on a field-programmable gate array (FPGA, EP2C20F484C8, Cyclone II) to produce gating commands.

For the 50 Hz sinusoidal reference with a normalized amplitude of 0.5 and a sampling frequency of 8 kHz, Figs. 9–12 plot the frequency-domain analysis of the measured phase voltage/current. The carrier frequency of the SVPWM (ECPWM) is 8 kHz (4 kHz), and the pulse bit resolution is 10. From Figs. 9–12, the baseband harmonics are reduced by using the proposed ECPWM. Tables III and IV list the harmonic distortions of the phase voltage/current for different carrier frequencies. Similar observations to simulations are obtained as follows: (a) the harmonic distortion increases with the reduction in the carrier frequency by using the SVPWM; (b) using the ECPWM can reduce baseband harmonic distortion under a low-carrier frequency setting.

B. Experimental Platform for Motor-Speed Controller

To confirm the feasibility of the proposed modulator, the motor drive system using FOC is implemented in a micro-controller (SH7137) to drive a PMSM (HVP75), which is connected to magnetic powder brakes (ZKB010AA). A torque-measuring shaft (DATAFLEXE 22/100) is inserted between the PMSM and the brakes. The input references for the SVPWM and the ECPWM are sampled at a rate of 8 kHz, and the pulse bit resolution for the SVPWM (ECPWM) is 13 (8). The carrier frequency of the SVPWM is 8 kHz, whereas that of the ECPWM is 4 kHz. An FPGA (EP2C35F484C6) is used to receive the desired duty ratio from the micro-controller and generate switching commands to produce the asymmetric switching commands of ECPWM. The block diagram of the motor driver using the SVPWM (ECPWM) is shown in Fig. 13 (Fig. 14). The three-phase

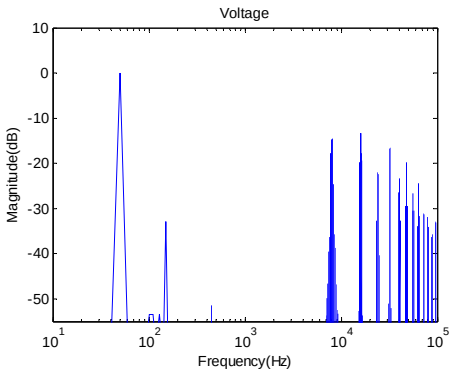


Fig. 9. Frequency analysis of the phase voltage produced by the SVPWM.

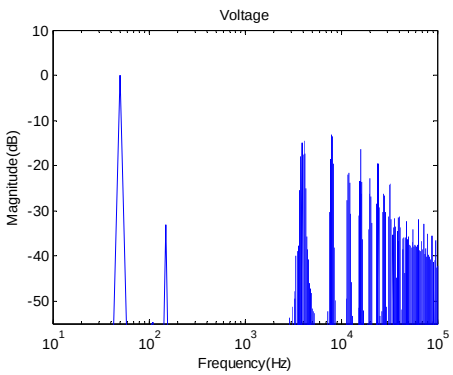


Fig. 10. Frequency analysis of the phase voltage produced by the ECPWM.

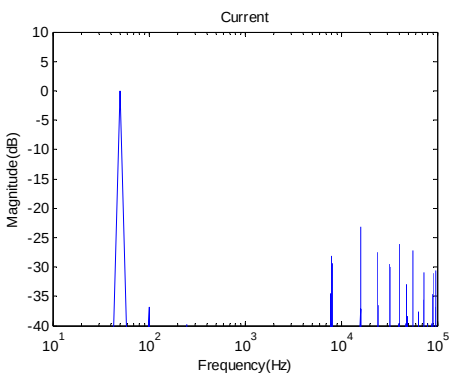


Fig. 11. Frequency analysis of the phase current produced by the SVPWM.

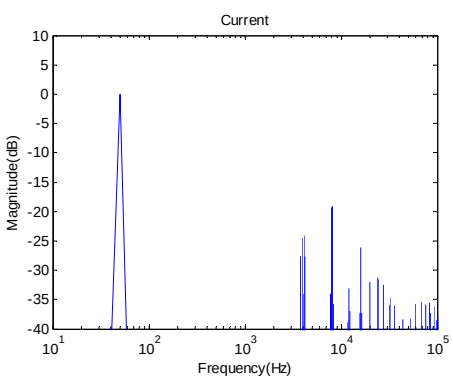


Fig. 12. Frequency analysis of the phase current produced by the ECPWM.

TABLE III
EXPERIMENTAL RESULT: HARMONIC ANALYSIS OF THE PRODUCED PHASE VOLTAGE

Modulator	Carrier frequency (Hz)	Harmonics within [0 1 k] Hz (%)	Harmonics within [0 3 k] Hz (%)
SVPWM	8 k	2.323	2.327
	4 k	2.457	2.483
ECPWM	4 k	2.251	2.283

TABLE IV
EXPERIMENTAL RESULT: HARMONIC ANALYSIS OF THE PRODUCED PHASE CURRENT

Modulator	Input frequency 50 Hz		
	Carrier frequency (Hz)	Harmonics within [0 1 k] Hz (%)	Harmonics within [0 3 k] Hz (%)
SVPWM	8k	1.888	2.029
	4k	2.532	2.685
ECPWM	4k	1.592	1.751

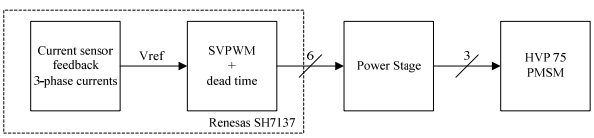


Fig. 13. Block diagram of the implementation platform using the SVPWM.

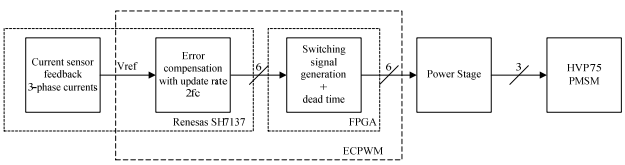


Fig. 14. Block diagram of the implementation platform using the ECPWM.

power stage is composed of six n-channel power MOSFETs (IRFP360). The specifications are listed in Table V. The dead-time is set to be 2 μs to prevent arm shooting through, and the DC-link voltage is 120 V.

C. Measured Waveforms for Motor-Speed Control

Fig. 15 shows the switching commands of the upper switch of the first phase lag under a motor speed of 300 rpm. The switching frequency of the ECPWM is half that of the SVPWM. Both modulators can properly produce three-phase current, as shown in Fig. 16. The current ripple produced by the ECPWM is higher than that of the SVPWM because of its lower carrier frequency.

For precise comparison, the harmonic distortions under different motor speeds are shown in Table VI. Using only half of the switching number, the baseband harmonic distortion of the ECPWM is lower than that of the SVPWM.

D. Efficiency of the Motor-Speed Control System

The power supplied to the system (denoted as P_{in}) and the the efficiency of the motor driving system. The efficiency is

TABLE V
SPECIFICATIONS OF POWER SWITCH

	IRFP360
V_{DS}	400 (V)
$I_{D(\max)}$	23 (A)
$R_{DS(on)}$	0.2 (Ω)
$Q_{g(\max)}$	210 (nC)
Q_{gs}	30 (nC)
Q_d	(nC)

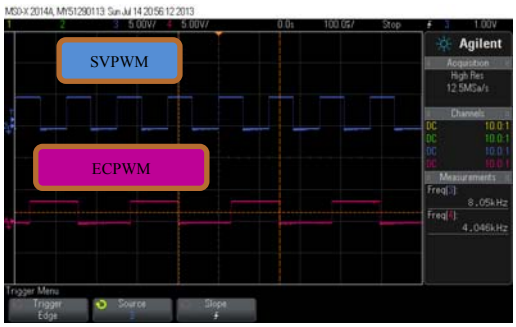
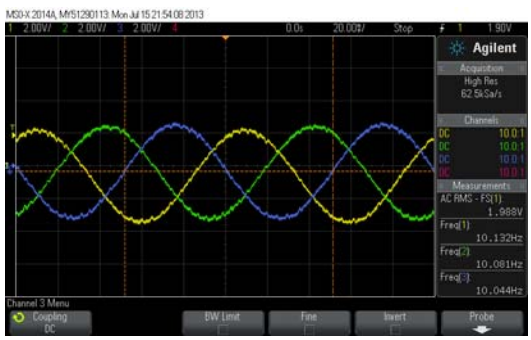
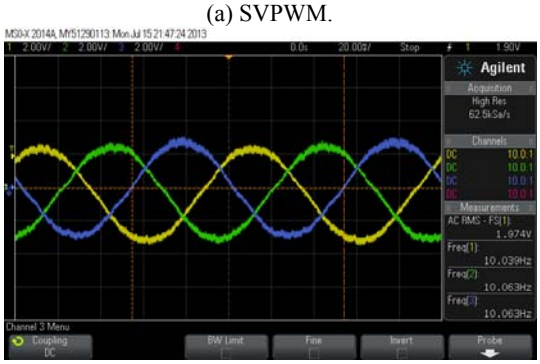


Fig. 15. Switching commands of the SVPWM and the ECPWM.



(a) SVPWM.



(b) ECPWM.

Fig. 16. Produced three-phase current under a motor speed of 300 rpm.

then obtained according to $\eta = (Torque \times Speed)/P_{in} \times 100(\%)$.

The measured motor speed and the output torque under different speed commands are listed in Table VII. The average input/output power within a 15-min operation is listed in Table VIII. The average input power by using the ECPWM is smaller than that by using the SVPWM, whereas the average output power by using the ECPWM is larger than

TABLE VI
SWITCHING NUMBER AND CURRENT HARMONIC DISTORTION AT DIFFERENT MOTOR SPEEDS

Motor speed (rpm)		300	400	500
Switching number per second	SVPWM	48 k	48 k	48 k
	ECPWM	24 k	24 k	24 k
Current harmonic within [0 250] Hz (%)	SVPWM	1.04	0.91	0.99
	ECPWM	0.93	0.70	0.80
Reduction rate (%)		10.6	23.1	19.2

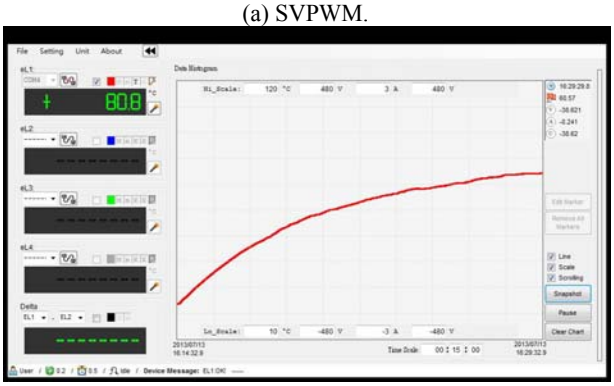
TABLE VII
PRODUCED MOTOR SPEED AND OUTPUT TORQUE

Motor speed command (rpm)		300	400	500
measured motor speed (rpm)	SVPWM	302.28	402.54	503.29
	ECPWM	302.28	402.52	503.23
measured output torque (Nm)	SVPWM	1.78	1.81	1.87
	ECPWM	1.81	1.88	1.91

TABLE VIII
MEASURED INPUT/OUTPUT POWER OF THE MOTOR DRIVE SYSTEM

Motor Speed (rpm)	Command	300	400	500
input power (W)	SVPWM	96.37	121.76	147.54
	ECPWM	91.24	117.21	142.39
motor mechanical power (W)	SVPWM	56.35	76.30	98.56
	ECPWM	57.29	79.33	100.65
efficiency (%)	SVPWM	58.45	62.66	66.80
	ECPWM	62.80	67.68	70.69
efficiency improvement (%)		7.44	8.01	5.82

(a) SVPWM.



(b) ECPWM.

Fig. 17. Measured temperature within [0 15]-min operating at a speed of 500 rpm.

TABLE IX
MEASURED MOSFET TEMPERATURE UNDER VARIOUS MOTOR SPEEDS

Motor speed (rpm)		300	400	500
temperature (°C)	SVPWM	101.1	104.1	107.4
	ECPWM	77.1	79.3	80.8

mechanical output power of the motor are measured to obtain that by using the SVPWM under the same motor speed commands. Therefore, the efficiency of the ECPWM is higher than that of the SVPWM. In Table VIII, the efficiency improvement is calculated according to

$$efficiency\ improvement = (\eta_{ECPWM} - \eta_{SVPWM})/\eta_{SVPWM} \times 100(\%).$$

An average of 7.09% efficiency improvement is obtained by using the ECPWM, and a maximum efficiency improvement of 8.01% is achieved at a motor speed of 400 rpm (refer to Table VIII).

The measured result reveals that the reduction in switching frequency and baseband harmonics helps to improve the efficiency of the motor drive.

E. MOSFET Operating Temperature

The advantage of switching frequency reduction can also be observed from the temperature measurement of MOSFET. Fig. 17 shows the temperature variation in MOSFET during the 15-min operation with a motor speed of 500 rpm. The initial temperature (air temperature in the room) is 25 °C. After 7.5-min operation, the MOSFET temperature corresponds to the following conditions: the ECPWM rises to 67 °C, whereas the SVPWM is 94 °C. Therefore, for the same operating time, the heat dissipation requirement of the ECPWM is lower. The temperature at the end of the operation is 107.4 (80.8) °C by using the SVPWM (ECPWM), which shows a great reduction in operation temperature by using the ECPWM. Similar observations are obtained with different motor speeds. The measured temperatures after 15-min operation are listed in Table IX. A maximum reduction of 26.6 °C is obtained. Therefore, the proposed method outperforms the SVPWM in reducing the operating temperature.

A high temperature of power MOSFET leads to low efficiency of the inverter [29]. For every 10 °C increase in the working temperature, the lifetime reduction in MOSFET is approximately 40% [26]. Therefore, reducing the temperature of switches not only lessens the heat sink requirement but also improves both the power efficiency and the lifetime of switches.

V. CONCLUSION

An ECPWM is proposed in this work. By adjusting the reference signal according to the accumulated error signal, the proposed method can compensate for the difference in the desired and the produced phase voltages. The switching frequency can also be reduced with an improved baseband

harmonic performance by selecting the compensating rate as twice the carrier frequency.

In the simulation, a three-phase VSI with R–L load is built. Results imply that the baseband harmonic distortion of the voltage/current produced by the SVPWM increases with decreased carrier frequency. By applying the error compensation mechanism every half-carrier period, the proposed ECPWM improves the baseband harmonic under a low-carrier frequency setting.

In the first experiment, a three-phase VSI with R–L load is built. The measured phase voltages/currents produced by the SVPWM and the ECPWM show similar observations to that obtained in the simulation. A motor drive platform based on FOC is built on Renesas SH7137 to drive a PMSM (HVP75) with magnetic powder brakes to further confirm the effectiveness of the proposed modulator. The measured results indicate that the reduction in both baseband harmonic and carrier frequency can improve the system efficiency.

The advantage of switching number reduction is shown by MOSFET temperature measurement. The measured data imply that the operating temperature is reduced by using the ECPWM with a maximum improvement of 26.6 °C. Therefore, by using the proposed modulator, the drive system can work with few cooling requirements, high efficiency, and long lifetime of power switches.

APPENDIX A

Proposition A1: For a reference $\mathbf{r}=[r_1 \quad r_2 \quad r_3]^T$ satisfying $r_1+r_2+r_3=0$ and with zero initial conditions, the desired signal $\mathbf{d}(k)$ produced according to Equs. (4) and (5b) satisfies Equ. (A1) regardless of the selection of duty ratios. $\mathbf{v}_1^T\mathbf{d}(k)=0, \ \forall k$,

where $\mathbf{v}_1=\left[-1/\sqrt{3} \quad -1/\sqrt{3} \quad -1/\sqrt{3}\right]^T$. (A1)

[Proof]:

To prove Equ. (A1), the expression of $\mathbf{d}(k)$ in Equ. (5b) is considered. By applying $r_1+r_2+r_3=0$ (i.e., $\mathbf{v}_1^T\mathbf{r}(k)=\mathbf{0}, \forall k$), we can write

$$\begin{aligned}\mathbf{v}_1^T\mathbf{d}(k)&=\mathbf{v}_1^T\left(\mathbf{e}(k-1)+\mathbf{r}(k)\right)\\&=\mathbf{v}_1^T\mathbf{e}(k-1)+\mathbf{v}_1^T\mathbf{r}(k).\\&=\mathbf{v}_1^T\mathbf{e}(k-1)\end{aligned} \quad (A2)$$

To analyze error signal $\mathbf{e}(k-1)$ under zero initial condition, let

$$\mathbf{e}(0)=\mathbf{r}(0)=\mathbf{d}(0)=\mathbf{0}.$$

The error signal at $k=1$ is obtained from Equ. (4), as shown below.

$$\mathbf{e}(1)=\mathbf{r}(1)-\mathbf{S}_c q_b\left\{\begin{bmatrix}\alpha_1(1)\\ \alpha_2(1)\\ \alpha_3(1)\end{bmatrix}\right\} \quad (A3)$$

Given that $\mathbf{v}_1$ is an eigenvector of $\mathbf{S}_c$ that corresponds to an eigenvalue of 0, we can write

$$\begin{aligned}\mathbf{v}_1^T\mathbf{e}(1)&=\mathbf{v}_1^T\mathbf{r}(1)-\mathbf{v}_1^T\mathbf{S}_c q_b\{[\alpha_1(1) \quad \alpha_2(1) \quad \alpha_3(1)]\}\\&=-\left(\mathbf{S}_c^T\mathbf{v}_1\right)^T q_b[\alpha_1(1) \quad \alpha_2(1) \quad \alpha_3(1)]\\&=-\left(\mathbf{S}_c\mathbf{v}_1\right)^T q_b[\alpha_1(1) \quad \alpha_2(1) \quad \alpha_3(1)]\\&=\mathbf{0}\end{aligned} \quad . \quad (A4)$$

For any values of $[\alpha_1(1) \quad \alpha_2(1) \quad \alpha_3(1)]$, $\mathbf{v}_1^T\mathbf{e}(1)=\mathbf{0}$ always holds. Following the procedures of Equs. (A3) and (A4), we can prove from Equ. (4) that $\mathbf{v}_1^T\mathbf{e}(k)=0, \ \forall k$, which implies that Equ. (A1) is satisfied.

ACKNOWLEDGMENT

This work was supported by the Ministry of Science and Technology, Taiwan under contract MOST 103-2221-E-155-025-.

REFERENCES

[1] D.-W. Chung, J.-S. Kim, and S.-K. Sul, "Unified voltage modulation technique for real-time three-phase power conversion," *IEEE Trans. Ind. Appl*., Vol. 34, No. 2, pp. 374-380, Mar./Apri. 1998.

[2] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverter," *IEEE Trans. Ind. Informat*., Vol. 9, No 2, pp. 609-619, May 2013.

[3] A. Iqbal and S. Moinuddin, "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI," *IEEE Trans. Power Electron*., Vol. 24, No. 10, pp. 2379-2390, Oct. 2009.

[4] J. Yuan, J. Pan, W. Fei, C. Cai, Y. Chen, and B. Chen, "An immune-algorithm-based space-vector PWM control strategy in a three-phase inverter," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 2084-2093, May 2013.

[5] M. Narimani and G. Moschopoulos, "Three-phase multimodule VSIs using SHE-PWM to reduce zero-sequence circulating current," *IEEE Trans. Ind. Electron*., Vol. 61, No. 4, pp. 1659-1668, Apr. 2014.

[6] K.-Y. Chen and J.-S. Hu, "A filtered SVPWM for multiphase voltage source inverters considering finite pulse-width resolution," *IEEE Trans. Power Electron*., Vol. 27, No. 7, pp. 3107-3118, Jul. 2012.

[7] B. Zhang, K. Zhou, and D. Wang, "Multirate repetitive control for PWM DC/AC converters," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 6, pp. 2883-2890, Jun. 2014.

[8] S. Mekhilef, M. N. A. Kadir, and Z. Salam, "Digital control of three phase three-stage hybrid multilevel inverter," *IEEE Trans. Ind. Informat.*, Vol. 9, No 2, pp. 719-727, May 2013.

[9] J. Shi and S. Li, "Analysis and compensation control of dead-time effect on space vector PWM," *Journal of Power Electronics*, Vol. 15, No. 2, pp. 431-442, Mar. 2015.

[10] B.-R. Lin and Y.-B. Nian, "Analysis and implementation of a new three-level converter," *Journal of Power Electronics*, Vol. 14, No. 3, pp. 478-487, May 2014.

[11] S. Srinivas and K. R. Sekhar, "Theoretical and experimental analysis for current in a dual-inverter-fed open-end winding induction motor drive with reduced switching PWM," *IEEE Trans. Ind. Electron*., Vol. 60, No. 10, pp. 4318-4328, Oct. 2013.

[12] F. Wang, Z. Zhang, A. Davari, J. Rodríguez, and R. Kennel,

"An experimental assessment of finite-state predictive torque control for electrical drives by considering different online-optimization methods," *Control Engineering Practice*, Vol. 31, pp. 1-8, Oct. 2014.
[13] A. E. Fadili, F. Giri, A. E. Magri, R. Lajouad, and F. Z. Chaoui, "Adaptive control strategy with flux reference optimization for sensorless induction motors," *Control Engineering Practice*, Vol. 26, pp. 91-106, May 2014.
[14] S. Du, J. Liu, and T. Liu, "A PDPWM based DC capacitor voltage control method for modular multilevel converters," *Journal of Power Electronics*, Vol. 15, No. 3, pp. 660-669, May 2015.
[15] R. Nagarajan and M. Saravanan, "Performance analysis of a novel reduced switching cascaded multilevel inverter," *Journal of Power Electronics*, Vol. 14, No. 1, pp. 48-60, Jan. 2014.
[16] A. R. Beig, S. Kanukollu, K. A. Hosani, and A. Dekka, "Space vector based synchronized three level discontinuous PWM for medium voltage high power VSI," *IEEE Trans. Ind. Electron*., Vol. 61, No. 8, pp 3891-3901, Aug. 2014.
[17] S.-L. An, X.-D. Sun, Q. Zhang, Y.-R. Zhong, and B-Y. Ren, "Study on the novel generalized discontinuous SVPWM strategies for three-phase voltage source inverters," *IEEE Trans. Ind. Informat*., Vol. 9, No 2, pp. 781-789, May 2013.
[18] J.-S. Hu, K.-Y. Chen, T.-Y. Shen, and C.-H. Tang, "Control of voltage source inverter using Multi-dimensional Feedback Quantization Modulator," *IEEE Trans. Ind. Electron*., Vol. 58, No. 7, pp. 3027-3036, Jul. 2011.
[19] K.-Y. Chen, J.-S. Hu, C.-H. Tang, and T.-Y. Shen, "A novel switching strategy for FOC motor drive using multi-dimensional feedback quantization," *Control Engineering Practice*, Vol. 20, No. 2, pp. 196-204, Feb. 2012.
[20] D. Zhao, V. S. S. P. K. Hari, G. Narayanan, and R. Ayyanar, "Space-vector-based hybrid pulsewidth modulation techniques for reduced harmonic distortion and switching loss," *IEEE Trans. Power Electron*., Vol. 25, No. 3, pp. 760-774, Mar. 2010.
[21] L. Mathe, F. Lungeanu, D. Sera, P. O. Rasmussen, and J. K. Pedersen, "Spread spectrum modulation by using asymmetric-carrier random PWM," *IEEE Trans. Ind. Electron*., Vol. 59, No. 10, pp. 3710-3718, Oct. 2012.
[22] A. T. Islier, A. Ersak, and G. Richards, "Harmonic minimization in a three-phase asymmetrical PWM rectifier," in *Proc. 7th Mediterranean Electrotechnical conference*, Vol. 2, pp. 829-832, Apr. 1994.
[23] P. Sanjit and A. Aurasopon, "Asymmetrical PWM for harmonics reduction and power factor improvement in PWM AC choppers using bee colony optimization," *Journal of Power Electronics*, Vol. 15, No. 1, pp. 227-234, Jan. 2015.
[24] A. M. Hava and E. Un, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron*., Vol. 26, No. 7, pp. 1998-2008, Jul. 2011.
[25] S. K. Singh, F. Guédon, P. J. Garsed, and R. A. McMahon, "Half-bridge SiC inverter for hybrid electric vehicles: Design, development and testing at higher operating temperature," in 6th IET International Conference on Power Electronics, Machines and Drives(PEMD 2012), pp.1-6, Mar. 2012.
[26] M. Ikonen, "*Power cycling lifetime estimation of IGBT power modules based on chip temperature modeling*," Ph.D. dissertation, Lappeenranta University of Technology, Lappeenranta, Finland, Dec. 2012.

Keng-Yuan Chen received her B.S., M.S., and Ph.D. degrees from the Department of Electrical and Control Engineering, National Chiao-Tung University, Taiwan in 2003, 2005, and 2010, respectively. From 2011 to July 2012, she was a researcher with the Mechanical and System Laboratory, Industrial Technology Research Institute, Hsinchu. Since August 2012, she has been with the Department of Electrical Engineering, Yuan Ze University, Chung-Li, Taiwan. Her research interests include multi-phase pulse-width modulation, digital signal processing, and power electronics.

Jwu-Sheng Hu (M'94) received his B.S. degree from the Department of Mechanical Engineering, National Taiwan University, Taiwan, in 1984 and his M.S. and Ph.D. degrees from the Department of Mechanical Engineering, University of California, Berkeley, in 1988 and 1990, respectively.
From 1991–1993, he was an assistant professor in the Department of Mechanical Engineering at Wayne State University, Detroit, MI. He joined the Department of Electrical Engineering, National Chiao Tung University, Taiwan, in 1993 and became a full professor in 1998. In 2008, he worked in part at the Industrial Technology Research Institute (ITRI) of Taiwan, where he served as an advisor for the Intelligent Robotics Program and as principal investigator of large-scale robotic research projects funded by the Ministry of Economic Affairs. He also served as an advisor at the National Chip Implementation Center of Taiwan for embedded system design applications. Since 2015, he has served as the general director of the Mechanical and System Laboratory, ITRI. His current research interests include robotics, mechatronics, and embedded systems.

Jau-Nan Lin received his B.S. degree from the Department of Electrical Engineering, National Chiao-Tung University, Taiwan, in 2010. He is currently studying for his Ph.D. degree at the Institute of Electrical Control Engineering, National Chiao-Tung University, Taiwan. His main research interests are embedded systems, intelligent mobile robots, and power electronics.