JPE 16-1-38

http://dx.doi.org/10.6113/JPE.2016.16.1.374
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Improved Analytical Model for Predicting the Switching Performance of SiC MOSFETs

Mei Liang†, Trillion Q. Zheng*, and Yan Li*

†*School of Electrical and Engineering, Beijing Jiaotong University, Beijing, China

Abstract

This paper derives an improved analytical model to estimate switching loss and analyze the effects of parasitic elements on the switching performance of SiC MOSFETs. The proposed analytical model considers the parasitic inductances, the nonlinearity of the junction capacitances and the nonlinearity of the trans-conductance. The turn-on process and the turn-off process are illustrated in detail, and equivalent circuits are derived and solved for each switching transition. The proposed analytical model is more accurate and matches better with experimental results than other analytical models. Note that switching losses calculated based on experiments are imprecise, because the energy of the junction capacitances is not properly disposed. Finally, the proposed analytical model is utilized to account for the effects of parasitic elements on the switching performance of a SiC MOSFET, and the circuit design rules for high frequency circuits are given.

Key words: Analytical model, Parasitic elements, SiC MOSFET, Switching loss, Switching performance

I. INTRODUCTION

The silicon carbide (SiC) MOSFET is a promising candidate for next generation power devices. It is featured by much higher blocking voltages, lower on-state resistance, higher switching speeds and higher thermal conductivity than conventional silicon (Si) devices [1]-[5]. In addition, a SiC MOSFET is capability of operation under higher density power conversion [6]. The switching frequency has been continuously pushed up to the megahertz range to reduce the size of the passive components [7], [8]. However, as the switching loss increases and the effects of parasitic elements on the switching performance become intensified, there is a further increase in the switching frequency. In order to take full advantage of a SiC MOSFET, it is necessary to estimate the switching loss and to analyze the effects of the parasitic elements on the switching performance of the SiC MOSFET for optimization.

Investigation into this issue can be classified into three categories. One way to study this is by measuring experimental switching waveforms [9]-[14]. Some device manufactures provide the switching energy dissipation in a datasheet by capturing the experimental switching waveforms in a double-pulse-test circuit. However, this method needs oscilloscope probes that have a sufficient bandwidth to insure the high fidelity of the switching waveforms, especially for testing high switching-speed devices [15], [16]. On the other hand, the experimental switching waveforms are impacted by the parasitic inductances of particular PCB traces and the characteristics of free-wheeling diodes. Therefore, switching loss based on different experimental platforms may be different. Not only that, this method only provides experimental switching waveforms under the influence of parasitic elements. It does not provide explanations of the influence mechanism of the parasitic elements through measurement results.

In [17]-[20], a method for making simulation models, such as pspice models or saber models, is presented. For SiC MOSFETs, Cree has published LTspice models with the parasitic inductances in the package. The simulation model can be combined with an external circuit including the parasitic inductances of the PCB traces to calculate the switching loss and to obtain the switching waveforms under the influence of the parasitic elements. However, like the experimental method, this simulation method does not give the influence mechanism.

Analytical models are set up based on the mathematical methods in [21]-[30]. The piecewise linear model is the most

Manuscript received Jun. 3, 2015; accepted Aug. 10, 2015
Recommended for publication by Associate Editor Jee-Hoon Jung.
†Corresponding Author: 12117352@bjtu.edu.cn
Tel: +86-10-51684911-15, Fax: +86-10-51684029, Beijing Jiaotong University
*School of Electrical and Engineering, Beijing Jiaotong University, China

simple and popular analytical model [21], [22]. However, the parasitic inductances and junction capacitances are not taken into consideration. In [32] and [33], it is shown that the nonlinear junction capacitances of power devices are critical for the switching transition. As a result they should be fully considered in the modeling and switching transient analysis, especially for high-frequency applications. In addition, the parasitic inductances are also very significant for the switching transient analysis in high-frequency applications [23]. Therefore, the results of the piecewise linear model cannot match well with the experimental results. In [23]-[30], analytical models considering the parasitic inductances and junction capacitances are presented. The equivalent circuits for each switching transition can be derived and solved. Then, the switching waveforms and switching loss can be calculated, and the effects of the parasitic elements on the switching performance can be analyzed. Some analytical models are designed to predict the switching performance of low-voltage MOSFETs [24]-[29]. The switching processes of a SiC MOSFET, which is a high voltage device, are different from the low-voltage devices usually operating at voltages lower than 40V. The drain-source voltage v_{DS} of low-voltage devices drops to 0V before the drain current i_D reaches I_o during the turn-on transition, and i_D can reach 0A before v_{DS} reaches V_{DC} during the turn-off transition [25], [31]. In general, these conditions will not happen to high voltage devices. The analytical models from [23] and [30] are for high voltage devices. In [23] and [30], the junction capacitances and trans-conductance are treated as constants, and the nonlinearity of these two elements is not considered. Therefore, these analytical models are also imprecise. In [30], the common source parasitic inductance is not considered, which is shared by the power loop and the gate loop. It plays a different role with the power loop parasitic inductances. In addition, [31] shows that the switching loss of a Cascode GaN HEMT, which are derived from terminal waveforms based on experiments, are imprecise. This is due to the fact that the energy in the junction capacitances is not dealt with well. However, this issue is not addressed or analyzed in any of the studies concerning SiC MOSFETs.

The objective of this paper is to estimate the switching loss and analyze the effects of the parasitic elements on the switching performance of a SiC MOSFET with an improved analytical model. The proposed analytical model considers the parasitic inductances, the nonlinearity of the junction capacitances and the nonlinearity of trans-conductance. The switching processes are illustrated in detail, and the equivalent circuits are derived and solved during the switching transition. This paper is organized as follows. The proposed analytical model is established in Section II. Verification of the proposed analytical model of a SiC MOSFET is in Section III. The effects of the parasitic elements on the switching performance of a SiC MOSFET are illustrated in Section IV. Some conclusions are given in Section V.

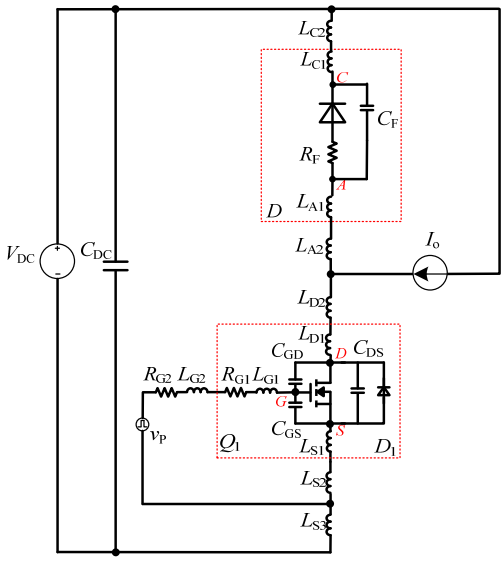


Fig. 1. Double-pulse-test circuit considering parasitic elements.

II. Analysis of Switching Processes

To analyze the switching processes of a SiC MOSFET, a double-pulse-test circuit is used as an example. The employed double-pulse-test circuit considering the parasitic elements is shown in Fig. 1. The input voltage source V_{DC} is constant, and the output current I_o is constant. The parasitic elements in the package of the SiC MOSFET Q_1 are the gate-source capacitance C_{GS}, the gate-drain capacitance C_{GD}, the drain-source capacitance C_{DS}, the gate inductance L_{G1}, the drain inductance L_{D1}, the source inductance L_{S1}, and the internal gate drive resistance R_{G1}. The parasitic elements in the package of the freewheeling diode D are the junction capacitance C_F, the cathode inductance L_{C1}, the anode inductance L_{A1}, and the on-state resistance R_F. A SiC JBS diode is employed as the freewheeling diode, which does not have the reverse recovery charge Q_{rr}. L_{C2}, L_{A2}, L_{G2}, L_{D2}, L_{S2}, and L_{S3} represent the interconnection parasitic inductances of the PCB traces. In all of the parasitic inductances, L_{S1} and L_{S2} are the common source inductances shared by the power loop and the gate drive loop. R_{G2} represents the external gate drive resistance. The gate signal v_P flips between V_{SS} and V_{GS}, and V_{SS} is a negative value. The circuit in Fig. 1 is also suitable for analyzing the device performance during the switching transitions for other bridge configuration-based topologies, such as boost, buck-boost, half bridge, and full bridge.

A. Turn-on Switching Transition

Before Q_1 is turned on, the output current I_o flows through D, and the input voltage source V_{DC} is applied to Q_1. The turn-on switching transition can be divided into four stages, which are analyzed as follows. The complete switching waveforms are shown in the next section.

1) Stage 1, Turn-on Delay Time: When V_{GS} is applied, the gate current i_G charges C_{GS} and C_{GD}. C_{GS} is much larger than C_{GD}. Thus, the majority of the gate current charges C_{GS}. Since the gate-source voltage v_{GS} does not reach the threshold voltage V_{th}, Q_1 is cut-off and almost no drain current flows into Q_1. The equivalent circuit of this stage is shown in Fig. 2(a). During this stage, the circuit equations can be expressed as:

$$v_{GS} = V_{GS} - R_G i_G - (L_G + L_{CS})\frac{di_G}{dt} \tag{1}$$

$$i_G = C_{GS}\frac{dv_{GS}}{dt} \tag{2}$$

where R_G=R_{G1}+R_{G2}, L_G=L_{G1}+L_{G2}, and L_{CS}=L_{S1}+L_{S2}. The gate-source voltage v_{GS} can be solved by the iterative method presented concretely in the next stage, and the coefficient matrixes are shown in Appendix.

This stage ends when v_{GS} reaches V_{th}. Since Q_1 is not activated, there is no switching loss during this stage.

2) Stage 2, Current Rising Time: When v_{GS} reaches V_{th}, the channel of Q_1 conducts, and the channel current i_{CH}, which is controlled by v_{GS}, increases. During this stage, I_o transfers from D to Q_1. The rising drain current i_D and the falling forward current i_F induce voltage drops across the parasitic inductances. This leads to C_{GD} and C_{DS} discharging through the channel of Q_1, and the drain-source voltage v_{DS} falling. The equivalent circuit is shown in Fig. 2(b), where Q_1 is modelled as a dependent current source controlled by v_{GS}. The expression of this source is given by:

$$i_{CH} = g_f(v_{GS} - V_{th}) \tag{3}$$

where g_f is the trans-conductance of Q_1. The circuit equations can be expressed as:

$$v_{GS} = V_{GS} - R_G i_G - L_G\frac{di_G}{dt} - L_{CS}\left(\frac{di_D}{dt} + \frac{di_G}{dt}\right) \tag{4}$$

$$i_G = C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{5}$$

$$v_{DS} = V_{DC} - v_F - L_P\frac{di_D}{dt} - L_{CS}\frac{di_G}{dt} \tag{6}$$

$$i_D = g_f(v_{GS} - V_{th}) + C_{DS}\frac{dv_{DS}}{dt} - C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{7}$$

$$v_F = R_F(i_D - I_o) - V_F \tag{8}$$

where L_P is the sum of the power loop parasitic inductances, L_P=L_{C1}+L_{C2}+L_{A1}+L_{A2}+L_{D1}+L_{D2}+L_{S1}+L_{S2}+L_{S3}, and V_F is the forward voltage of D.

Since there are four independent state variables in Equs. (4)-(8), it is difficult to derive the time domain solutions without simplification. In order to enhance the accuracy of this analytical model, the iterative method is employed. Equs. (4)-(8) are transformed into:

$$\frac{d\boldsymbol{X}}{dt} = \boldsymbol{A}\cdot\boldsymbol{X} + \boldsymbol{B} \tag{9}$$

where $\boldsymbol{X}$=[i_G v_{GS} i_D v_{DS} v_F]^T, and $\boldsymbol{A}$ and $\boldsymbol{B}$ are the coefficient matrixes, which are shown in the Appendix. Afterwards, Equs. (4)–(8) can be solved according to the following formula:

$$\boldsymbol{X}(n\Delta t) = \boldsymbol{X}[(n-1)\Delta t] + \{\boldsymbol{A}\cdot\boldsymbol{X}[(n-1)\Delta t] + \boldsymbol{B}\}\Delta t \tag{10}$$

where n=1, 2, 3…, and Δt is the calculation time step. All of the variables can be solved as Equ. (10).

This stage ends when the drain current i_D reaches I_o. During this stage, the channel of Q_1 conducts, and a portion of the energy stored in C_{GD} and C_{DS} is dissipated through the channel. Therefore, the turn-on loss can be calculated as:

$$P_{sw\_on\_s2} = \int_{t_{n1}}^{t_{n2}} v_{DS}\cdot i_{CH}\,dt \tag{11}$$

where, t_{n1} is the time of stage 1, and t_{n2} is the time of stage 1 and stage 2.

3) Stage 3, Voltage Falling Time: When i_D reaches I_o, D is able to block the voltage, Q_1 need to assume I_o, and the additional current is charging C_F of the freewheeling diode. v_{DS} eventually decreases and C_{GD} and C_{DS} continue to discharge through the channel of Q_1. i_D may have a ringing because of oscillations between L_P and C_F. The equivalent circuit is shown in Fig. 2(c), and the circuit equations different from stage 2 can be expressed as:

$$\frac{dv_F}{dt} = \frac{i_D - I_o}{C_F} \tag{12}$$

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix.

This stage ends when v_{DS} decreases to i_D·R_{on}, where R_{on} is the on-state resistance of Q_1. At this point, the drain-source voltage and drain current transition are over. During this stage, the turn-on loss is the same as that of the previous stage, and it can be calculated as:

$$P_{sw\_on\_s3} = \int_{t_{n2}}^{t_{n3}} v_{DS}\cdot i_{CH}\,dt \tag{13}$$

where t_{n3} is the time of stage 1, stage 2, and stage 3.

4) Stage 4, Gate Remaining Charging Time: Once v_{DS} reaches i_D·R_{on}, v_{GS} continues to increase until it reaches V_{GS}. The channel current i_{CH} is no longer controlled by v_{GS}, and ultimately goes back to I_o. The equivalent circuit is shown in Fig. 2(d), where Q_1 is modelled as the on-state resistance. The circuit equations different from stage 2 and stage 3 can be expressed as:

$$i_D = \frac{v_{DS}}{R_{on}} + C_{DS}\frac{dv_{DS}}{dt} - C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{14}$$

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix.

During this stage, the drain-source voltage and the drain current are almost steady. Therefore, there is no turn-on loss.

B. Turn-off Switching Transition

Before Q_1 is turned off, the output current I_o flows through Q_1, and the input voltage source V_{DC} is applied to D. The turn-off switching transition can be divided into four stages, which are analyzed as follows. The complete waveforms are shown in the next Section.

1) Stage 1, Turn-off Delay Time: When V_{SS} is applied, C_{GS}

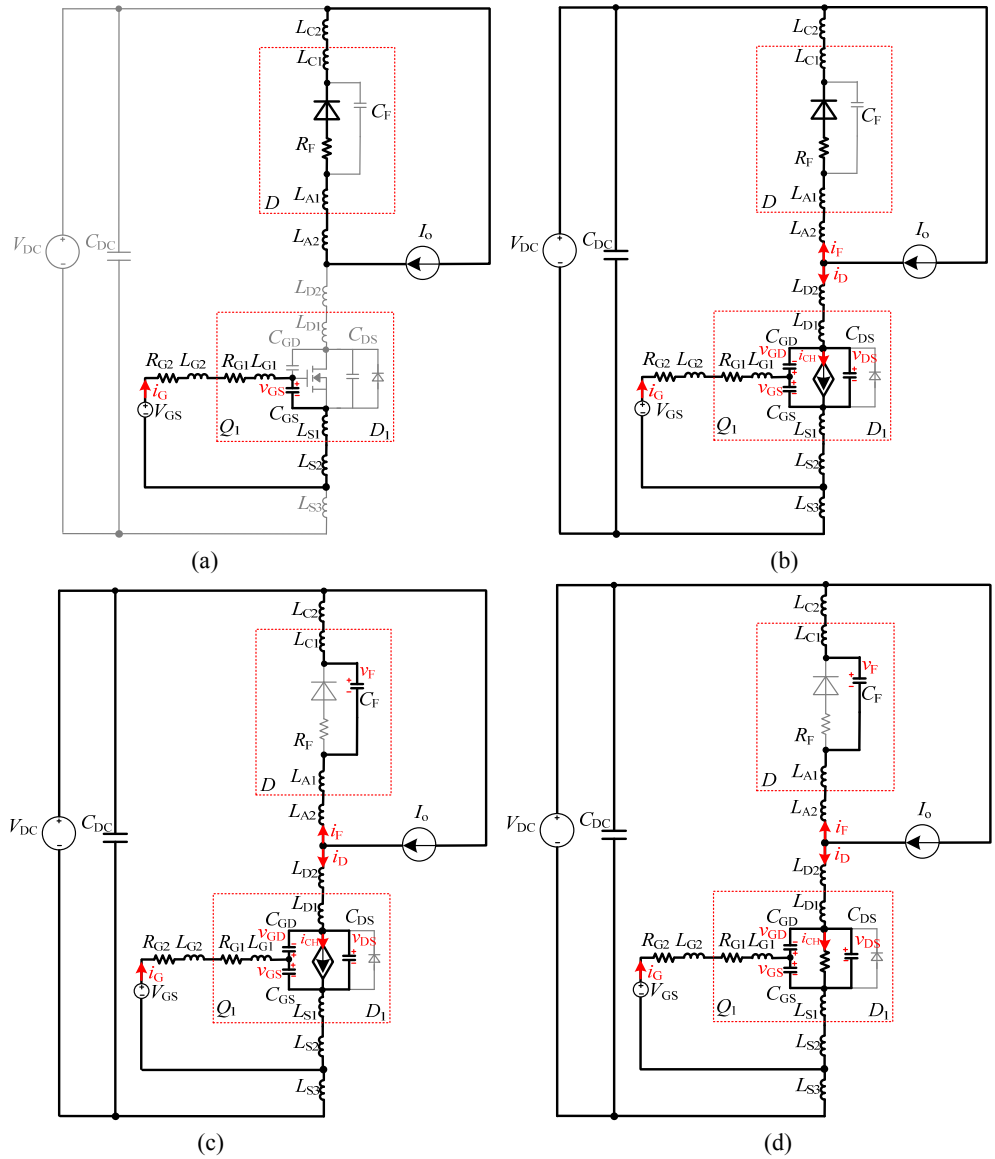


Fig. 2. Equivalent circuits for the turn-on transition. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4.

and C_{GD} discharge, and v_{GS} decreases. However, when Q_1 is still in the on-state, I_o keeps flowing through the channel of Q_1. The equivalent circuit of this stage is shown in Fig. 3(a), and the circuit equations can be expressed as:

$$v_{GS} = V_{ss} - R_G i_G - (L_G + L_{CS})\frac{di_G}{dt} \tag{15}$$

$$i_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \tag{16}$$

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix.

This stage ends when v_{GS} reaches V_{mil}, which is given as Equ. (17). During this stage, Q_1 is still turned on. As a result, there is no turn-off loss.

$$V_{mil} = \frac{I_o}{g_f} + V_{th} \tag{17}$$

2) Stage 2, Voltage Rising Time: During this stage, v_{DS} increases, and i_D charges C_{GD} and C_{DS}. i_{CH} decreases because C_{GD} and C_{DS} need the charging current, and C_F need to release energy. Therefore, v_{GS} continues to decrease due to its dependent relation with i_{CH}. The equivalent circuit is shown in Fig. 3(b), where Q_1 is modelled as a dependent current source. The circuit equations can be expressed as:

$$v_{GS} = V_{ss} - R_G i_G - L_G\frac{di_G}{dt} - L_{CS}\left(\frac{di_D}{dt} + \frac{di_G}{dt}\right) \tag{18}$$

$$i_G = C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{19}$$

$$v_{DS} = V_{DC} - v_F - L_P\frac{di_D}{dt} - L_{CS}\frac{di_G}{dt} \tag{20}$$

$$i_D = g_f(v_{GS} - V_{th}) + C_{DS}\frac{dv_{DS}}{dt} - C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{21}$$

$$\frac{dv_F}{dt} = \frac{i_D - I_o}{C_F} \tag{22}$$

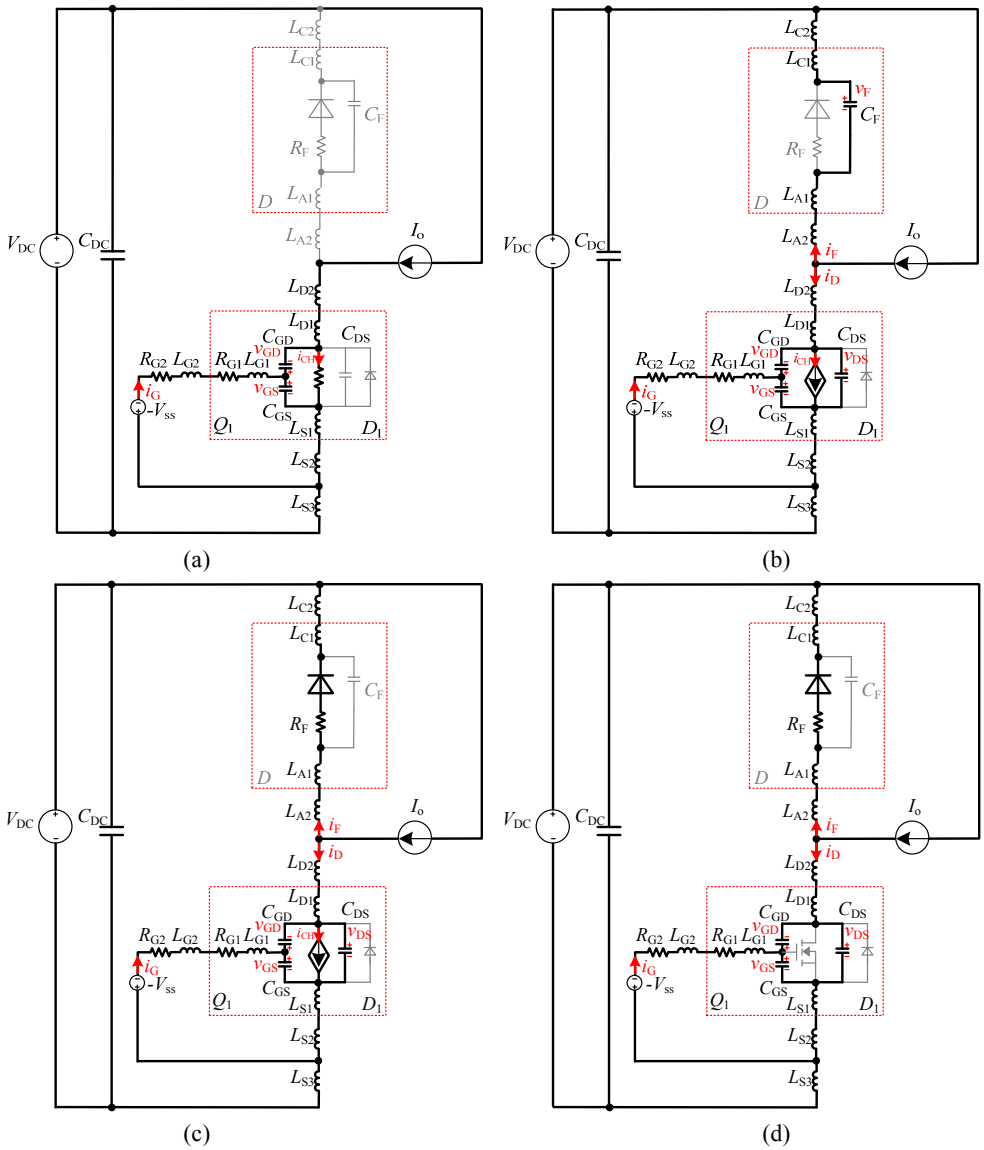


Fig. 3. Equivalent circuits for the turn-off transition (a) stage 1, (b) stage 2, (c) stage 3, and (d) stage 4.

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix.

This stage ends when the forward voltage v_F of D decreases to $-V_F$. Then, D is in the on-state. During this stage, the turn-off loss of Q_1 can be calculated as:

$$P_{sw\_off\_s2} = \int_{t_{f1}}^{t_{f2}} v_{DS} \cdot i_{CH} dt \tag{23}$$

where, t_{f1} is the time of stage 1, and t_{f2} is the time of stage 1 and stage 2.

3) Stage 3, Current Falling Time: During this stage, v_{GS} and i_{CH} decrease. v_{DS} continues to increase, and C_{GD} and C_{DS} are charged. The rapidly changing currents i_D and i_F induce voltage drops across the parasitic inductances, which eventually incurs a voltage overshoot on v_{DS}. The equivalent circuit is shown in Fig. 3(c), and the circuit equations different from stage 2 can be expressed as:

$$v_F = R_F(i_D - I_o) - V_F \tag{24}$$

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix.

This stage ends when i_{CH} reaches zero, and v_{GS} reaches V_{th}. During this stage, the turn-off loss can be calculated as:

$$P_{sw\_off\_s3} = \int_{t_{f2}}^{t_{f3}} v_{DS} \cdot i_{CH} dt \tag{25}$$

where, t_{f3} is the time of stage 1, stage 2, and stage 3.

4) Stage 4, Gate Remaining Discharging Time: When v_{GS} drops below V_{th}, the channel of Q_1 is totally shut down. Then v_{GS} continues to decrease until it reaches V_{ss}. During this stage, the drain-source voltage and the drain current have a ringing because the parasitic inductances oscillate with C_{GD} and C_{DS}. The equivalent circuit is shown in Fig. 3(d), and the circuit equations different from stage 2 and stage 3 can be expressed as:

$$i_D(t) = C_{DS}\frac{dv_{DS}}{dt} - C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} \tag{26}$$

The iterative method is also employed in this stage, and the coefficient matrixes are shown in the Appendix. As the ringing dissipation is very small and can be neglected, this stage has no turn-off loss.

III. Verification of the Analytical Model

In this part, experiments based on a double-pulse-test circuit are carried out to validate the proposed analytical model. In the double-pulse-test circuit, the device under examination is a 1200V SiC MOSFET C2M0080120D from CREE, Inc. The freewheeling diode is a 1200V SiC JBS diode C4D20120A with no reverse recovery charge. Note that the proposed analytical model is suitable for not only 1200V SiC MOSFETs from CREE, Inc., but for high voltage SiC MOSFETs from other companies as well.

A. Extraction of Key Parameters

In the proposed analytical model, the key parameters are the parasitic inductances, the junction capacitances and the trans-conductance, the accuracy of which influences the accuracy of the analytical model.

As packaging technology develops, L_{G1}, L_{S1}, and L_{D1} in the package of devices can be minimized to as low as the nH level. In addition, the extraction of the interconnection parasitic inductances of the PCB traces is implemented by an Ansoft Q3D Extractor finite-element analysis (FEA) simulation [34], [35]. Table I shows the parasitic inductances in the proposed analytical model.

The device manufacturer provides the curves of the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse capacitance C_{rss} in the datasheet. The relations between the capacitances given in the datasheet and the junction capacitances are $C_{iss}=C_{GS}+C_{GD}$, $C_{oss}=C_{GD}+C_{DS}$, and $C_{rss}=C_{GD}$. Therefore, junction capacitances can be extracted from the datasheet. Obviously, C_{oss} and C_{rss} change with an applied voltage. According to [26], [32], and [33], the nonlinearity of the capacitance versus the voltage can be modelled as:

$$C(v)=\frac{C_0}{(1+\frac{v}{k})^{\lambda}} \tag{27}$$

where k and λ are the two adjustment parameters extracted from the capacitance curves in the datasheet, v is the applied voltage, and C_0 is the 0 V capacitance value.

Nevertheless, Equ. (27) cannot accurately fit the capacitance curves, especially the inflection point. Thus, the piecewise fitting method is employed for modelling. The values of C_{oss} and C_{rss} for the SiC MOSFET C2M0080120D can be expressed as Equs. (28)- (29).

Fig. 4 shows a comparison between the capacitance curves provided by the datasheet and the piecewise fitting. This figure shows that the capacitance curves under the piecewise fitting method match well with the datasheet. In addition, the junction capacitance C_F of the freewheeling diode is also nonlinear, and it can be extracted based on the piecewise fitting method.

TABLE I
Parasitic Inductances in the Proposed Analytical Model

L_{C1}	5nH
L_{A1}	5nH
L_{G1}	6nH
L_{S1}	13nH
L_{D1}	10nH
L_{C2}	67nH
L_{A2}	39nH
L_{G2}	17nH
L_{S2}	0nH
L_{S3}	59nH
L_{D2}	47nH

The device manufacture also provides the transconductance characteristic curve in the datasheet. The transconductance g_f represents the incremental change of i_{CH} over an incremental change of v_{GS}. g_f is also nonlinear and can be extracted according to the transconductance characteristic curve. The transconductance characteristic curve of a SiC MOSFET C2M0080120D can be expressed based on the piecewise fitting method. Fig. 5 shows a comparison between the transconductance characteristic curve provided by the datasheet and the piecewise fitting.

$$C_{oss}=\begin{cases}\dfrac{1450}{(1+\frac{v_{DS}}{5})^{0.8}} & 0<v_{DS}\le 35\\ \dfrac{1450}{(1+\frac{v_{DS}}{1.3})^{0.5}} & 35<v_{DS}\le 400\end{cases} \tag{28}$$

$$C_{rss}=\begin{cases}\dfrac{400}{(1+\frac{v_{DS}}{300})^{40}} & 0<v_{DS}\le 20\\ \dfrac{400}{(1+\frac{v_{DS}}{0.8})^{0.8}} & 20<v_{DS}\le 35\\ \dfrac{400}{(1+\frac{v_{DS}}{0.09})^{0.49}} & 35<v_{DS}\le 400\end{cases} \tag{29}$$

B. Verification

In this part, the experimental results of the drain current i_D, the drain-source voltage v_{DS}, and the switching loss p are recorded to compare with the analytical model. Fig. 6 shows the double-pulse-test hardware setup. Table II shows the critical test equipment for the experimental verification. Because of the high switching speed of the SiC MOSFET, the probes should have sufficient bandwidth to capture the fast rising and falling edges of the switching waveforms with high fidelity. As stated in [36] and [37], the equivalent frequency of

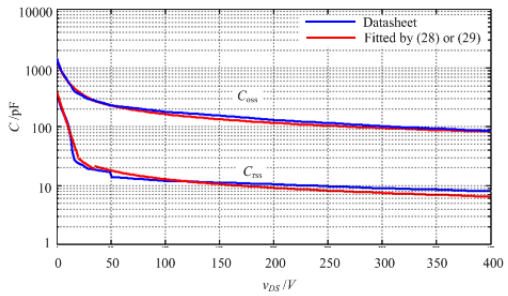


Fig. 4. Capacitance curves of SiC MOSFET C2M0080120D.

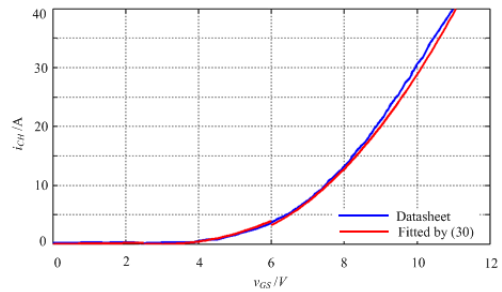


Fig. 5. Transconductance characteristic curve of SiC MOSFET C2M0080120D.

a rising/falling edge can be approximated as:

$$f_{bd} = \frac{0.25}{\min(t_r, t_f)} \tag{30}$$

where t_r is the rising time of the switching waveform, and t_f is the falling time of the switching waveform. In this experiment, the rising/falling edge of the captured waveform may less than 25ns. Therefore, the equivalent frequency is more than 10MHz. For the sake of accuracy, the bandwidth of the test equipment should be higher than ten times the equivalent frequency of the measured waveform [36], [37]. The test equipment shown in Table II meets this bandwidth requirement. Table III shows the initial parameters of the proposed analytical model.

Fig. 7 shows comparisons between the switching waveforms provided by the experiment, the proposed analytical model, the analytical model in [23], and the analytical model in [30]. Table IV shows a switching time comparison during the switching transition. It is apparent that the proposed analytical model matches better with the experimental results (in terms of the voltage slope, the current slope, the voltage spike, and the current spike) than analytical models in [23] and [30]. It is easy to see that the oscillation frequency and oscillation amplitude in the voltage and current provided by the proposed analytical model are different from those of the experimental results. This is because the junction capacitances and trans-conductance of all the devices are difficult to maintain a high consistency with the data in the datasheet. In addition, the parasitic inductances include the self-inductances and the mutual-inductances, which are influenced by several factors, including the conductor position, current direction, and oscillation frequency [34], [35]. However, the current directions and oscillation frequency are difficult to predict accurately when conducting a FEA simulation.

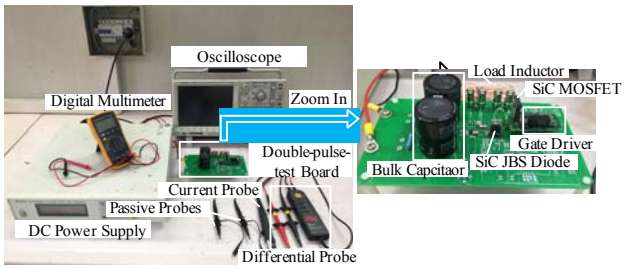


Fig. 6. Double-pulse-test hardware setup.

TABLE II
CRITICAL TEST EQUIPMENT FOR EXPERIMENTAL VERIFICATION

Type	Model	Bandwidth
Oscilloscope	Tektronix DPO4054B	500M
Differential probe	Tektronix P6139B	500M
Passive probe	Tektronix P2220	200M
Current probe	Tektronix TCP0030A	120M

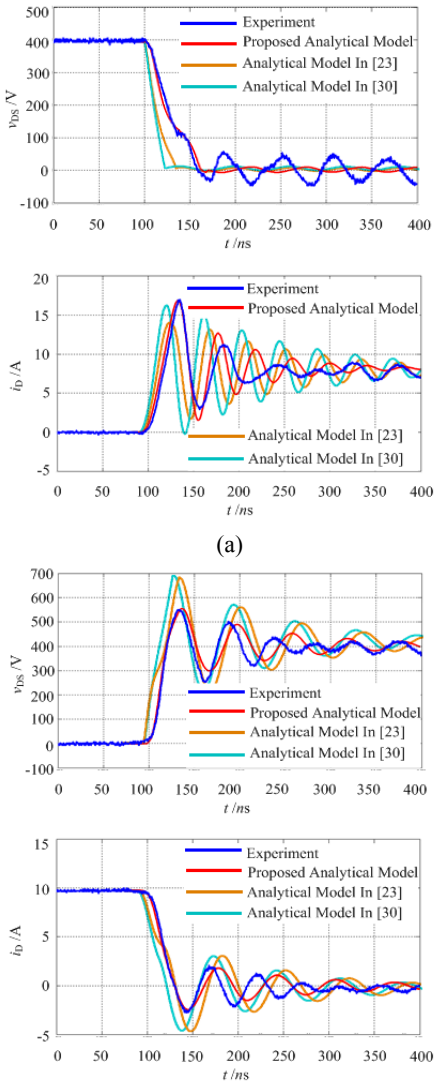
TABLE III
INITIAL PARAMETERS OF THE PROPOSED ANALYTICAL MODEL

V_{DC}	400V
V_{GS}	19V
V_{SS}	-2V
V_{th}	2.5V
R_{G1}	5Ω
R_{G2}	20Ω
V_F	0.9V
R_F	50mΩ

The turn-on loss and the turn-off loss are shown in Fig. 8. The switching loss calculated based on experimental switching waveforms by integrating i_D and v_{DS} is called p_e. The switching loss calculated based on the proposed analytical model by integrating i_D and v_{DS} is called p_{m1}. The switching loss calculated based on the proposed analytical model by integrating i_{CH} and v_{DS} is called p_{m2}. As shown in Fig. 8(a), p_{m2} is more than the other calculated results. This is due to the fact that the energy stored in C_{GD} and C_{DS} is dissipated by the channel during the turn-on transition, which is ignored by p_e and p_{m1}. As shown in Fig. 8(b), p_{m2} is less than the other calculated results. This is due to the fact that some of i_D charges C_{GD} and C_{DS} during the turn-off transition, and the energy stored in the junction capacitances is embraced by p_e and p_{m1}.

IV. EFFECTS OF PARASITIC ELEMENTS ON THE SWITCHING PERFORMANCE

The switching processes of a SiC MOSFET are modeled in detail, and the proposed analytical model is verified effectively in the previous section. Therefore, the effects of the parasitic elements on the switching performance can be predicted according to the proposed analytical model. The effects of the gate drive resistance R_G, the gate inductance L_G, the common

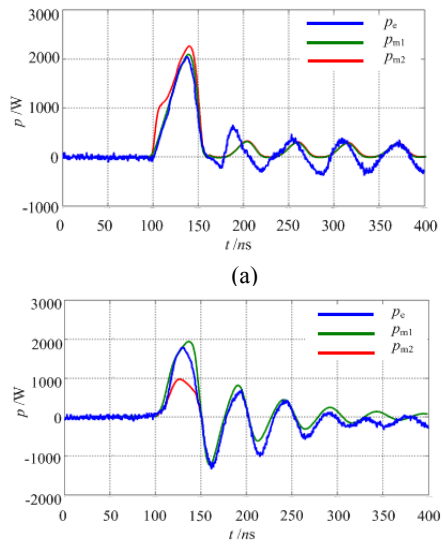


(a)

(b)

Fig. 7. Switching waveforms of SiC MOSFET C2M0080120D provided by the experiment, the proposed analytical model, the analytical model in [23] and the analytical model in [30] (a) turn-on waveforms, and (b) turn-off waveforms.
(Remark: According to the datasheet of SiC MOSFET C2M0080120D, in the analytical model in [23] and [30], the transconductance g_f is set 9.8, and the junction capacitances are set as follows, C_{GD}=100pF and C_{DS}=300pF when $v_{GS}>V_{th}$ and $v_{DS}<v_{GS}-V_{th}$, C_{GD}=10pF and C_{DS}=90pF when $v_{GS}<V_{th}$, or $v_{GS}>V_{th}$ and $v_{DS}>v_{GS}-V_{th}$. And L_{CS} is set 0nH in the analytical model in [30])

source inductance L_{CS}, and the power loop inductance L_P are analyzed. These parasitic elements can be changed within reasonable ranges of the actual conditions. Nevertheless, the effects of the junction capacitances are not analyzed because they are in the package of device and cannot be changed. In order to interpret the effects of the parasitic elements directly by sensors, the switching waveforms of the proposed analytical model with varied parasitic elements are plotted. It should be noted that one parameter is studied, while the other parameters are keep invariable and at their initial values.



(a)

(b)

Fig. 8. Switching loss of SiC MOSFET C2M0080120D provided by the experiment and the proposed analytical model (a) turn-on loss, and (b) turn-off loss.

TABLE IV
SWITCHING TIME COMPARISON DURING SWITCHING TRANSITION

	Turn-on transition		Turn-off transition	
	Current rising time	**Voltage falling time**	**Voltage rising time**	**Current falling time**
Experiment	22ns	41ns	23ns	14ns
Proposed model	21ns	44ns	22ns	16ns
Model in [23]	15ns	23ns	26ns	16ns
Model in [30]	14ns	12ns	18ns	9ns

A. Gate Drive Resistance R_G

The switching waveforms of the proposed analytical model with varied values of R_G are shown in Fig. 9. With a large R_G, the switching speed is slowed down. The voltage stress is the voltage drops across the parasitic inductances induced by the falling current, and the current stress is caused by the charging current of C_F of the freewheeling diode, which is related to the current slew rate and the parasitic inductances. Therefore, the device stress is reduced with an increasing R_G. The switching loss is positively correlated to the switching time and the values of the voltage and current. In addition, it is negatively correlated to the switching speed. The increase in R_G leads to an increase in the switching loss. The turn-on loss is due to the increase in the switching time, the decrease in the voltage and current slew rates, and the decrease in the voltage drops across the parasitic inductances. The turn-off loss is due to the increase in the switching time and the decrease in the voltage and current slew rates which outweigh the reduction of the voltage and current stresses.

B. Gate Inductance L_G

The switching waveforms of the proposed analytical model with varied values of L_G are shown in Fig. 10. It can be seen that they almost overlap. This proves that L_G has little effect on the switching speed, device stress, and switching loss. In fact, according to the circuit design guidelines, L_G should be kept small to minimize the oscillations in the gate drive circuit.

C. Common Source Inductance L_{CS}

The switching waveforms of the proposed analytical model with varied values of L_{CS} are shown in Fig. 11. L_{CS} is the sum of the common source inductances L_{S1} and L_{S2}. This shows that a large L_{CS} can reduce the current slew rate. However, the effect on the voltage slew rate is inconspicuous. L_{CS} is shared by the power loop and the gate drive loop. In addition, the changing current will generate the voltage drop across L_{CS} opposing real intention of the gate drive stage. Therefore, the effect of L_{CS} on the current slew rate is similar to R_G. According to Fig. 11, L_{CS} decreases the device stress by reducing the current slew rate. The switching loss increases with L_{CS}. This is due to the same reason as R_G.

D. Power Loop Inductance L_P

L_P lumps all of the parasitic inductances (L_{C1}, L_{C2}, L_{A1}, L_{A2}, L_{S1}, L_{S2}, L_{S3}, L_{D1}, and L_{D2}) along the power loop. The switching waveforms of the proposed analytical model with varied values of L_P are shown in Fig. 12. The effect of L_P on the switching speed is similar to L_{CS}, which has been given. However, the effect of L_P on the device stress is opposite to L_{CS}. L_P increases the device stress so that the increase in L_P outweighs the reduction in the current slew rate. The turn-on loss decreases with an increasing L_P, because the decrease in voltage drops across the parasitic inductances outweighs the other factors. The turn-off loss increases with a large L_P due to the decrease in the current slew rate and the increase in the voltage stress.

E. Summary

Based on the preceding discussion, the effects of the parasitic elements on the switching performance can be summarized as follows.

With respect to the switching speed, an increase in R_G can slow down the switching speed. L_{CS} or L_P can slow down the current slew rate. However, they have little effect on the voltage slew rate. Regarding to the device stress, R_G and L_{CS} can reduce the device stress. However, L_P has the opposite reaction. For the switching loss, R_G and L_{CS} can add to the switching loss. Nevertheless, L_P decreases the turn-on loss and increases the turn-off loss.

Note that L_G has little effect on the switching speed, device stress and switching loss. However, L_G may cause oscillations in the gate drive circuit.

After a comprehensive assessment of the effects of the parasitic elements, when initially proceeding the PCB circuit design, L_{CS} should be minimized to get a low switching loss, L_P should be minimized to get a low device stress and a low

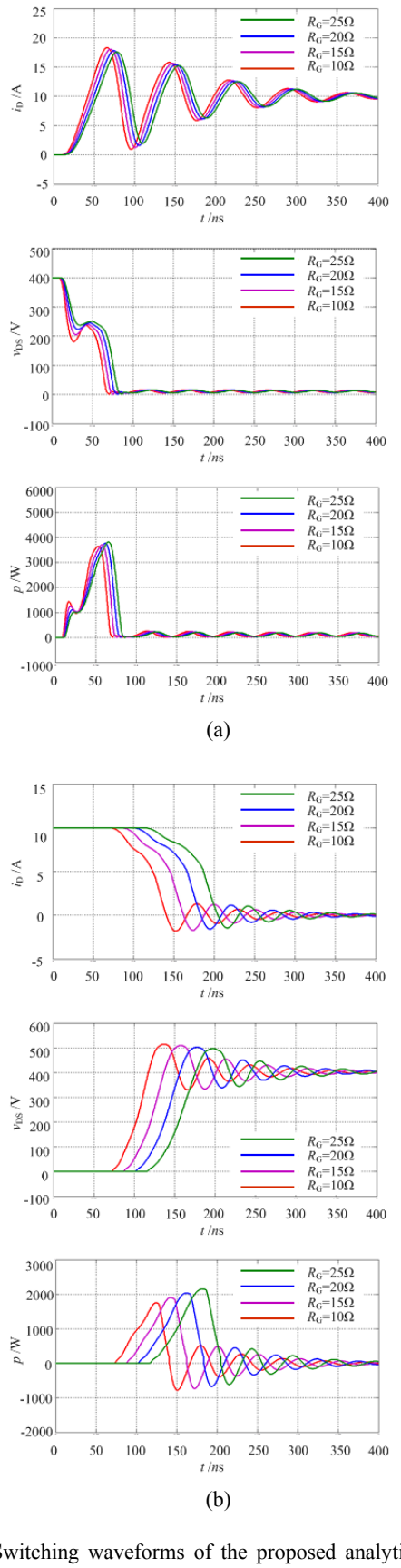
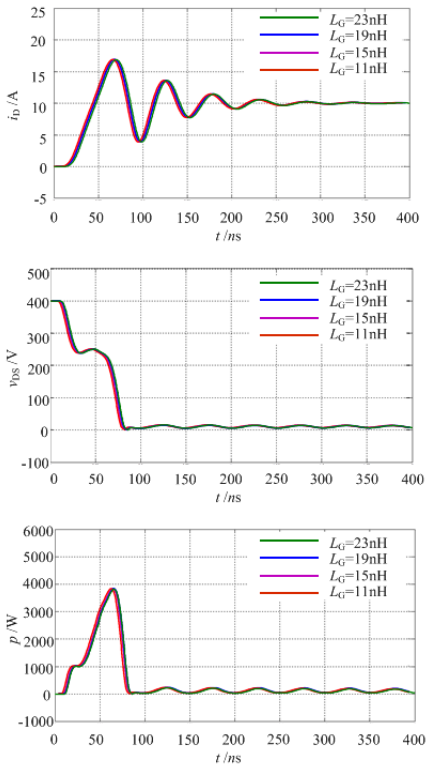
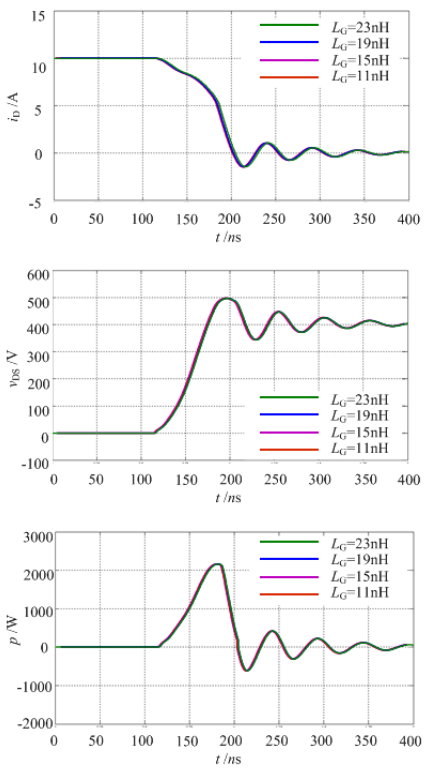


Fig. 9. Switching waveforms of the proposed analytical model with varied R_G (a) turn-on waveforms, and (b) turn-off waveforms.

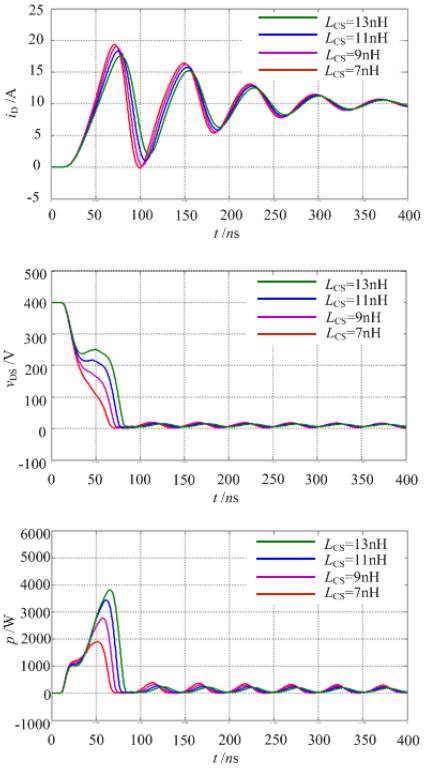


(a)

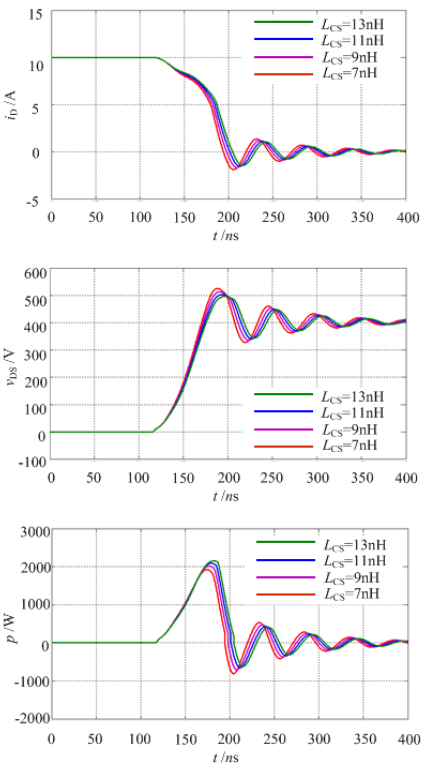


(b)

Fig. 10. Switching waveforms of the proposed analytical model with varied L_G (a) turn-on waveforms, and (b) turn-off waveform.

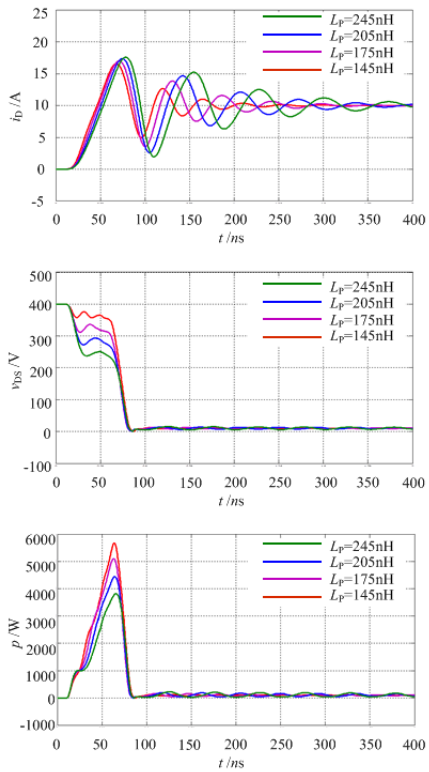


(a)

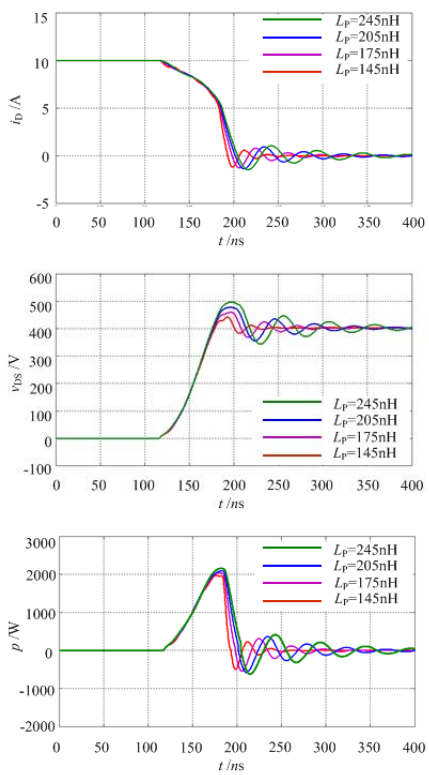


(b)

Fig. 11. Switching waveforms of the proposed analytical model with varied L_{CS} (a) turn-on waveforms, and (b) turn-off waveforms.



(a)



(b)

Fig. 12. Switching waveforms of the proposed analytical model with varied L_P (a) turn-on waveforms, and (b) turn-off waveforms.

turn-off loss, and R_G should be chosen at a reasonable value to mitigate the conflict between the switching loss and the device stress.

V. CONCLUSION

This paper presents an improved analytical model to estimate switching loss and analyze the effects of parasitic elements on the switching performance of a SiC MOSFET. The proposed analytical model takes the parasitic inductances, the nonlinearity of the junction capacitances, and the nonlinearity of the trans-conductance into account. The proposed analytical model is more accurate and matches better with experimental results than other analytical models. The proposed analytical model with varied parasitic elements is compared to account for the effects of parasitic elements on the switching performance of a SiC MOSFET.

In this paper, the following points should be noted:

1): The switching loss calculated based on an experiment is imprecise. The experimental results neglect the energy released by C_{GD} and C_{DS} during the turn-on transition and embrace the energy stored in C_{GD} and C_{DS} during the turn-off transition.

2): When initially proceeding with the PCB circuit design, L_{CS} should be minimized to get a low switching loss, L_P should be minimized to get a low device stress and a low turn-off loss, and R_G can be chosen to achieve a better compromise between the device stress and the switching loss.

APPENDIX

A. Turn-on Switching Transition

The coefficient matrixes of stage 1 are as follows:

$$\boldsymbol{A}=\begin{bmatrix} \frac{-R_G}{L_G+L_S} & \frac{-1}{L_G+L_S} & 0 & 0 & 0 \\ \frac{1}{C_{GS}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{31}$$

$$\boldsymbol{B}=\begin{bmatrix} \frac{V_{GS}}{L_G+L_S} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{32}$$

The coefficient matrixes of stage 2 are as follows:

$$\boldsymbol{A}=\begin{bmatrix} \frac{-R_G}{\alpha} & \frac{-1}{\alpha} & \frac{L_S R_F}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0 \\ \frac{C_{oss}C_{iss}}{\beta} & \frac{-g_f C_{GD}C_{iss}}{\beta} & \frac{C_{GD}C_{iss}}{\beta} & 0 & 0 \\ \frac{L_S R_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & \frac{-(L_G+L_S)R_F}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha} & 0 \\ \frac{C_{GD}C_{iss}}{\beta} & \frac{-g_f C_{iss}^2}{\beta} & \frac{C_{iss}^2}{\beta} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{33}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{L_PV_{GS}-L_S(V_{DC}+R_FI_o+V_F)}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-L_SV_{GS}+(L_G+L_S)(V_{DC}+R_FI_o+V_F)}{L_P\alpha}\\ \frac{g_fC_{iss}^2V_{th}}{\beta}\\ 0\end{bmatrix} \tag{34}$$

Where, $\alpha=L_G+L_S-L_S^2/L_P$, $\beta=C_{iss}(C_{oss}C_{iss}-C_{GD}^2)$.

The coefficient matrixes of stage 3 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{\alpha} & \frac{-1}{\alpha} & 0 & \frac{L_S}{L_P\alpha} & \frac{L_S}{L_P\alpha}\\ \frac{C_{oss}C_{iss}}{\beta} & \frac{-g_fC_{GD}C_{iss}}{\beta} & \frac{C_{GD}C_{iss}}{\beta} & 0 & 0\\ \frac{L_SR_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0 & \frac{-(L_G+L_S)}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha}\\ \frac{C_{GD}C_{iss}}{\beta} & \frac{-g_fC_{iss}^2}{\beta} & \frac{C_{iss}^2}{\beta} & 0 & 0\\ 0 & 0 & \frac{1}{C_F} & 0 & 0\end{bmatrix} \tag{35}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{L_PV_{GS}-L_SV_{DC}}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-L_SV_{GS}+(L_G+L_S)V_{DC}}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-I_o}{C_F}\end{bmatrix} \tag{36}$$

The coefficient matrixes of stage 4 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{\alpha} & \frac{-1}{\alpha} & 0 & \frac{L_S}{L_P\alpha} & \frac{L_S}{L_P\alpha}\\ \frac{C_{oss}C_{iss}}{\beta} & 0 & \frac{C_{GD}C_{iss}}{\beta} & \frac{-C_{GD}C_{iss}}{R_{on}\beta} & 0\\ \frac{L_SR_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0 & \frac{-(L_G+L_S)}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha}\\ \frac{C_{GD}C_{iss}}{\beta} & 0 & \frac{C_{iss}^2}{R_{on}\beta} & -\frac{C_{iss}^2}{R_{on}\beta} & 0\\ 0 & 0 & \frac{1}{C_F} & 0 & 0\end{bmatrix} \tag{37}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{L_PV_{GS}-L_SV_{DC}}{L_P\alpha}\\ 0\\ \frac{-L_SV_{GS}+(L_G+L_S)V_{DC}}{L_P\alpha}\\ 0\\ \frac{-I_o}{C_F}\end{bmatrix} \tag{38}$$

B. Turn-off Switching Transition

The coefficient matrixes of stage 1 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{L_G+L_S} & \frac{-1}{L_G+L_S} & 0 & 0 & 0\\ \frac{1}{C_{GS}+C_{GD}} & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix} \tag{39}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{V_{SS}}{L_G+L_S}\\ 0\\ 0\\ 0\\ 0\end{bmatrix} \tag{40}$$

The coefficient matrixes of stage 2 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{\alpha} & \frac{-1}{\alpha} & 0 & \frac{L_S}{L_P\alpha} & \frac{L_S}{L_P\alpha}\\ \frac{C_{oss}C_{iss}}{\beta} & \frac{-g_fC_{GD}C_{iss}}{\beta} & \frac{C_{GD}C_{iss}}{\beta} & 0 & 0\\ \frac{L_SR_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0 & \frac{-(L_G+L_S)}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha}\\ \frac{C_{GD}C_{iss}}{\beta} & \frac{-g_fC_{iss}^2}{\beta} & \frac{C_{iss}^2}{\beta} & 0 & 0\\ 0 & 0 & \frac{1}{C_F} & 0 & 0\end{bmatrix} \tag{41}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{L_PV_{GS}-L_SV_{DC}}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-L_SV_{GS}+(L_G+L_S)V_{DC}}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-I_o}{C_F}\end{bmatrix} \tag{42}$$

The coefficient matrixes of stage 3 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{\alpha} & \frac{-1}{\alpha} & \frac{L_SR_F}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0\\ \frac{C_{oss}C_{iss}}{\beta} & \frac{-g_fC_{GD}C_{iss}}{\beta} & \frac{C_{GD}C_{iss}}{\beta} & 0 & 0\\ \frac{L_SR_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & \frac{-(L_G+L_S)R_F}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha} & 0\\ \frac{C_{GD}C_{iss}}{\beta} & \frac{-g_fC_{iss}^2}{\beta} & \frac{C_{iss}^2}{\beta} & 0 & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix} \tag{43}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{L_PV_{GS}-L_S(V_{DC}+R_FI_o+V_F)}{L_P\alpha}\\ \frac{g_fC_{GD}C_{iss}V_{th}}{\beta}\\ \frac{-L_SV_{GS}+(L_G+L_S)(V_{DC}+R_FI_o+V_F)}{L_P\alpha}\\ \frac{g_fC_{iss}^2V_{th}}{\beta}\\ 0\end{bmatrix} \tag{44}$$

The coefficient matrixes of stage 4 are as follows:

$$\boldsymbol{A}=\begin{bmatrix}\frac{-R_G}{\alpha} & \frac{-1}{\alpha} & \frac{L_SR_F}{L_P\alpha} & \frac{L_S}{L_P\alpha} & 0\\ \frac{C_{oss}C_{iss}}{\beta} & 0 & \frac{C_{GD}C_{iss}}{\beta} & 0 & 0\\ \frac{L_SR_G}{L_P\alpha} & \frac{L_S}{L_P\alpha} & \frac{-(L_G+L_S)R_F}{L_P\alpha} & \frac{-(L_G+L_S)}{L_P\alpha} & 0\\ \frac{C_{GD}C_{iss}}{\beta} & 0 & \frac{C_{iss}^2}{\beta} & 0 & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix} \tag{45}$$

$$\boldsymbol{B}=\begin{bmatrix} \dfrac{L_P V_{GS}-L_S(V_{DC}+R_F I_o+V_F)}{L_P\alpha} \\ 0 \\ \dfrac{-L_S V_{GS}+(L_G+L_S)(V_{DC}+R_F I_o+V_F)}{L_P\alpha} \\ 0 \\ 0 \end{bmatrix} \quad (46)$$

REFERENCES

[1] P. Ning, F. Wang, and K. D. Ngo, "High-temperature SiC power module electrical evaluation procedure," *IEEE Trans. Power Electron.*, Vol. 26, No. 11, pp. 3079-3083, Nov. 2011.

[2] I. Josifovic, J. Popovic-Gerber, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3843-3854, Aug. 2012.

[3] B. Wrzecionko, D. Bortis, J. Biela, and J.W. Kolar, "Novel AC-coupled gate driver for ultrafast switching of normally off SiC JFETs," *IEEE Trans. Power Electron.*, Vol. 27, No. 7, pp. 3452-3463, July 2012.

[4] D. Han, J. Noppakunkajorn, and B. Sarlioglu, "Analysis of a SiC three phase voltage source inverter under various current and power factor operations," in *Conf. IECON 2013*, pp. 447-452, 2013.

[5] D. Han, J. Noppakunkajorn, and B. Sarlioglu, "Efficiency comparison of SiC and Si-Based bidirectional DC-DC converters," in *Conf. ITEC 2013*, pp. 1-7, 2013.

[6] W. Zhang, Z. Xu, Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter," in *Conf. ECCE 2013*, pp. 3571-3578, 2013.

[7] A. Kadavelugu, S. Baek, S. Dutta, S. Bhattacharya, M. Das, A. Agarwal, and J. Scofield, "High-frequency design considerations of dual active bridge 1200 V SiC MOSFET dc-dc converter," in *Conf. APEC 2011*, pp. 314-320, 2011.

[8] Y. Wang, S. W. H. de Haan, and J. A. Ferreira, "Potential of improving PWM converter power density with advanced components," *Power Electronics and Applications*, pp. 1-10, 2009.

[9] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Conf. IPEC 2010*, pp. 164-169, 2010.

[10] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "Evaluation of SiC MOSFETs for a high efficiency three-phase Buck rectifier," in *Conf. APEC 2012*, pp. 1762-1769, 2012.

[11] O. Mostaghimi, N. Wright, and A. Horsfall, "Design and performance evaluation of SiC based DC-DC converter for PV applications," in *Conf. ECCE 2012*, pp. 3956-3963, 2012.

[12] C. Stewart, A. Escobar-Mejia, and J. C. Balda, "Guidelines for developing power stage layouts using normally-off SiC JFETs based on parasitic analysis," in *Conf. ECCE 2013*, pp. 948-955, 2013.

[13] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, "Parasitic inductance effects on the switching loss measurement of power semiconductor devices," *Industrial Electronics, 2006 IEEE International Symposium on,* Vol. 2, pp. 847-852, 2006.

[14] H. Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," in *Conf. PEDG 2014*, pp. 1-5, 2014.

[15] Tektronix, Low Capacitance Probes Minimize Impact on Circuit Operation, http://www.tek.com/document/ application- note, 2014.

[16] Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in *Conf. APEC 2014*, pp. 2534-12541, 2014.

[17] R. Fu, A. Grekov, K. Peng, and E. Santi, "Parasitic modeling for accurate inductive switching simulation of converters using SiC devices," in *Conf. ECCE 2013*, pp. 1259-1265, 2013.

[18] Y. Cui, M. Chinthavali, and L. M. Tolbert, "Temperature dependent Pspice model of silicon carbide power MOSFET," in *Conf. APEC 2012*, pp. 1698-1704, 2012.

[19] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Master thesis, Virginia Polytechnic Institute and State University, USA, 2009.

[20] R. Pratap, R. K. Singh, and V. Agarwal, "SiC Power MOSFET modeling challenges," *Engineering and Systems*, pp. 1-3, 2012.

[21] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer-Verlag GmbH, Chap. 6, pp. 437-443, 2008.

[22] M. Rodriguez, A. Rodriguez, P. F. Miaja, and J. Sebastian, "A complete analytical switching loss model for power MOSFETs in low voltage converters," *Power Electronics and Applications*, pp. 1-10, 2009.

[23] J. Wang, S. H. Chung and R. H. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Trans. Power Electron.*, Vol. 28, No. 1, pp. 573-590, Jan. 2013.

[24] Y. Ren, M. Xu, J. Zhou, and F.C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, Vol. 21, No.2, pp. 310-319, Mar. 2006.

[25] M. Rodríguez, A. Rodriguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: an improved analytical losses model," *IEEE Trans. Power Electron.*, Vol. 25, No. 6, pp. 1626-1640, Jun. 2010.

[26] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Conf. APEC 2004*, pp. 516-521, 2004.

[27] D. Díaz, M. Vasic, O. García, J. A. Oliver, P. Alou, and J. A. Cobos, "Hybrid behavioral-analytical loss model for a high frequency and low load DC-DC buck converter," in *Conf. ECCE 2012*, pp. 4288-4294, 2012.

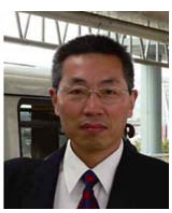
[28] T. Meade, D. O'Sullivan, R. Foley, C. Achimescu, M. G. Egan, and P. McCloskey, "Parasitic inductance effect on switching losses for a high frequency Dc-Dc converter," in *Conf. APEC 2008*, pp. 3-9, 2008.

[29] J. Wang, and S. H. Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," in *Conf. ECCE 2013*, pp. 480-487, 2013.

[30] C. N. Ho, F. Canales, A. Coccia, and M. Laitinen, "A circuit-level analytical study on switching behaviors of SiC diode at basic cell for power converters," *Industry Applications Society Annual Meeting*, pp. 1-8, 2008.

[31] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, Vol. 29, No. 5, pp. 2208-2219, May 2014.
[32] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET," *IEEE Trans. Electron. Devices*, Vol. 62, No. 2, pp. 333-338, Feb. 2015.
[33] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-Oriented Treatment of Nonlinear Capacitances in Switched-Mode Power Supplies," *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 985-995, Feb. 2015.
[34] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," *IEEE Trans. Power Electron.*, Vol. 29, No. 4, pp. 1977-1985, Apr. 2014.
[35] D. Reusch, and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, Vol. 29, No. 4, pp. 2008-2015, Apr. 2014.
[36] J. Wang, , and S. H. Chung, "A novel rcd level shifter for elimination of spurious turn-on in the bridge-leg configuration," *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 976-984, Feb. 2015.
[37] J. B. Witcher, "Methodology for switching characterization of power devices and modules," Master thesis, Virginia Polytechnic Institute and State University, USA, 2003.

Mei Liang was born in Hebei Province, China, in 1988. She received her B.S. degree in Electronic Engineering from Beijing Jiaotong University, Beijing, China, in 2011. She is presently working towards her Ph.D. degree at Beijing Jiaotong University. Her current research interests include power conversion systems and wide band-gap semiconductor applied research.



Trillion Q. Zheng (Qionglin Zheng) (M'06-SM'07) was born in Jiangshan, Zhejiang Province, China, in 1964. He received his B.S. degree in Electrical Engineering from Southwest Jiaotong University, Sichuan, China, in 1986; and his M.S. and Ph.D. degrees in Electrical Engineering from Beijing Jiaotong University, Beijing, China, in 1992 and 2002, respectively. He is presently a University Distinguished Professor at Beijing Jiaotong University. He is the director of the Center for Electric Traction, founded by Ministry of Education, China. His current research interests include the power supplies and AC drives of railway traction systems, high performance and low loss power electronics systems, PV based converters and control, active power filters, and power quality correction. He holds 17 Chinese patents, and has published over 60 journal articles and more than 100 technical papers in conference proceedings. From 2003 to 2011, he served as the Dean of the School of Electrical Engineering at Beijing Jiaotong University. He is presently the Deputy Director of the Council of the Beijing Society for Power Electronics, and a member of the Council of the China Electrotechnical Society. He received an Excellent Teacher Award of Beijing Government (1997), and a Youth Award of Railway Science and Technology of Zhan Tianyou (2005). He is a laureate of the Youth Elite of Science and Technology of the Railway Ministry of China (1998), and is a Zhongda Scholar for power electronics and motor drive area, by Delta Environmental and Educational Foundation (2007).

Yan Li was born in Heilongjiang Province, China, in 1977. She received her B.S. and M.S. degrees in Electrical Engineering from Yanshan University, Qinhuangdao, China, in 1999 and 2003, respectively; and her Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2009. From 1999 to 2009, she was at Yanshan University. Since 2009, she has been in the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China. Her current research interests include multiple-input dc/dc converters, renewable power systems, and PV grid-tied systems.