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High-Performance Control of Three-Phase Four-Wire DVR Systems using Feedback Linearization

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Abstract

Power quality is a critical issue in distribution systems, where a dynamic voltage restorer (DVR) is commonly used to mitigate the voltage disturbances for loads. This paper deals with a nonlinear control for the three-phase four-wire (3P-4W) DVR under a grid voltage unbalance and nonlinear loads in the distribution system, where a novel control scheme based on the feedback linearization technique is proposed. Through feedback linearization, a nonlinear model of a DVR with a PWM voltage-source inverter (VSI) and LC filters is linearized. Then, the controller design of the linearized model is performed by applying the linear control theory, where the load voltages are kept constant by controlling the *d-q-0* axis components of the DVR output voltages. To keep the load voltage unchanged, an in-phase compensation strategy is employed, where the load voltages are recovered to be the same as the previous voltage without a change in the magnitude. With this strategy, the performance of the DVR becomes faster and more stable even under unbalanced source voltages and nonlinear loads. The validity of the proposed control strategy has been verified by simulation and experimental results.

Key words: Dynamic voltage restorers, feedback linearization, SOGI-PLL, three-phase four-wire VSI, voltage unbalance

I. INTRODUCTION

In recent decades, the high penetration of renewable energy systems such as wind energy, solar energy, fuel cell, etc. and the use of semiconductor devices in electrical equipment connected to power distribution systems have degraded the power quality of distribution networks. The critical power quality issue in distribution systems is related to disturbances in the grid voltages. Due to the increase in the application of power electronics devices, which are integrated in industrial processes, the industrial loads are seriously affected by disturbances of the power supply. This results in malfunctions, tripping, or even faults of the load system. Voltage sags, swells, harmonics, unbalances, and flickers are generally considered as critical phenomena of voltage disturbances in distribution systems [1]-[3]. The main reason for voltage sags is short-circuit faults such as line-to-ground faults and line-to-line faults. They are also caused by the startup of high power rated induction motors. Voltage swells are normally caused by switched capacitors or the removal of a large load. The extensive use of nonlinear loads increases the current and voltage harmonic contents further [4]-[6].

There have been several schemes to improve the power quality in the distribution networks. One of the preferable schemes is a DVR system, in which the DVR plays the role of maintaining the load voltage at its nominal value when the grid voltage drops suddenly. The DVR is a custom power device, which is composed of a VSI, output LC filters, and an isolated transformer inserted between the source and the loads [7]-[10]. In view of the load side, a Δ/Y transformer is usually used to connect industrial loads to a power supply, from which the zero-sequence component in the source side can be eliminated. On the other hand, a Y/Y transformer with a grounded neutral is still used in distribution systems [11]. This results in a propagation of the zero-sequence component to the load during unbalanced faults. Then, the DVR is required to generate the zero-sequence voltage component. For this requirement, a DVR system based on a four-leg VSI or a 3P-4W VSI with split capacitors is

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preferred [11]-[13].

Control of a DVR system takes two steps: the generation of a voltage reference to be injected, and the control of an inverter to produce a required output voltage. A cascaded controller consisting of an outer voltage control loop for the *d-q* components and inner current control loops has been presented in [14]. However, its control dynamic is slow due to a limitation on the bandwidth of the voltage control loop [7]. Moreover, under unbalanced sag conditions, negative-sequence and zero-sequence components may appear in the source voltage. Then, the *d-q* components of the source voltage cannot be DC signals. Under these conditions, a typical PI (proportional integral) controller does not work appropriately for regulating the AC signals. To overcome the limitation on the control bandwidth, an enhanced resonant control strategy has been presented for controlling the UPQC (unified power quality conditioner) [15], which can compensate for the load voltages under the conditions of an unbalanced and distorted source voltage and load. Another critical issue considered for controlling the DVR is the nonlinearity of the DVR. To overcome this drawback, a feedback linearization technique has been suggested for controlling uninterruptible power supply (UPS) inverter systems [16], [17]. Furthermore, for the nonlinear system model, the feedback linearization control gives better transient performance than the linear control techniques based on the PI and resonant controls.

In this paper, the application of feedback linearization for controlling DVR systems is proposed, which is a modification of previous research [18]. In the extended version, an advanced PLL (phase-locked loop) scheme based on a second-order generalized integrator (SOGI) is newly added, which is used to extract the phase angle of the source voltage. The SOGI-based PLL is a very precise and fast detection system with a self-tuning function against grid frequency variations and without any errors even in the case of unbalanced and distorted conditions of the source voltage. In addition, new simulation and experimental results with different conditions from those of the previous one are presented in this paper.

In detail, a feedback linearization-based control algorithm for 3P-4W DVR systems is proposed in this paper, in which the positive-sequence, negative-sequence, and zero-sequence components of the DVR output voltages are injected into the distribution system to keep the load voltage unchanged. For this control scheme, a nonlinear relationship between the inverter currents and the output voltages is derived from a power balance between the inverter output and the load sides. Then, the output voltage controller is designed using the linear control theory. The pole placement technique is used to design the tracking control law. In addition, for the DVR system based on a three-phase four-wire VSI, the three-dimensional space-vector PWM is applied. With the nonlinear control scheme, a high dynamic response of the DVR control is obtained under unbalanced conditions in terms of grid voltages and loads as well as nonlinear loads. The effectiveness of the proposed method is verified with simulation and experimental results for 3P-4W distribution systems.

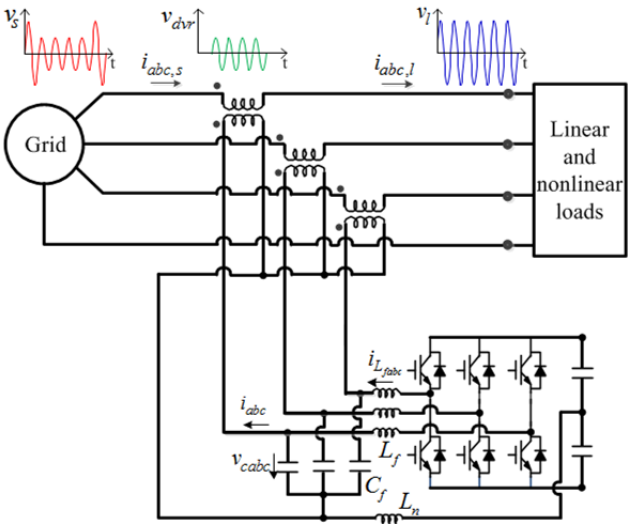

Fig. 1. DVR circuit in three-phase four wire distribution power system.

II. Overview of 3P-4W DVR Systems

A. System Description

Fig. 1 shows a DVR circuit connected to a three-phase four-wire distribution power system. To compensate for unbalanced grid voltage sags, the 3P-4W DVR should be able to produce positive, negative, and zero-sequence components, where output L_fC_f filters are used to filter out the harmonic ripples of the voltage and current. The DC input of the DVR inverter can be an energy storage device or a shunt rectifier connected to the grid side or the load side [8], [9]. In this study, the DC-input voltage of the DVR inverter is supplied from a separated diode rectifier for simplicity.

B. Modeling of a 3P-4W DVR Inverter

The DVR inverter shown in Fig. 1 is modeled through the relationship of the output voltages and currents expressed in the synchronous *d-q-0* reference frame as [17]:

$$\dot{i}_{d,L_f} = \frac{1}{L_f}v_d - \frac{1}{L_f}v_{d,c} + \omega i_{q,L_f} \tag{1}$$

$$\dot{i}_{q,L_f} = \frac{1}{L_f}v_q - \frac{1}{L_f}v_{q,c} - \omega i_{d,L_f} \tag{2}$$

$$\dot{i}_{0,L_f} = \frac{1}{\left(L_f + 3L_n\right)}v_0 - \frac{1}{\left(L_f + 3L_n\right)}v_{0,c} \tag{3}$$

$$\dot{v}_{d,c} = \frac{1}{C_f}i_d - \frac{1}{C_f}i_{d,L_f} + \omega v_{q,c} \tag{4}$$

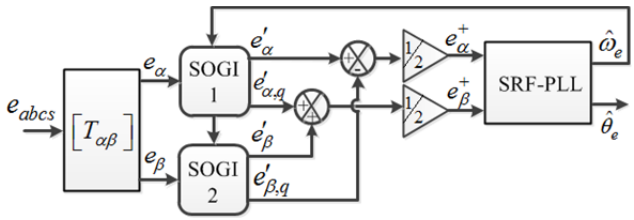

Fig. 2. Block diagram of SOGI-based PLL scheme.

$$\dot{v}_{q,c} = \frac{1}{C_f} i_q - \frac{1}{C_f} i_{q,L_f} - \omega v_{d,c} \tag{5}$$

$$\dot{v}_{0,c} = \frac{1}{C_f} i_{0,L_f} - \frac{1}{C_f} i_0 \tag{6}$$

where i_{dq0,L_f} are the *d-q-0* axis inverter output currents, i_{dq0} are the *d-q-0* axis output currents of the DVR, v_{dq0} are the *d-q-0* axis inverter terminal voltages, $v_{dq0,c}$ are the *d-q-0* axis capacitor voltages, ω is the grid angular frequency, L_f and C_f are the output filter inductance and capacitance, respectively, and L_n is the neutral-line inductance.

C. SOGI-Based PLL Scheme for Phase Angle Detection

In this study, the SOGI-based PLL scheme is adopted to detect the phase angle of the source voltage, where the phase angle information is used for the operation of a DVR inverter. The operation principle of the SOGI-PLL is based on the estimation of the positive-sequence and negative-sequence components of the grid voltage vector by the SOGI [19], [20]. A diagram of the SOGI-PLL scheme is shown in Fig. 2. Firstly, by a *Clarke* transformation, the three-phase voltage vector, e_{abcs}, can be transformed into the $\alpha-\beta$ components, e_α and e_β, respectively, in the stationary reference frame. Then, by the SOGI, a set of two signals (α and β) which are in-phase and in-quadrature components is generated. From these signals, the positive-sequence and negative-sequence components are calculated as shown in Fig. 2 [19]. Finally, a conventional PLL scheme based on the synchronous reference frame (SRF-PLL) is applied to the estimated positive-sequence component, where the phase angle can be estimated.

D. Generation of the Voltage References for DVR Systems

For normal operation of the loads in the case of grid voltage sags, the DVR needs to compensate voltage disturbance instantaneously. There are three categories for DVR control schemes [9]. The first type is referred to as pre-sag compensation, where the load voltage is recovered to be the same as the previous one in terms of magnitude and phase. The second strategy is referred to as in-phase compensation, which means that the phase of the load voltage is controlled

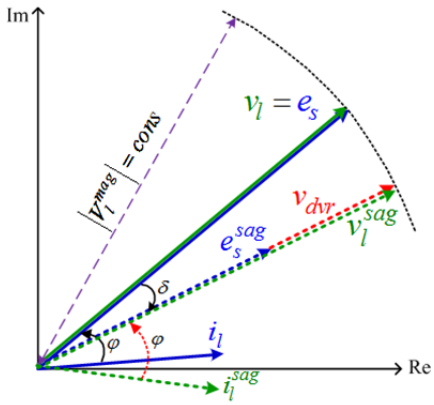

Fig. 3. Phasors of the voltages and currents for the in-phase compensation strategy.

to be the same as that of the grid voltage after a sag. This method requires a low voltage rating of the DVR system when compared to that of the first one. However, a phase jump in the load voltage may occur. The other scheme is to control the compensation voltage of the DVR so that it lags the load current by 90 degrees. This scheme is able to control zero real power flowing through the DVR, and is referred to as energy optimized compensation.

In this study, the in-phase compensation strategy is adopted, where the amplitude of the load voltage is kept exactly the same as before the sag, while the phase of the load voltage is the same as that of the source voltage after the sag. From Fig. 1, the load voltage is expressed as:

$$v_{abc,l} = e_{abc,s} - v_{abc,dvr} \tag{7}$$

where $v_{abc,l}$ is the load voltage, $e_{abc,s}$ is the three-phase source voltage, and $v_{abc,dvr}$ is the voltage injected by the DVR. Fig. 3 shows the voltage and current phasors before and during a sag, in which the solid lines indicate the source and load voltages before the sag. During the sag, the source voltage drops, but the magnitude of the load voltage is kept constant by the compensated voltage of the DVR system. The dash lines indicate the voltages during the sag.

The control of the DVR inverter is performed in the synchronous reference frame, where the phase angle of the source voltage is utilized for transforming the DVR output voltages and load voltages. In order to keep the load voltage constant, the voltage references for the DVR system expressed in the synchronous reference frame are calculated as:

$$\begin{bmatrix} v^*_{de,dvr} = e_{de,s} - v^*_{de,l} \\ v^*_{qe,dvr} = e_{qe,s} - v^*_{qe,l} \\ v^*_{0,dvr} = e_{0,s} - v^*_{0,l} \end{bmatrix} \tag{8}$$

where $v^*_{de,dvr}, v^*_{qe,dvr}, v^*_{0,dvr}$ are the *d-q-0* components of the voltage references of the DVR, $e_{de,s}, e_{qe,s}, e_{0,s}$ are the *d-q-*

0 components of the source voltage, and $v_{de,l}^{*}, v_{qe,l}^{*}, v_{0,l}^{*}$ are the *d-q-0* components of the load voltage references, which are set at the constant values as:

$$\begin{bmatrix} v_{de,l}^{*} = 0 \\ v_{qe,l}^{*} = V_l^{mag} \\ v_{0,l}^{*} = 0 \end{bmatrix} \tag{9}$$

where V_l^{mag} is the magnitude of the load voltage at the rating.

III. Proposed Control Strategy Based on Feedback Linearization

A. Review of the Feedback Linearization Theory

Firstly, the feedback linearization theory is briefly reviewed, where the state equations for a multi-input multi-output system are expressed as [21]:

$$\dot{x} = f(x) + g(x)u \tag{10}$$

$$y = h(x) \tag{11}$$

where *x* is the state vector, *u* is the control inputs, *y* is the outputs, *f* and *g* are the smooth vector fields, and *h* is the smooth scalar function.

Then, the outputs in (11) are differentiated until the inputs appear, from which the linear relationship between the inputs and outputs of the system are obtained. This process is expressed as:

$$\begin{bmatrix} y_1^{(r_1)} \\ \cdots \\ \cdots \\ y_m^{(r_m)} \end{bmatrix} = \begin{bmatrix} L_f^{r_1} h_1(x) \\ \cdots \\ \cdots \\ L_f^{r_m} h_m(x) \end{bmatrix} + E(x) \begin{bmatrix} u_1 \\ \cdots \\ \cdots \\ u_m \end{bmatrix} \tag{12}$$

where the $m \times m$ matrix E(x) is defined as:

$$E(x) = \begin{bmatrix} L_{g_1} L_f^{r_1-1} h_1 & \cdots & \cdots & L_{g_m} L_f^{r_1-1} h_1 \\ \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots \\ L_{g_1} L_f^{r_m-1} h_m & \cdots & \cdots & L_{g_m} L_f^{r_1-1} h_m \end{bmatrix} \tag{13}$$

and $L_g h$ and $L_f h$ are the Lie derivatives of *h(x)* with respect to *g(x)* and *f(x)*, respectively.

From (12), the input transformation can be obtained as:

$$u = -E^{-1}(x) \begin{bmatrix} L_f^{r_1} h_1(x) \\ \cdots \\ \cdots \\ L_f^{r_m} h_m(x) \end{bmatrix} + E^{-1}(x) \begin{bmatrix} v_1 \\ \cdots \\ \cdots \\ v_m \end{bmatrix} \tag{14}$$

where $[v_1 \; v_2 \cdots v_m]^T$ is the new input, which has a linear differential relation with the output *y* derived from (12) and (14) as:

$$\begin{bmatrix} v_1 \\ \cdots \\ \cdots \\ v_n \end{bmatrix} = \begin{bmatrix} y_1^{(r_1)} \\ \cdots \\ \cdots \\ y_m^{(r_m)} \end{bmatrix} \tag{15}$$

where $y_1^{(r_1)}, \ldots, y_m^{(r_m)}$ are the outputs differentiated *r* times, $v_1, \ldots, v_m$ are the new inputs, which have a linear relationship with the control inputs.

B. Proposed Feedback Linearization Control Technique for Three-Phase Four-Wire DVR Systems

In order to apply feedback linearization for the DVR inverter, equations (1) to (6) are rewritten in the form of (10) and (11), which are expressed as:

$$f = \begin{bmatrix} \omega i_{q,L_f} - \frac{1}{L_f} v_{d,c} \\ -\omega i_{d,L_f} - \frac{1}{L_f} v_{q,c} \\ -\frac{1}{L_f + 3L_n} v_{n,c} \\ \frac{1}{C_f} i_{d,L_f} - \frac{1}{C_f} i_{d,c} + \omega v_{q,c} \\ \frac{1}{C_f} i_{q,L_f} - \frac{1}{C_f} i_q - \omega v_d \\ \frac{1}{C_f} i_{0,L_f} - \frac{1}{C_f} i_0 \end{bmatrix}, \quad g = \begin{bmatrix} \frac{1}{L_f C_f} & 0 & 0 \\ 0 & \frac{1}{L_f C_f} & 0 \\ 0 & 0 & \frac{1}{(L_f + 3L_n) C_f} \end{bmatrix}$$

$$x = \begin{bmatrix} i_{d,L_f} & i_{q,L_f} & i_{0,L_f} & v_{d,c} & v_{q,c} & v_{0,c} \end{bmatrix}^T$$

$$u = \begin{bmatrix} v_d & v_q & v_0 \end{bmatrix}^T, \qquad y = \begin{bmatrix} v_{d,c} & v_{q,c} & v_{0,c} \end{bmatrix}^T.$$

Next, the outputs are differentiated twice to produce a linear relationship with the control inputs, which are written as:

$$\begin{bmatrix} \ddot{y}_1 \\ \ddot{y}_2 \\ \ddot{y}_3 \end{bmatrix} = A(x) + E(x) \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{16}$$

where:

$$A(x) = \begin{bmatrix} \frac{2}{C_f} \omega i_{q,L_f} - \left(\frac{1}{L_f C_f} + \omega^2 \right) v_{d,c} - \frac{1}{C_f} \dot{i}_d - \frac{1}{C_f} \omega i_q \\ -\frac{2}{C_f} \omega i_{d,L_f} - \left(\frac{1}{L_f C_f} + \omega^2 \right) v_{q,c} - \frac{1}{C_f} \dot{i}_q + \frac{1}{C_f} \omega i_d \\ -\frac{1}{(L_f + 3L_n) C_f} v_{0,c} - \frac{1}{C_f} \dot{i}_0 \end{bmatrix}$$

$$E(x) = \begin{bmatrix} \frac{1}{L_f C_f} & 0 & 0 \\ 0 & \frac{1}{L_f C_f} & 0 \\ 0 & 0 & \frac{1}{(L_f + 3L_n) C_f} \end{bmatrix}.$$

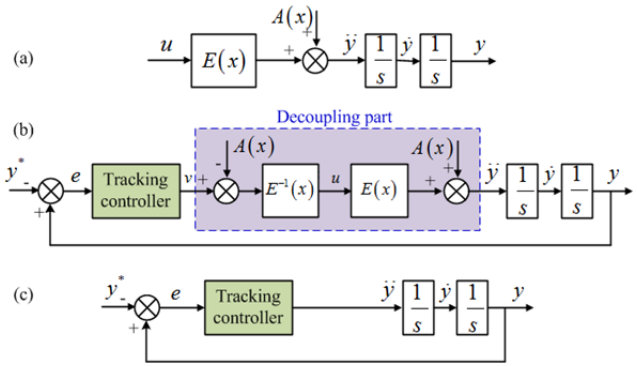

Fig. 4. Process of feedback linearization control. (a) Relation of control inputs and outputs. (b) Decoupling process. (c) Simplified control diagram.

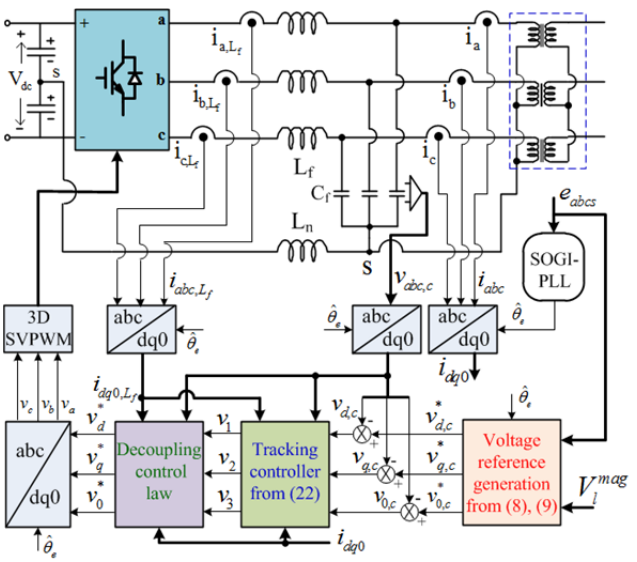

Fig. 5. Block diagram of proposed control strategy for DVR.

Then, the control law is given as:

$$\begin{bmatrix} v_d^* \\ v_q^* \\ v_n^* \end{bmatrix} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = (-A(x) + \begin{bmatrix} \ddot{y}_1 \\ \ddot{y}_2 \\ \ddot{y}_3 \end{bmatrix} E^{-1}(x). \quad (17)$$

Fig. 4 shows the process of the feedback linearization control for the DVR. Fig. 4(a) shows the input-output relation consisting of double integrators. A decoupling control law for the DVR system with a tracking controller is shown in Fig. 4(b). Then, the system with decoupling is shown in Fig. 4(c).

The new control inputs for the tracking control are obtained as:

$$\begin{aligned} v_1 &= \ddot{y}_1^* - k_{11}\dot{e}_1 - k_{12}e_1 \\ v_2 &= \ddot{y}_2^* - k_{21}\dot{e}_2 - k_{22}e_2 \\ v_3 &= \ddot{y}_3^* - k_{31}\dot{e}_3 - k_{32}e_3 \end{aligned} \quad (18)$$

where: $e_1 = y_1 - y_1^*$, $e_2 = y_2 - y_2^*$, $e_3 = y_3 - y_3^*$, and $k_{ij}(i, j = 1 \sim 3)$ are the tracking controller gains, and y_i^* refers to the references of the control variables, which are the voltage references for the output filter capacitors of the DVR system, $v_{d,c}^*$, $v_{q,c}^*$, $v_{0,c}^*$, expressed in the synchronous reference frame.

For eliminating the error of the tracking controller, the new control inputs, including the integral control, are given by:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} \ddot{y}_1^* - k_{11}\dot{e}_1 - k_{12}e_1 - k_{13}\int e_1 \\ \ddot{y}_2^* - k_{21}\dot{e}_2 - k_{22}e_2 - k_{23}\int e_2 \\ \ddot{y}_3^* - k_{31}\dot{e}_3 - k_{32}e_3 - k_{33}\int e_3 \end{bmatrix}. \quad (19)$$

TABLE I
PARAMETERS OF GRID, LOAD, AND DVR

	Parameters	Values
Grid	AC grid voltage	220 V / 60 Hz
DVR system	DC input voltage	311 V
	Neutral inductance	0.5 mH
	Filter inductance	2.25 mH
	Filter capacitance	50 μF
	Transformer ratio	1:1
	Switching frequency	5 kHz

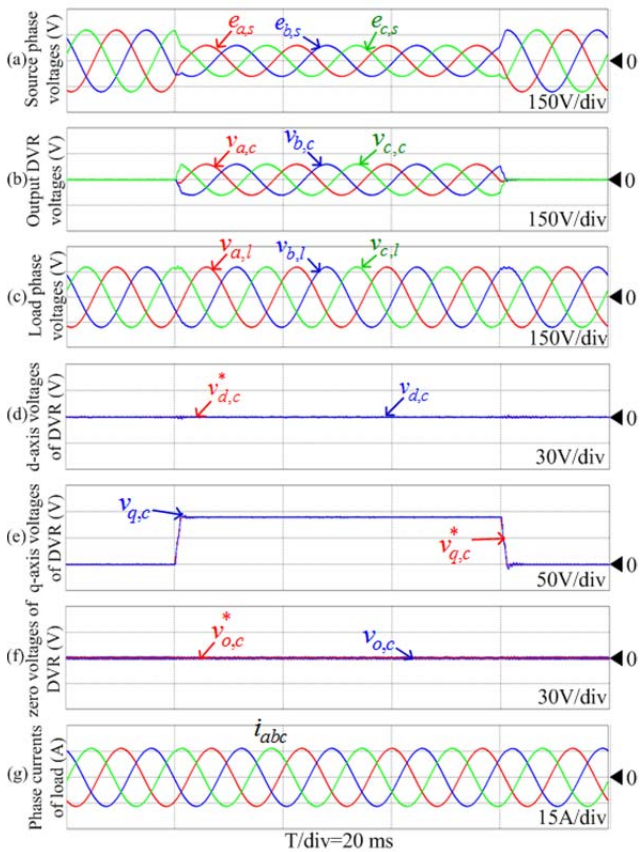

Fig. 6. Performance of DVR by FL control under balanced-voltage sag conditions with linear load. (a) Grid voltages. (b) DVR output voltages. (c) Load voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

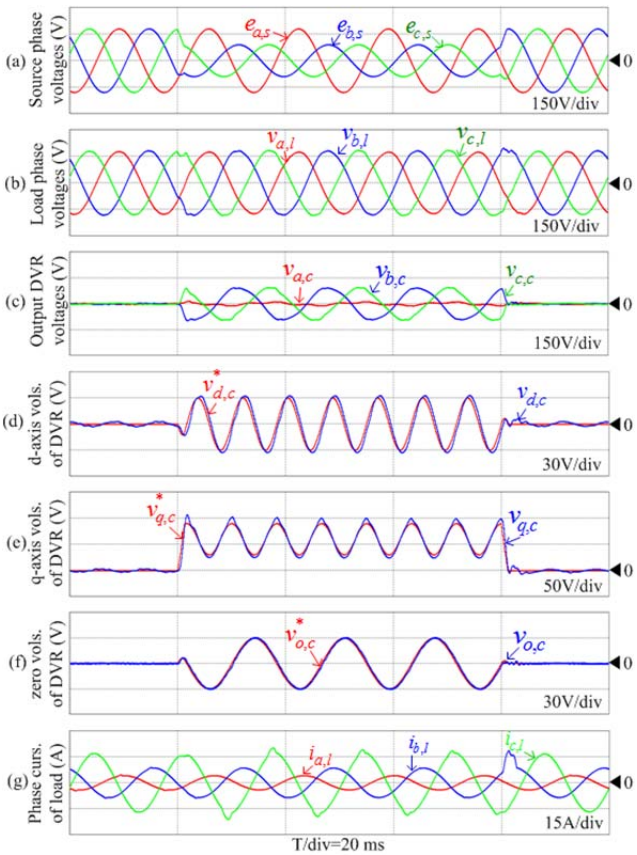

Fig. 7. Performance of DVR using the conventional PI control. (a) Grid voltages. (b) Load voltages. (c) DVR voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

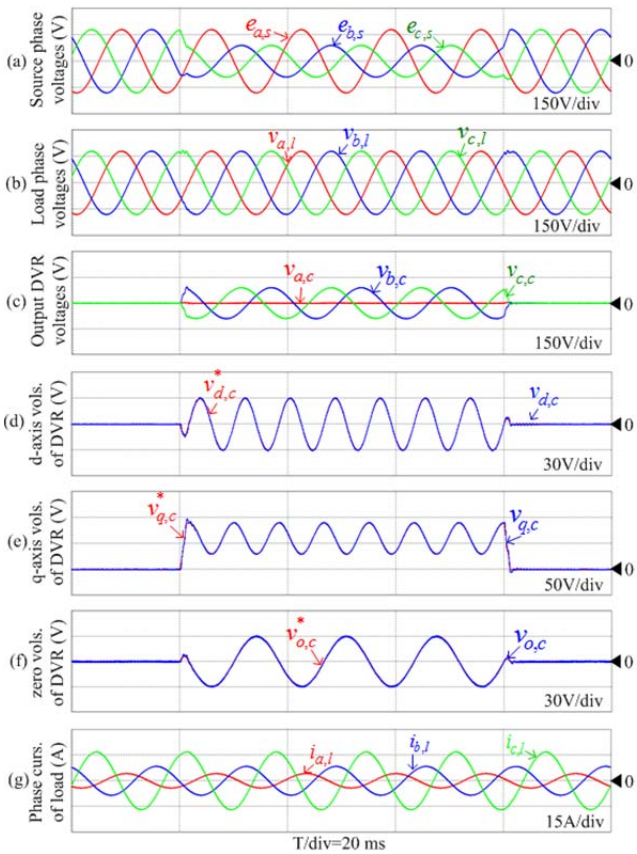

Fig. 8. Performance of DVR using feedback linearization control. (a) Source voltages. (b) Load voltages. (c) DVR voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

Then, the dynamic errors of the tracking controller from (19) are obtained as:

$$\begin{aligned} &\dddot{e}_1 + k_{11}\ddot{e}_1 + k_{12}\dot{e}_1 + k_{13}e_1 = 0 \\ &\dddot{e}_2 + k_{21}\ddot{e}_2 + k_{22}\dot{e}_2 + k_{23}e_2 = 0 \\ &\dddot{e}_3 + k_{31}\ddot{e}_3 + k_{32}\dot{e}_3 + k_{33}e_3 = 0 \end{aligned} . \quad (20)$$

From Fig. 4(c) and (20), the closed-loop transfer function for the *d*-axis DVR voltage can be expressed as:

$$\frac{y}{y^*} = \frac{v_{d,c}}{v_{d,c}^*} = \frac{\left(k_{11}s^2 + k_{12}s + k_{13}\right)}{\left(s^3 + k_{11}s^2 + k_{12}s + k_{13}\right)} \quad (21)$$

which is similar to those of the *q*-axis and zero-sequence component voltages.

The tracking controller gains are chosen by the pole-placement technique, where the poles of the transfer function, s_1, s_2, s_3, are chosen to be located in the left-half complex plane. Then, the gains of the tracking controllers are given as [14]:

$$\begin{aligned} k_{11} &= k_{21} = k_{31} = -(s_1 + s_2 + s_3) \\ k_{12} &= k_{22} = k_{32} = s_1 \cdot s_2 + s_2 \cdot s_3 + s_3 \cdot s_1 \\ k_{13} &= k_{23} = k_{33} = k_{21} = k_{31} = -s_1 \cdot s_2 \cdot s_3 \end{aligned} . \quad (22)$$

Fig. 5 shows a control block diagram of the three-phase four-wire DVR system. The voltage references expressed in the synchronous reference frame for the DVR are calculated from (8), where the phase angle of the source voltage detected by the SOGI-PLL is utilized for the *d-q-0* transformation of the voltages and currents of the DVR system. The decoupling control law gives the voltage references for the 3D-SVPWM (three-dimensional SVPWM) [17].

IV. Simulation Results

To validate the feasibility of the proposed control scheme, PSIM simulations were carried out for the 3-phase 4-wire DVR system connected in series with a distribution system, as shown in Fig. 1. The system parameters used for the simulation are listed in Table I.

Firstly, under the condition of a balanced grid voltage sag with three-phase balanced and linear loads of 10 Ω and 10mH, the ability of the DVR system to keep load voltages at a nominal value of 220 V is shown in Fig. 6. Fig. 6(a) shows the source voltages, where all of the three phase voltages drop to 50% for 60 ms. With the DVR activated, the DVR output voltages are injected, as shown in Fig. 6(b), and the

TABLE II
CONTROLLER GAINS

Controllers	Gains	
PI method	Voltage controller	$K_P = 0.057$; $K_I = 16$
	Current controller	$K_P = 8.58$; $K_I = 625$
Feedback linearization	$k_{11} = k_{21} = k_{31} = 6.05\times10^3$ $k_{12} = k_{22} = k_{32} = 9.3\times10^6$ $k_{13} = k_{23} = k_{33} = 4.5\times10^9$	

load voltages are unchanged as shown in Fig. 6(c). The load voltages after the sag are almost sinusoidal and balanced, like those pre-sag. For the DVR control, the *d-q-0* components of the DVR voltages are regulated, and their control performances are satisfactory as shown in Fig. 6(d)-(f). For the balanced grid sag condition, the *d*-axis voltage and zero-sequence voltage components are equal to zero as shown in Fig. 6(d) and (f), respectively. It can be seen in Fig. 6(e) that the *q*-axis DVR voltages are DC quantities, which are the magnitude of the DVR output voltages required to compensate for the balanced grid sag condition. Fig. 6(g) shows the three-phase load currents, which are sinusoidal and balanced.

Next, a comparison of the performance of the conventional method with PI controllers and the proposed method based on the feedback linearization control is shown in Fig. 7 and 8. For the conventional method, the design of the PI controller gains has been described in [16], [22], where the damping ratio and natural frequencies of the outer voltage and inner current control loops are 0.707 for both, 1,200 and 5,500, respectively. Then, the controller gains are obtained as listed in Table II. Here, an unbalanced grid sag where both the phase-B and C voltages drop to 50% for 60 ms is considered, which supplies three-phase unbalanced and linear loads with impedances of $40 + j15.08\ (\Omega)$, $20 + j7.54\ (\Omega)$, and $10 + j3.77\ (\Omega)$, respectively.

The performance of the DVR with the conventional PI control is shown in Fig. 7, where the unbalanced grid voltage is applied as shown in Fig. 7(a). With compensation, the load voltages are not fully balanced or sinusoidal, as shown in Fig. 7(b). Fig. 7(c) shows the DVR voltages. It can be seen in Fig. 7(d)-(f) that the control performance of the *d-q-0* components of the DVR voltages are not good. The actual voltages cannot follow their references satisfactorily since the references are time-varying. Fig. 7(g) shows the load currents.

Under the same simulation conditions, the control performance of the DVR with the proposed feedback linearization technique is shown in Fig. 8. Fig. 8(b) shows the load voltages, which are kept at nominal values even though the grid voltages are unbalanced as shown in Fig. 8(a). The output voltages of the DVR to compensate for the voltage sags are shown in Fig. 8(c), which are also unbalanced. Thus, the *d-q* components of the DVR output voltage appear in the AC waveform, which are shown in Figs. 8(d) and (e),

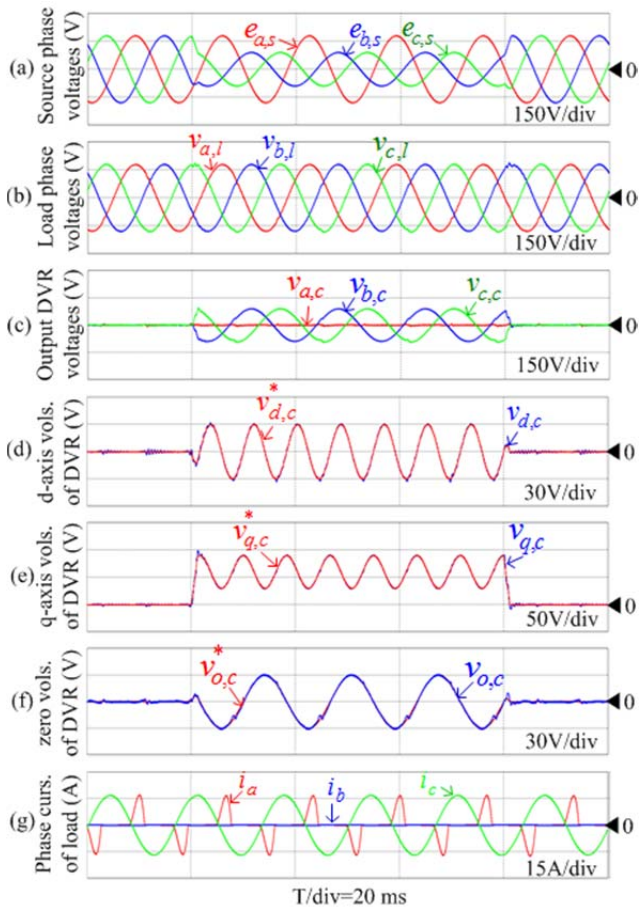

Fig. 9. DVR control for the unbalanced-voltage sag with nonlinear and unbalanced loads. (a) Grid voltages. (b) DVR output voltages. (c) Load voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

respectively. In addition, the zero-sequence voltage of the DVR appears in the AC quantity as shown in Fig. 8(f). It isobvious in Figs. 8(d)-(f) that the control performances of the *d-q-0* component voltages are satisfied, and that the actual values follow their reference well. Fig. 8(g) shows the load currents, which are unbalanced.

Finally, the control performance of the DVR system is investigated for a more critical condition, which is the condition of an unbalanced-voltage sag with nonlinear and unbalanced loads. The simulation results are shown in Fig. 9, where Fig. 9(a)-(f) correspond to those of Fig. 8(a)-(f). The nonlinear and unbalanced loads are demonstrated in Fig. 9(g), which are the three-phase currents of the loads. Due to the series connection, the currents flowing through the source, the load, and the DVR system are the same. For this condition, the DVR control still works satisfactorily, since the *d-q-0* component voltages of the DVR inverter are regulated well, as shown in Figs. 9(d)-(f).

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed control scheme,

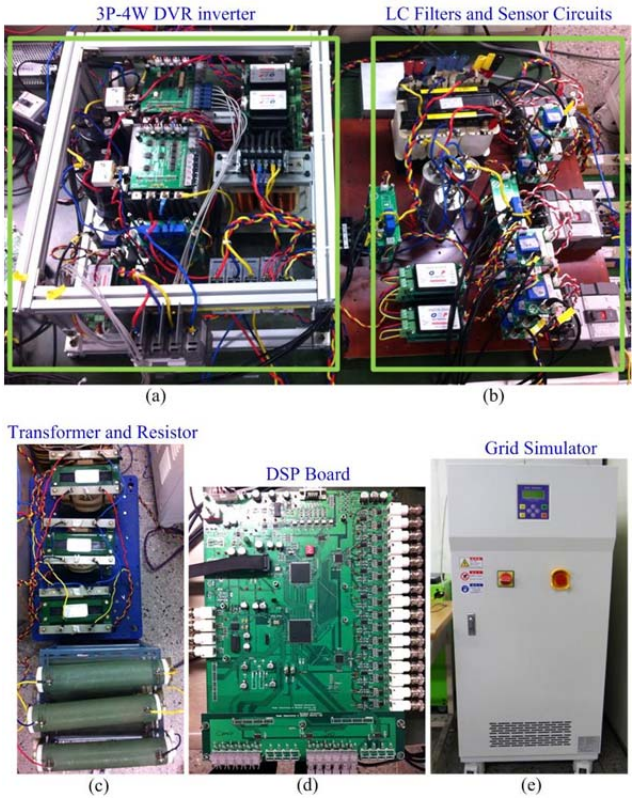

Fig. 10. Experimental prototype in the laboratory.

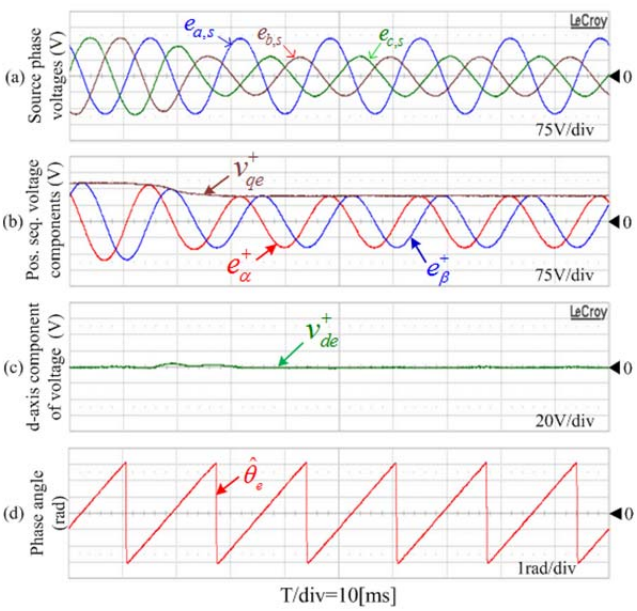

Fig. 11. SOGI-PLL performance under the unbalanced sag.

experimental tests were also conducted on an experimental prototype in the laboratory. The experimental set-up is shown in Fig. 10. The parameters of the hardware system are the same as those of the simulation system as listed in Table I. The 3P-4W split-capacitor VSI consists of an intelligent power module (PM75RLA060) and two DC-link capacitors of 1,650 μF. A high-performance DSP chip (TMS320C28335) is used as the main digital controller. A bilinear transform is

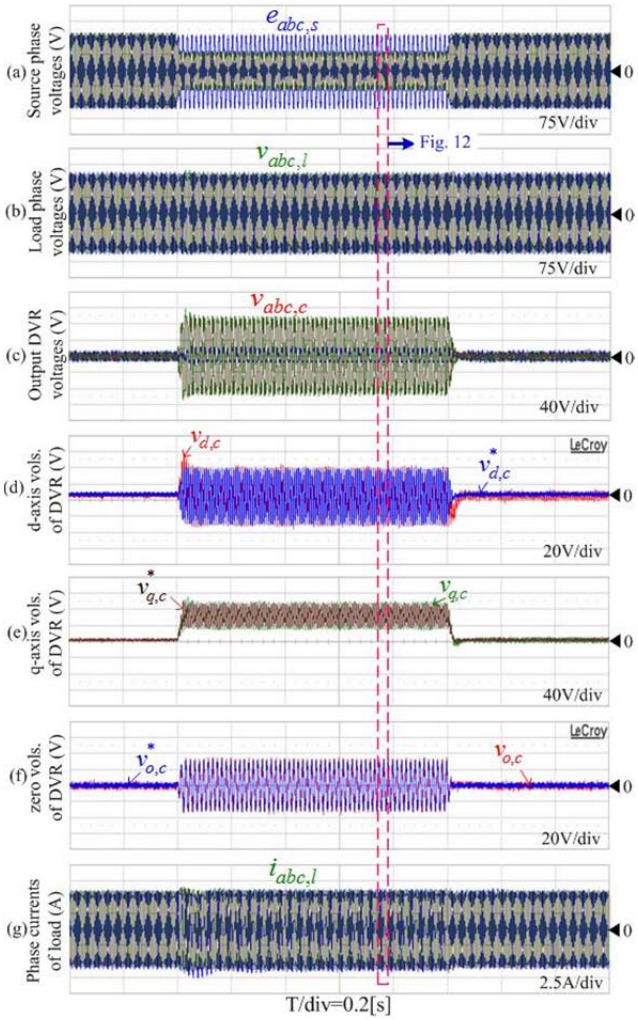

Fig. 12. Experimental results for DVR control using FL under unbalanced sag. (a) Grid voltages. (b) Load voltages. (c) DVR voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

applied to discretize the controllers for digital implementation. For generating grid voltage disturbances, a 10-kVA grid simulator is used.

Fig. 11 shows the performance of the SOGI-based PLL for the three-phase system under an unbalanced grid sag, where the three-phase grid voltages are shown in Fig. 11(a). The symmetrical positive-sequence components of the grid voltage are extracted through the SOGI, as shown in Fig. 11(b). From these components, the SRF-PLL scheme is employed to detect the phase angle as shown in Fig. 11(d), which is precisely tracked even under unbalanced voltage conditions. The SRF-PLL method utilizes the voltage orientation, where the *d*-axis component is adjusted to zero, as shown in Fig. 11(c).

The performance of the DVR inverter control for an unbalanced grid sag with the three-phase balanced RL loads of $30 + j1.13\ (\Omega)$ is investigated, as shown in Figs. 12 and 13. Fig. 13 shows magnified waveforms from Fig. 12. Fig.

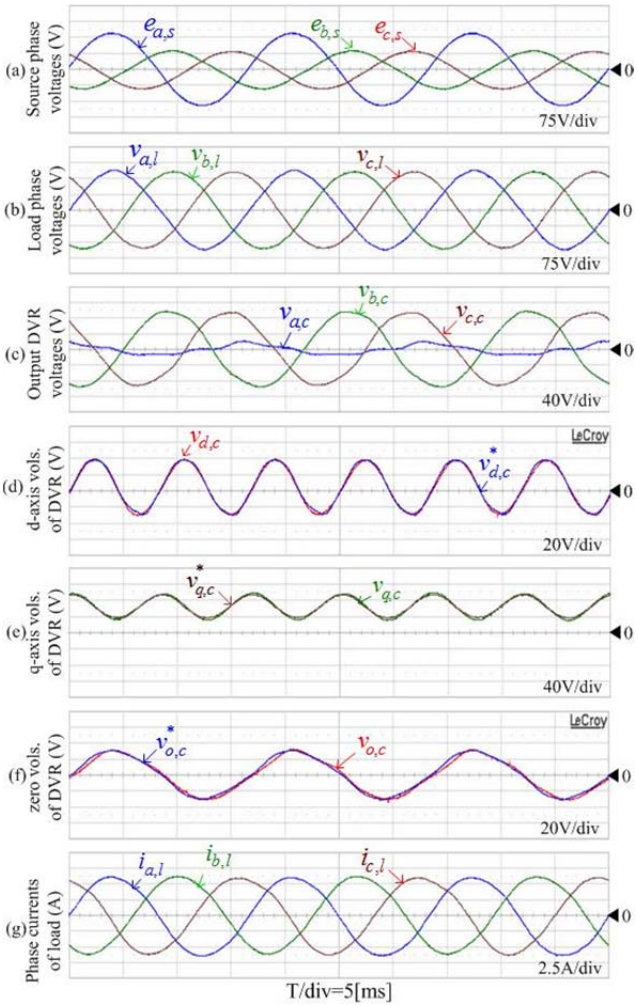

Fig. 13. Magnified waveforms of Fig. 12. (a) Grid voltages. (b) Load voltages. (c) DVR voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

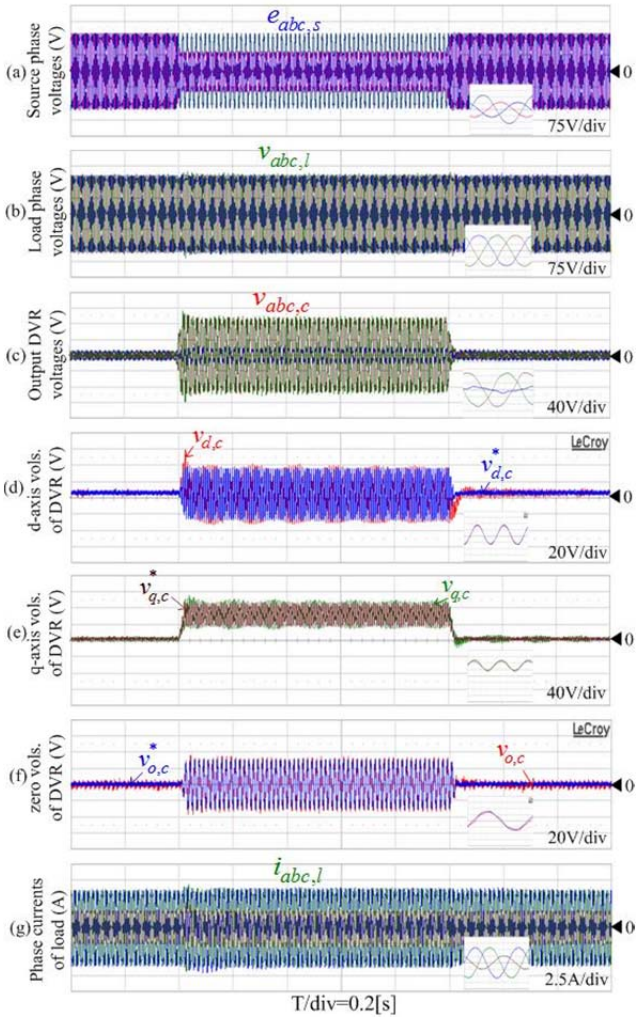

Fig. 14. Control performance of DVR under unbalanced sag with unbalanced loads. (a) Grid voltages. (b) Load voltages. (c) DVR voltages. (d) *d*-axis voltages of DVR. (e) *q*-axis voltages of DVR. (f) Zero-sequence voltages of DVR. (g) Load currents.

12(a) shows the grid voltages, where the phase-B and phase-C voltages simultaneously drop to 50% for 1 s. The three-phase unbalanced grid voltages can be clearly seen in Fig. 13(a). In order to keep the load voltages unchanged at an amplitude of 220 V, as shown in Fig. 12(b), the DVR output voltages are injected into the system as shown in Fig. 12(c). From the zoomed-in waveforms, it can be seen from Fig. 13(b) that the load voltages are balanced and sinusoidal. Fig. 13(c) shows the DVR voltages. The control performance of the DVR inverter is demonstrated in Figs. 12(d)-(f), which show the *d-q-0* components of the DVR output voltages. Figs. 13(d)-(f) show that the control performances of the *d-q-0* voltage components are satisfactory, where the actual values are regulated toward their references closely even though the *d-q-0* components of the DVR voltages are AC quantities during unbalanced sag conditions. Fig. 12(g) shows the three-phase load currents, which are kept balanced during the sag. A magnified version of this waveform is shown in Fig. 13(g).

Fig. 14 shows the control performance of the DVR inverter under unbalanced loads and unbalanced grid sag conditions, where the grid voltage condition is the same as that of the previous test shown in Fig. 14(a). The three-phase unbalanced loads of $30+j1.13\,(\Omega)$, $30+j1.13\,(\Omega)$ and $70+j1.13\,(\Omega)$ are connected. Under this condition, the load voltages are still kept at the nominal value, as shown in Fig. 14(b), by injecting the DVR voltages in Fig. 14(c). Figs. 14(d)-(f) show the *d-q-0* components of the DVR voltages. The three-phase load currents are unbalanced due to the load unbalance, as shown in Fig. 14(g).

VI. Conclusion

This paper proposed a new control algorithm for a 3P-4W DVR system in distribution power systems, where a linear model is obtained by applying the feedback linearization control theory. With the nonlinearity of the DVR system eliminated, the linear control theory can be applied to the

controller design, where the pole placement method is used for gain selection. On the other hand, for a reduction of the DVR voltage rating, the in-phase compensation strategy is utilized, where the advance SOGI-PLL scheme is used for detecting the phase angle of the source voltage. With the proposed scheme, the control performance of the DVR becomes faster and more stable under unbalanced grid voltages and nonlinear loads. This level of performance cannot be obtained by conventional PI controllers as demonstrated by the simulation results. In addition, simulation and experimental results have verified the effectiveness of the proposed control scheme for 3P-4W DVR systems.

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REFERENCES

[1] Q. N. Trinh, H.-H. Lee, and T. W. Chun, "An enhanced harmonic voltage compensator for general loads in stand-alone distributed generation systems," *Journal of Power Electronics*, Vol. 13, No. 6, pp. 1070-1079, Nov. 2013.

[2] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 2676-2683, Oct. 2010.

[3] H. Xu, X. Ma, and D. Sun, "Reactive current assignment and control for DFIG based wind turbines during grid voltage sag and swell conditions," *Journal of Power Electronics*, Vol. 15, No. 1, pp. 235-245, Jan. 2015.

[4] V. Khadkikar and A. Chandra, "UPQC-S: a novel concept of simultaneous voltage sag/swell and load reactive power compensations utilizing series inverter of UPQC," *IEEE Trans. Power Electron.*, Vol. 26, No. 9, pp. 2414-2425, Sep. 2011.

[5] C. Liu, K. Dai, K. Duan, and Y. Kang, "Application of a C-type filter based LCFC output filter to shunt active power filters," *Journal of Power Electronics*, Vol. 13, No. 6, pp. 1058-1069, Nov. 2013.

[6] G. Mahendran, M. Sathikumar, S. Thiruvenkadam, and L. Lakshminarasimman, "Multi-objective unbalanced distribution network reconfiguration through hybrid heuristic algorithm," *Journal of Electric Engineering and Technology*, Vol. 8, No. 2, pp. 215-222, Mar. 2013.

[7] H. Kim and S.-K. Sul, "Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme," *IEEE Trans. Power Electron.*, Vol. 20, No. 5, pp. 1169-1177, May 2005.

[8] T. Jimichi, H. Fujita, and H. Akagi, "Design and experimentation of a dynamic voltage restorer capable of significantly reducing an energy-storage element," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 3, pp. 817-825, May/Jun. 2008.

[9] C. Meyer, R. W. De Doncker, Y. W. Li, and F. Blaabjerg, "Optimized control strategy for a medium-voltage DVR-theoretical investigations and experimental results," *IEEE Trans. Power Electron.*, Vol. 23, No. 6, pp. 2746-2754, Nov. 2008.

[10] L.-Y. Yang, C.-L. Wang, J.-H. Liu, and C.-X. Jia, "A novel phase locked loop for grid-connected converters under non-ideal grid conditions," *Journal of Power Electronics*, Vol. 15, No. 1, pp. 216-226, Jan. 2015.

[11] S. R. Naidu and D. A. Fernandes, "Dynamic voltage restorer based on a four-leg voltage-source converter," *IET Gener. Transm. Distrib.*, Vol. 3, No. 5, pp. 437-447, 2009.

[12] S. B. Karanki, N. Geddada, M. K. Mishra, and B. K. Kumar, "A modified three-phase four-wire UPQC topology with reduced DC-link voltage rating," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 9, pp. 3555-3566, Sep. 2013.

[13] V. Khadkikar and A. Chandra, "A novel structure for three-phase four-wire distribution system utilizing unified power quality conditioner (UPQC)," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 5, pp. 1897-1902, Sep./Nov. 2009.

[14] S. Lee, Y. Chae, J. Cho, G. Choe, H. Mok, and D. Jang, "A new control strategy for instantaneous voltage compensator using 3-phase PWM inverter," in *Proc. IEEE PESC'98*, 1998, pp. 248-254.

[15] Q.-N. Trinh and H.-H. Lee, "Improvement of unified power quality conditioner performance with enhanced resonant control strategy," *IET Gener. Transm. Distrib.*, Vol. 8, No. 12, pp. 2114-2123, Dec. 2014.

[16] D.-E. Kim and D.-C. Lee, "Feedback linearization control of three-phase UPS inverter system," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 3, pp. 963-968, Mar. 2010.

[17] N. Q. T. Vo and D.-C. Lee, "Advanced control of three-phase four-wire inverters using feedback linearization under unbalanced and nonlinear load condition," *Transactions of Korean Institute of Power Electronics(KIPE)*, Vol. 18, No. 4, pp. 333-341, Aug. 2013.

[18] S.-Y. Jeong, T. H. Nguyen, D.-C. Lee, and J.-M. Kim, "Nonlinear control of three-phase four-wire dynamic voltage restorers for distribution system," in *Proc. IEEE IPEC*, pp. 2406-2412, 2014.

[19] P. Rodriguez, A. Luna, R. S. M. Aguilar, I. E. Otadui, R. Teodorescu, and F. Blaabjerg, "A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions," *IEEE Trans. Power Electron.*, Vol. 27, No. 1, pp. 99-112, Jan. 2012.

[20] A. Luna, C. Citro, C. Gavriluta, J. Hermoso, I. Candela, and P. Rodriguez, "Advanced PLL structures for grid synchronization in distributed generation," in *Proc. ICREPQ'12*, pp. 1-10, 2012.

[21] J. J. E. Slotine and W. Li, *Applied Nonlinear Control*. Englewood Cliffs, NJ:Prentice-Hall, 1991, pp. 207-271.

[22] J.-I. Jang and D.-C. Lee, "High performance control of three-phase PWM converters under non-ideal source voltage," in *Proc. IEEE ICIT*, pp. 2791-2796, 2006.

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