

Converter Utilization Ratio Enhancement in the THD Optimization of Cascaded H-Bridge 7-level Inverters

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Abstract

In this paper, a new technique for harmonic optimization in cascaded H-bridge 7-level inverters is proposed. The suggested strategy is based on minimizing an objective function which simultaneously optimizes the converter utilization and Total Harmonic Distortion (THD). The Switch Utilization Ratio (SUR) is formulized for both the phase and line-line voltages of a 7-level inverter and is considered in the final objective functions. Based upon the SUR formula, utilization ratio enhancement will reduce the value of feeding DC links, which improves the efficiency and lifetime of the circuit components due to lower voltage stresses and losses. In order to achieve more effective solution in different modulation indices, it is assumed that the DC sources can be altered. Experimental validation is presented based on a three-phase 7-level inverter prototype.

Key words: Cascaded H-bridge multi-level inverter, Optimization Methods, Switch Utilization Ratio, Total Harmonic Distortion

I. INTRODUCTION

Multi-level inverters are widely utilized in various areas like STATCOM (Static Compensators) [1], [2], machine drives [3], [4], Flexible AC Transmission Systems (FACTS) [5], and photovoltaic and wind energy applications [6], [7]. Among the different topologies and structures, owing to some characteristics like modular structure, extendibility and electromagnetic compatibility, cascaded H-bridge inverters are the most popular [8]. Different switching techniques and control algorithms are employed to control these inverters [9]-[12]. In most of these methods, the main purpose is harmonic reduction in generated output voltage. A noticeable portion of research on multi-level inverters has focused on THD minimization or improving previous harmonic rejection techniques. The adaptive harmonic elimination technique in [13] and the harmonic mitigation method for inverters with unequal DC links in [14] are among instances in this area. Based on the repetitive control algorithm, harmonic rejection in circulating current for multi-level converters is investigated in [15]. Furthermore, based on the line voltage

THD calculation, line-line harmonic minimization is presented in [16].

DC sources operation, play an important role in efficiency and operation of multi-level converters. As a result, many studies revolve around efficient control of DC links. By cascading a flying capacitor and an H-bridge inverter, a five level inverter with a single DC source is proposed in [17]. Furthermore, by using switched DC sources, a multi-level structure with reduced number of components is designed in [18]. The voltage control of capacitors by phase shift modulations in configurations which use a single DC source is discussed in [19]. Owing to the high penetration of energy conversion in renewable systems, inverters are increasingly employed as interfaces between customers and renewable energy resources. Hence, the operation and design of inverters can greatly affect the performance and cost of a system. An inappropriate design will have an adverse effect on the switch rating, DC links performance, component expenses, etc.

In this paper, a novel method for THD minimization in cascaded H-bridge inverters is presented. For a semiconductor switch, the ratio of the output transferred power to the power rating of the switch indicates how much of the switch's capability is exploited and in a typical design, the switches rating are designed conservatively for safety purposes. In this study, the SUR is defined and enhanced in

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terms of harmonic optimization for phase and line-line operations. This enhancement in the utilization ratio will reduce the DC sources. As a result, the voltage stresses, losses and lifetime of the switches will be improved. In order to attain a more effective solution for different modulation indices, alterable DC sources are utilized.

This paper is organized as follows. In Section II, the topology and switching strategies of H-bridge inverters are reviewed. SUR and THD definitions and expressions are presented in Sections III and IV. The proposed technique is explained in Section V. Simulation and experimental results are presented in Sections VI and VII. Finally, section 8 concludes the paper.

II. CASCADED H-BRIDGE MULTI-LEVEL INVERTERS

Fig. 1 shows a 7-level cascaded inverter, which is formed by series connection of H-bridges, alongside its output waveform. The output staircase voltage is generated by synthesizing the DC source voltages which feed each cell. In the first half cycle, the i^{th} cell generates one voltage level which rises at θ_i and goes down at $\pi-\theta_i$ with a magnitude of V_{DCi} . There are various methods for harmonic reduction in the output voltage of these inverters. The Optimized Minimization of THD (OMTHD) and Selective Harmonic Elimination (SHE) are examples of these methods. The OMTHD method minimizes the THD by using different optimization algorithms. On the other hand, a set of nonlinear equations, which contain lower order harmonics are solved in the SHE method to eliminate harmonics in the output waveform. Efficient operation of the inverters is not considered in the discussed methods which can degrade the performance of the system. In addition, the DC link converters, switch ratings, and cost of the system can be affected by inefficient control and operation of the inverters in the above mentioned methods.

III. SWITCH UTILIZATION RATIO IN H-BRIDGE INVERTERS

Intermediate converters play a major role in the performance of energy systems and the cost of produced energy. The SUR in a converter represents the ratio of the delivered energy and the power rating of the utilized semiconductor switches. In order to efficiently exploit the power handling capability of switches and to enhance the amount of delivered energy in a typical converter, utilization ratio optimization must be considered. Furthermore according to the SUR formula, SUR enhancement diminishes the DC links which in turn lowers the voltage stresses and losses and improves the lifetime of an inverter.

In order to define a formula for the SUR, it is assumed that the load is inductive enough and that its current is sinusoidal. The output rms volt-ampere at the fundamental frequency and

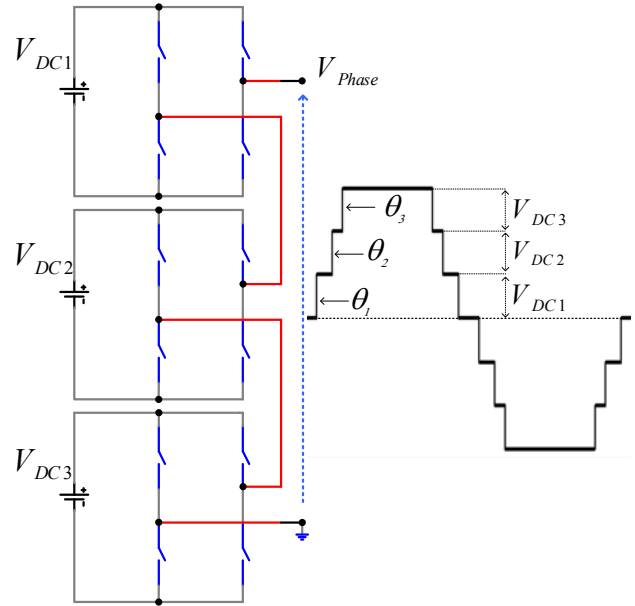


Fig. 1. 7-level cascaded H-bridge inverter configuration.

maximum loading is $V_{fund} \times I_{max}$ in the SUR formula which is defined in (1).

$$SUR = \frac{V_{fund} \times I_{max}}{4 \sum_{i=1}^N V_{Ti} I_{Ti}} \quad (1)$$

Here V_{fund} is the rms voltage, and I_{max} is the rms current both at a 50 Hz frequency and maximum rated output. N is the cell numbers, and V_{Ti} and I_{Ti} are the rating voltage and current of the i^{th} cell. It should be noted that for safe operation of the inverter, oversize coefficients are considered for the rating voltage and current. In this paper, these coefficients are set to 1.25. However, they are not shown for the sake of simplicity.

A. Phase Operation Utilization Ratio

In this section, the SUR formula is defined for single phase operation. Expression (2) is written for the output voltage of a 7-level inverter according to the Fourier expansion. The fundamental rms phase voltage is also expressed in (3).

$$V_n = \frac{4}{n\pi} [V_{dc1} \cos(n\theta_1) + V_{dc2} \cos(n\theta_2) + V_{dc3} \cos(n\theta_3)] \quad (2)$$

$$V_{rms}^{p1} = \frac{2\sqrt{2}}{\pi} [V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3)] \quad (3)$$

In equation (4), the per unit value for the phase voltage main component is obtained.

$$V_{p.u.}^{p1} = \frac{V_{rms}^{p1}}{6\sqrt{2}} = \frac{V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3)}{3} \quad (4)$$

The value of V_{Ti} in each H-bridge is equal to its feeding source and is based upon each cell's DC link. The value of I_{Ti} is also defined as:

$$I_{Ti} = \sqrt{2}I_{max} \quad (5)$$

Where I_{max} is the maximum rms current at the fundamental frequency. Finally, by substituting (3) and (5) into equation (1), the phase SUR is obtained (6).

$$SUR_{phase} = \frac{V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3)}{2\pi(V_{dc1} + V_{dc2} + V_{dc3})} \quad (6)$$

B. Line operation utilization ratio

The line voltage rms value is expressed in (7) and is different from the phase voltage in a $\sqrt{3}$ coefficient. The per unit value of the line voltage is also defined in (8).

$$V_{rms}^{l1} = \sqrt{3}V_{rms}^{p1} = \frac{2\sqrt{6}}{\pi} [V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3)] \quad (7)$$

$$V_{p.u.}^{l1} = \frac{\pi V_{rms}^{l1}}{6\sqrt{6}} = \frac{V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3)}{3} \quad (8)$$

The V_{Ti} in the line SUR is similar to the phase section and is equal to its feeding DC link. In addition, I_{Ti} is $\sqrt{2}$ times greater than I_{max} . Finally, the line SUR is expressed in equation (9).

$$SUR_{line} = \frac{\sqrt{3}V_{rms}^{l1}}{12\sqrt{2}(V_{dc1} + V_{dc2} + V_{dc3})} \quad (9)$$

By substituting (7) into (9), the line SUR is obtained which according to (10) is equal to the phase SUR.

$$SUR_{line}(\theta_1, \theta_2, \theta_3) = SUR_{phase}(\theta_1, \theta_2, \theta_3) \quad (10)$$

IV. TOTAL HARMONIC DISTORTION

The phase and line voltage THD of a 7-level inverter is formulized in this section. According to (11), the THD for a waveform is defined as the ratio of all of the harmonic components and the fundamental rms value.

$$THD = \sqrt{\left(\frac{V_{rms}^2 - V_{1,rms}^2}{V_{1,rms}^2} \right)} \quad (11)$$

A. Phase Operation THD

The phase voltage rms can be obtained by taking the integral of the output voltage as expressed in (12).

$$V_{rms}^{phase} = \sqrt{\frac{\left(V_{dc1}^2 (\theta_2 - \theta_1) + (V_{dc1} + V_{dc2})^2 (\theta_3 - \theta_2) + (V_{dc1} + V_{dc2} + V_{dc3})^2 \left(\frac{\pi}{2} - \theta_3 \right) \right)}{\pi/2}} \quad (12)$$

By substituting (3) and (12) into formula (11), the phase voltage THD is obtained (13).

$$THD_{phase} =$$

$$\sqrt{\frac{\left(V_{dc1}^2 (\theta_2 - \theta_1) + (V_{dc1} + V_{dc2})^2 (\theta_3 - \theta_2) + (V_{dc1} + V_{dc2} + V_{dc3})^2 \left(\frac{\pi}{2} - \theta_3 \right) \right)}{\left(V_{dc1} \cos(\theta_1) + V_{dc2} \cos(\theta_2) + V_{dc3} \cos(\theta_3) \right)^2}}^{-1} \quad (13)$$

B. Line Operation THD

The line voltage of an H-bridge inverter, equation (14), does not have a constant form at different switching angles. However, it is possible to integrate its waveform and obtain an rms value similar to [16], which can be expressed by (15). V_a and V_b are the phase voltages with a 120° phase difference. By substituting (7) and (15) into (11), the THD of the line voltage is calculated and expressed in (16).

$$V_{line}(\theta) = V_a^{phase}(\theta) - V_b^{phase}(\theta) \quad (14)$$

$$V_{rms}^{line} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V_{line}^2(\theta) d\theta} \quad (15)$$

$$THD_{line} = \sqrt{\left(\frac{V_{rms,line}^2 - V_{rms,L1}^2}{V_{rms,L1}^2} \right)} \quad (16)$$

V. PROPOSED TECHNIQUE FOR SUR CONSIDERATION IN HARMONIC OPTIMIZATION

In this section, the proposed technique for utilization ratio enhancement is investigated. This method is based on minimizing an objective function which simultaneously optimizes the THD and the SUR. To achieve this goal, two approaches are proposed in this paper. In the first approach, an objective function that contains the fundamental component adjustment, the THD, and the SUR inverse formula is minimized for each modulation index. This approach is called the Variable Modulation (VM) index method. On the other hand, in the second technique, the objective function considers only the THD and SUR inverse formula, and the optimal index is obtained as a result of the optimization. In this method, which is called the Constant Modulation (CM) index technique, the obtained results are applied for the entire range of the output voltage.

A. Variable Modulation (VM) Index Method

As mentioned before, the objective function in this method contains three main parts. The first one is the fundamental component adjustment formula in which the subtraction of the desired modulation index from the fundamental voltage component is considered. The THD and the inverse value of the SUR are the 2nd and 3rd part of this objective function,

respectively. This formula is expressed as follows:

$$\begin{aligned} \text{Obj. Function} = & 10 \times |M - V_1| \\ & + |THD| + \left| \frac{1}{SUR} \right| \end{aligned} \quad (17)$$

The 10 coefficient in (17) is for emphasizing the fundamental component adjustment versus the THD and SUR optimizations. The following constraint must be satisfied by the obtained switching angles.

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \frac{\pi}{2} \quad (18)$$

Where θ_i denotes the switching angles in radians. In this method, the objective function must be minimized in each predefined M . Furthermore, based on the operation of the inverter, a suitable formula for the THD (single phase or three-phase) must be replaced in (17). Finally, after achieving results, in order to obtain different output voltages, the values of the switching angles and DC sources, which are between 0 and 1^{p.u.} must be altered according to the obtained results.

B. Constant Modulation (CM) Index Method

In the CM approach, the proposed objective function considers the THD and the inverse value of the SUR. The main difference between this method and the first proposed approach is that in the first one, the minimization is applied to the objective function for each predefined M while in this technique, the minimization is executed one time and the obtained optimum DC source values and switching angles are utilized for the all values of the output voltage. The suggested objective function for this technique is expressed in (19).

$$\text{Obj. Function} = |THD| + \left| \frac{1}{SUR} \right| \quad (19)$$

Like the first approach, the constraint for the switching angles presented in (18) must be satisfied. After optimization, the results can only be used in a certain M which is obtained by optimization. In order to operate at a different output voltage, the DC sources must be altered according to expression (20).

$$V_{dc\ i}^{new} = \frac{V_{dc\ i}^{old}}{\sum_{i=1}^3 V_{dc\ i}^{old}} \times \frac{M^{new}}{M^{old}} \quad (20)$$

Where $V_{dc\ i}^{new}$ is the updated value for the i^{th} DC source, $V_{dc\ i}^{old}$ is the value of the i^{th} DC source obtained by minimization, and M^{new} and M^{old} are the desired and the old modulation indices, respectively. The generated switching angles remain unchanged which produces constant THD and SUR in different output voltages.

VI. SIMULATION RESULTS

In this section, a simulation is performed based on the suggested algorithms. Due to the non-linear nature of the suggested functions, the Genetic Algorithm (GA) which is a powerful evolutionary optimization method is employed. The GA method produces a solution for optimization problems by using techniques, which are inspired by natural evolution. In this method, a population of initial solutions to a problem (usually a target function) is evolved and eventually the best solution is achieved. In this paper, the population size is equal to 20 and the number of generations is set to 1000. In order to get a better comparison, the CM algorithm is also performed without SUR consideration and results obtained by the OMTHD with constant DC links are presented. The mentioned techniques are thoroughly compared in terms of the phase and line operations of the inverter to demonstrate the effectiveness of the suggested schemes.

A. Single Phase Operation

1) *Variable Modulation (VM) Technique*: In the suggested objective function (17), the values of V_1 , SUR, and THD are replaced with (4), (6) and (13) respectively. The value of M can vary from 0 to 1 and the objective function is minimized over the all of the values of M . The obtained optimum switching angles, DC sources and output voltage adjustments are depicted in Fig. 2(a), (b) and (c), respectively. The utilization ratio versus the output per unit voltage is plotted in Fig. 4. The utilization factor is between 0.09 and 0.101 over the entire range of the output voltage. According to Fig. 3(a), the harmonic level is lower than 15% for voltages from 0.1 to 0.9, and it reaches higher values at the unity voltage.

2) *Constant Modulation (CM) Technique*: In this scheme, the SUR is maximized in the harmonic optimization. The main component adjustment is not considered in the objective function and the optimum modulation index is one of the obtained solutions. By substituting (6) and (13) into equation (19), the optimum switching angles, DC sources, THD, SUR and modulation indexes are tabulated in Table. I.

3) *Analysis and Comparison*: A comparison of the results obtained by four methods is presented in this section including; 1) the standard OMTHD with constant DC sources, 2) the CM method without SUR consideration, 3) the proposed CM technique and 4) the proposed VM technique. The THD and SUR values obtained by these methods are depicted in Fig. 3(a) and (b). Comparing these results indicates that standard OMTHD produces higher THD in comparison with the other approaches. The SUR values obtained with this method are also lower than the other approaches for voltages under 0.8 and the difference is significant at lower p.u. voltages. The two proposed SUR optimization techniques (CM and VM) produce same THD and SUR for lower output voltages. Meanwhile at higher

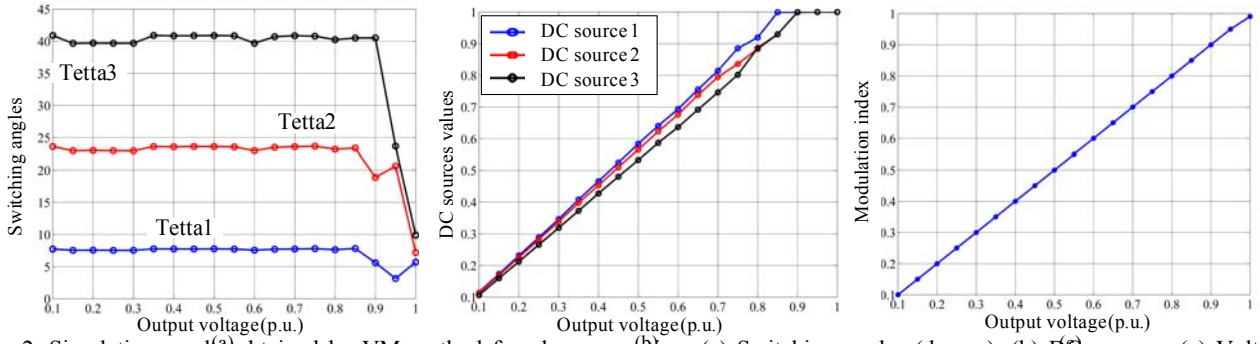


Fig. 2. Simulation results obtained by VM method for phase operation: (a) Switching angles (degree); (b) DC sources; (c) Voltage adjustment.

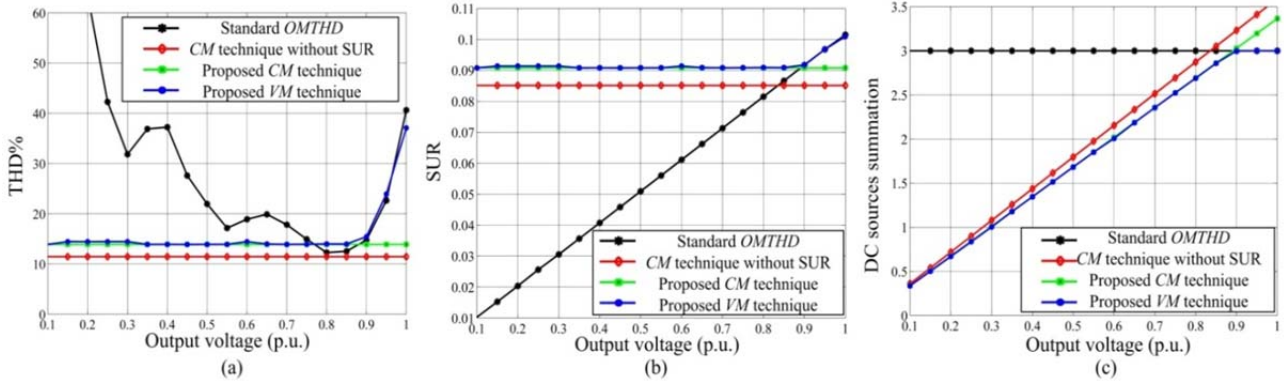


Fig. 3. Comparison between the results obtained by 4 techniques for phase operation: (a) THD; (b) SUR; (c) Summation of DC sources.

TABLE I

OPTIMUM PARAMETERS OBTAINED BY CM METHOD (PHASE OPERATION)

Optimum Modulation Index= 0.53						THD%	SUR
Switching angles (degree)			DC sources (p.u.)				
θ_1	θ_2	θ_3	V_{DC1}	V_{DC2}	V_{DC3}		
7.73	23.60	40.88	0.62	0.60	0.57	13.91	0.0908

TABLE II

COMPARISON BETWEEN OBTAINED RESULTS BY PROPOSED CM METHOD AND CM METHOD WITHOUT SUR CONSIDERATION (PHASE OPERATION)

Methods	THD%	SUR	DC sum
Proposed CM method	13.91	0.0908	2.356
CM method without SUR	11.47	0.0851	2.513

voltages, the CM method is more effective from the harmonic point of view. Finally, a summation of the DC source values is plotted in Fig. 3(c), which is constant in the standard OMTD and higher in the other methods at all voltages under 0.8. At lower voltage levels, the two proposed approaches show the same performance while at higher voltages, the proposed VM is preferred. The DC source summation of the CM method without SUR optimization is always higher than the two proposed methods.

The THD, SUR, and DC link summations obtained by the CM method are presented in Table. II for both with and without the SUR cases. An increase in the THD (2.44%) is observed when the SUR is considered and it can be seen that the SUR is enhanced about 6.69% and the DC sum is decreased 6.37% at an output voltage of 0.7.

B. Line-Line Operation

1) *Variable Modulation (VM) Technique:* Like the phase section, the V_i , SUR, and THD in function (17) are substituted

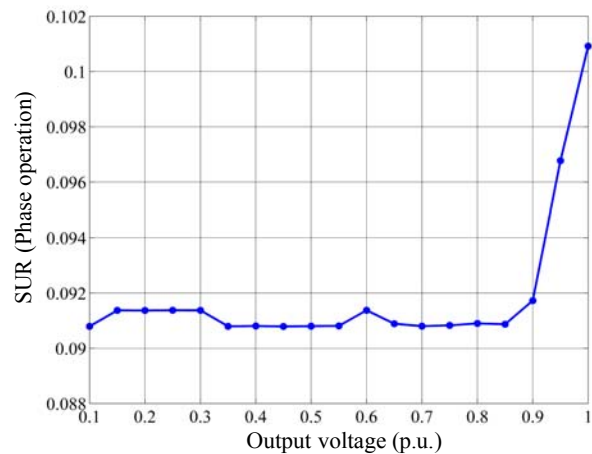


Fig. 4. SUR obtained by proposed VM method for phase operation.

with (8), (9), and (16), respectively. Having M varied between 0 and 1, the function is minimized. The optimum switching angles, DC sources, and output voltage adjustments

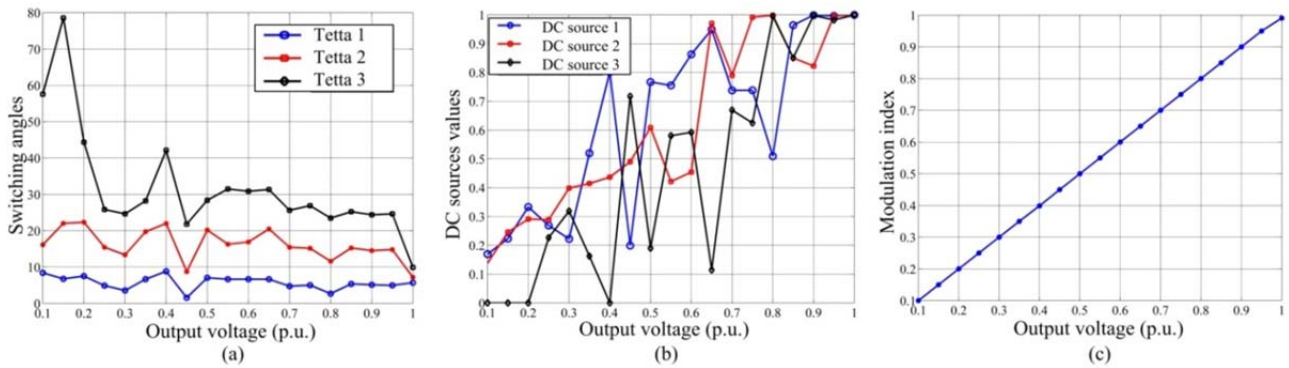


Fig. 5. Simulation results obtained by VM method for line operation: (a) Switching angles (degree);(b) DC sources;(c) Voltage adjustment.

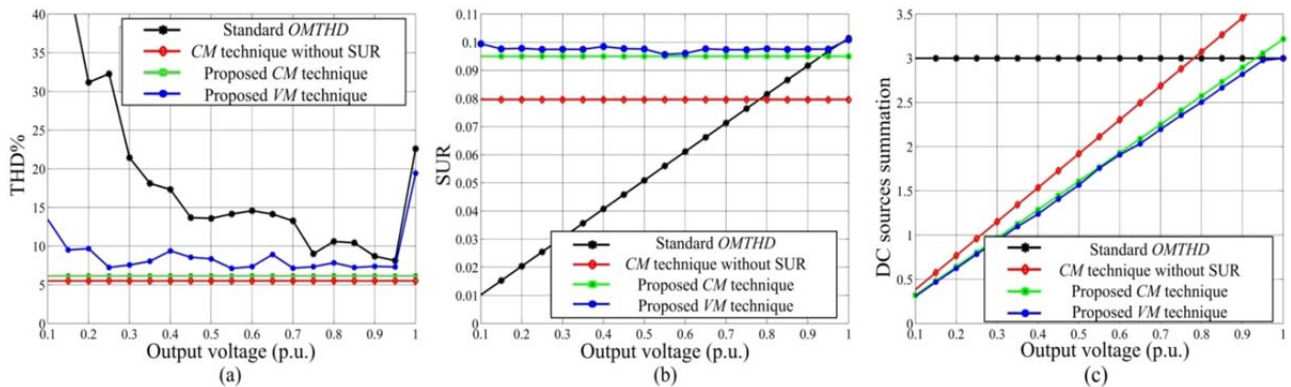


Fig. 6. Comparison between the results obtained by 4 techniques for line operation: (a) THD; (b) SUR; (c) Summation of the DC sources.

are shown in Fig. 5(a), (b), and (c), respectively. The SUR values are plotted in Fig. 7. Regarding the figures, the obtained SUR is between 0.0950 and 0.101 and the THD is below 14% for most of the output voltages.

2) *Constant Modulation (CM) Technique*: By replacing the SUR and THD expressions in (19) by (9) and (16), the appropriate switching angles and DC sources are achieved. These values, along with the obtained results, are expressed in Table. III.

3) *Analysis and Comparison*: In order to get a better understanding of the obtained results, in the same manner as the phase section, the four methods are compared. The harmonics and SUR obtained by the four methods are depicted in Fig. 6(a) and (b). It can be seen that the OMTHD technique is less effective compared to the other approaches. Between the two suggested schemes, the CM method has lower harmonic levels than the VM method, while the SUR has greater values in the VM. According to the harmonic and SUR diagram, by adding a utilization ratio to the objective function, the harmonics are not affected while the SUR is enhanced strikingly. In Table IV, the obtained results in the presence and absence of the SUR constraint are presented. It can be seen from Table 4 that by considering the utilization ratio, there is a negligible increase (0.67%) in the line THD. Meanwhile, this method enhances the SUR by at least 19.3%.

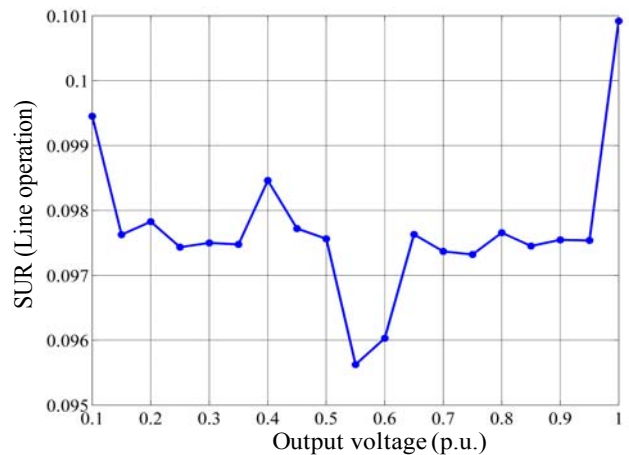


Fig. 7. SUR obtained by proposed VM method for line operation.

TABLE III
OPTIMUM PARAMETERS OBTAINED BY CM METHOD
(LINE OPERATION)

Optimum Modulation Index = 0.61							
Switching angles (degree)			DC sources (p.u.)			THD%	SUR
θ_1	θ_2	θ_3	V_{DC1}	V_{DC2}	V_{DC3}		
5.55	16.89	33.55	0.69	0.68	0.60	6.19	0.0949

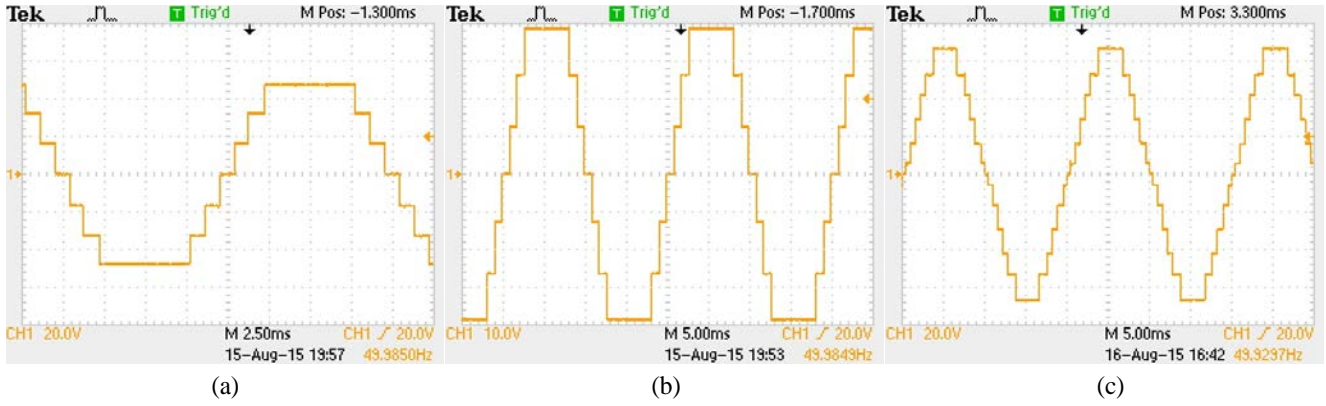


Fig. 8. Experimental results for 7-level inverter based on Table V: (a) Phase voltage obtained by CM method implemented in phase operation (Time/Div: 2.5 ms, Volt/Div: 20 Volts); (b) Phase voltage obtained by CM method implemented in phase operation (Time/Div: 5 ms, Volt/Div: 10 Volts); (c) Line voltage obtained by CM method implemented in line operation (Time/Div: 5 ms, Volt/Div: 20 Volts).

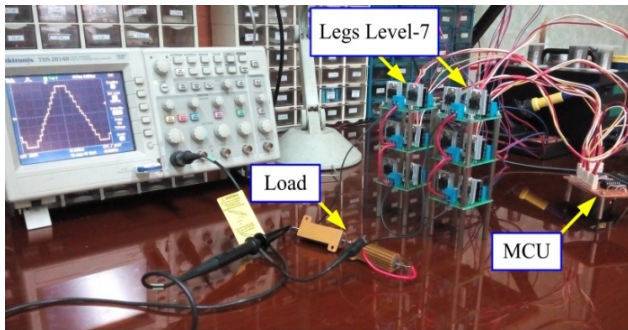


Fig. 9. Experimental setup of the cascaded H-bridge inverter.

TABLE IV
COMPARISON BETWEEN OBTAINED RESULTS BY PROPOSED CM METHOD AND CM METHOD WITHOUT SUR CONSIDERATION (LINE OPERATION)

Methods	THD%	SUR	DC sum
Proposed CM method	6.19	0.0950	2.252
CM method without SUR	5.52	0.0796	2.689

TABLE V
SWITCHING ANGLES, DC SOURCES VALUES AND EXPERIMENTAL THD OBTAINED BY PROPOSED CM METHOD

Case	Switching Angles(degree)			DC Sources(p.u.)			THD %
	θ_1	θ_2	θ_3	V_{DC1}	V_{DC2}	V_{DC3}	
Phase	7.7 3	23.60	40.8 8	16.5	16	15	13.97
Line	5.5 5	16.89	33.5 5	13.3	13.2	11.6	6.22

This noticeable utilization ratio enhancement improves the converters performance in an economic manner and shows that the method is effective. The total values of the DC links are also shown in Fig. 6(c). The DC sources in the OMTHD are constant. Meanwhile, in the proposed methods, it has

smaller values. The difference in the DC sources obtained by the CM techniques with and without SUR consideration is more noticeable at higher output voltages. According to Table IV, the DC links are decreased more than 16% at an output voltage of 0.7. This has a strong effect on reducing the voltage stress and losses and in improving the components lifetime.

VII. EXPERIMENTAL RESULTS

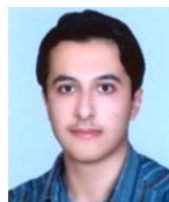
In order to verify the obtained results, experimental tests are performed on a cascaded H-bridge 7-level inverter. The experimental setup is depicted in Fig. 9. An ATMEGA-8 is utilized as a controller to generate the gating signals. In order to convert the control signals into higher current and voltage levels, dual power MOSFET drivers are utilized. A 6N137 optocoupler is also employed in this design. The maximum voltage of each cell is 75 Volts, which is specified based on the maximum stress of the switches. The CM method is performed for phase and line-line operations of the inverter, and the measured THDs are presented in Table 5. Fig. 8(a) shows the voltage of the inverter in single phase operation with the dc levels presented in Table 5. Fig. 8(b) shows the voltage of the inverter with a 20% reduction in the levels presented in Fig. 8(a). Fig. 8(c) shows the line voltage of the inverter in line operation. As can be seen, the line voltage (Fig. 8(c)) reaches 13 levels which implies that the harmonics are effectively eliminated. Based upon the obtained harmonic values, which are presented in simulation section (Table I and III), the measured harmonics in the experiments show little deviation from the calculated THDs. According to the obtained results, the proposed technique for SUR enhancement does not degrade the harmonic minimization, specifically in 3 phase applications. In addition, it noticeably improves the utilization ratio and DC source values, which has a great effect on switch losses and stresses as well as the inverter performance.

VIII. CONCLUSION

In this paper, a new technique for converter utilization ratio enhancement in the harmonic optimization of cascaded H-bridge 7-level inverters is proposed. The new method simultaneously optimizes the SUR and THD. It also utilizes the power handling capability of the switches effectively while eliminating the output voltage harmonics. Moreover, by the SUR enhancement, the DC source values are reduced. This has a direct effect on the switches losses and voltage stresses. This in turn strikingly improves the lifetime of the converter. A comparison between the methods demonstrates the effectiveness of the methods especially in line-line operation. Simulations are presented and experiments are used to validate the obtained results.

REFERENCES

- [1] H. M. Pirouz and M. T. Bina, "Modular multilevel converter based STATCOM topology suitable for medium-voltage unbalanced systems," *Journal of Power Electronics*, Vol. 10, No.5, pp. 572-578, Sep. 2010.
- [2] L. Haw, M. Dahidah, and H. Almurib, "SHE-PWM Cascaded Multilevel Inverter With Adjustable DC Voltage Levels Control for STATCOM Applications," *IEEE Trans. Power Electron.*, Vol. 29, No.12, pp. 6433-6444, Dec. 2014.
- [3] N.K. Kumar and K. Sivakumar, "A quad two-level inverter configuration for four-pole induction-motor drive with single DC link," *IEEE Trans. Ind. Electron.*, Vol. 62, No.1, pp. 105-112, Jan. 2015.
- [4] R. Kaarthik, K. Gopakumar, J. Mathew, and T. Undeland, "Medium-voltage drive for induction machine with multilevel dodecagonal voltage space vectors with symmetric triangles," *IEEE Trans. Ind. Electron.*, Vol. 62, No.1, pp. 79-87, Jan. 2015.
- [5] J. Chivite-Zabalza, P. Izurza-Moreno, D. Madariaga, G. Calvo, and M. Rodríguez, "Voltage balancing control in 3-level neutral-point clamped inverters using triangular carrier PWM modulation for FACTS applications," *IEEE Trans. Power Electron.*, Vol. 28, No.10, pp. 4473-4484, Oct. 2013.
- [6] L. Yushan, B. Ge, H. Abu-Rub, and F. Peng, "An effective control method for three-phase quasi-z-source cascaded multilevel inverter based grid-tie photovoltaic power system," *IEEE Trans. Ind. Electron.*, Vol. 61, No.12, pp. 6794-6802, Dec. 2014.
- [7] C. Gu, H. S. Krishnamoorthy, P. N. Enjeti, Z. Zheng, and Y. Li, "A medium-voltage matrix converter topology for wind power conversion with medium frequency transformers," *Journal of Power Electronics*, Vol.14, No.6, pp. 1166-1177, Nov. 2014.
- [8] M. Malinowski, K. Gopakumar, J. Rodriguez, M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No.7, pp. 2197-2206, Jul. 2010.
- [9] C. Buccella, C. Cecati, M. G. Cimatorini, and K. Razi, "Analytical method for pattern generation in five-level cascaded H-bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 11, pp. 5811-5819, Nov. 2014.
- [10] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, "Elimination of low order harmonics in multilevel inverters using genetic algorithm," *Journal of Power Electronics*, Vol. 11, No. 2, pp. 132-139, Mar. 2011.
- [11] B. Jacob and M. R. Baiju, "A new space vector modulation scheme for multilevel inverters which directly vector quantize the reference space vector," *IEEE Trans. Ind. Electron.*, Vol. 62, No.1, pp. 88-95, Jan. 2015.
- [12] W. Jiang, W. Li, Z. Wu, Y. She, and Z. Tao, "Space-vector pulse-width modulation algorithm for multilevel voltage source inverters based on matrix transformation and including operation in the over-modulation region," *IETPower Electron.*, Vol. 7, No.12, pp. 2925-2933, Dec. 2014.
- [13] F. Filho, H. Z. Maia, T. H. A. Mateus, B. Ozpineci, L. M. Tolbert, and J. O. P. Pinto, "Adaptive selective harmonic minimization based on ANNs for cascade multilevel inverters with varying DC sources," *IEEE Trans. Ind. Electron.*, Vol. 60, No.5, pp. 1955-1962, May 2013.
- [14] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler, and M. A. Aguirre, "Selective harmonic mitigation technique for cascaded H-bridge converters with non-equal DC link voltages," *IEEE Trans. Ind. Electron.*, Vol. 60, No.5, pp. 1963-1971, May 2013.
- [15] B. Li, D. Xu, and D. Xu, "Circulating current harmonics suppression for modular multilevel converters based on repetitive control," *Journal of Power Electronics*, Vol. 14, No.6, pp. 1100-1108, Nov. 2014.
- [16] N. Yousefpoor, S.H. Fathi, N. Farokhniaand, and H. A. Abyaneh, "THD minimization applied directly on the line-to-line voltage of multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 373-380, Jan. 2012.
- [17] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3505-3512, Aug. 2012.
- [18] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, Vol. 61, No.7, pp. 3269-3278, Jul. 2014.
- [19] H. Sepahvand, L. Jingsheng, M. Ferdowsi, and K.A. Corzine, "Capacitor voltage regulation in single-dc-source cascaded H-bridge multilevel converters using phase-shift modulation," *IEEE Trans. Ind. Electron.*, Vol. 60, No.9, pp. 3619-3626, Sep. 2013.



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