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# Carrier Based Common Mode Voltage Reduction Techniques in Neutral Point Clamped Inverter Based AC-DC-AC Drive System

Amit Ojha[†], Pradyumn Chaturvedi[*], Arvind Mittal[**], and Shailendra Jain[***]

[†,***]Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal,India
[*]Dept. of Electrical and Electronics Eng., Birla Institute of Technology and Science, Pilani, India
[**]Energy Centre, Maulana Azad National Institute of Technology, Bhopal, India

## Abstract

Common mode voltage (CMV) generation is a major problem in switching power converter fed induction motor drive systems. CMV is the zero sequence voltage generated due to the switching action of power converters. Even a small magnitude of CMV with a high rate of change may circulate large bearing currents which may damage a machine's bearings and shorten its life. There are several methods of controlling CMV. This paper presents 3-level sinusoidal pulse width modulation based techniques to control the magnitude and rate of change of CMV in multilevel AC-DC-AC drive systems. Simulation and experimental investigations have been presented to validate the performance of proposed technique to control CMV in 3-level neutral point clamped inverter based AC-DC-AC system.

**Key words:** AC-DC-AC Drives, Common Mode Voltage Control, Neutral Point Clamped Inverter, Switching Converters

## I. INTRODUCTION

Energy saving has become apriority in industrialized countries nowadays. About 70% of the total generated electric energy is utilized by electrical motors. This fact draws attention for energy saving in AC-DC-AC drive systems. Variable voltage and variable frequency ac supply is required to feed induction motors to achieve energy efficient operation of various industrial applications. At a medium voltage, high power level, AC-DC-AC drive systems face practical problems related to the switching action of converters. Fig. 1 shows a basic block diagram of an AC-DC-AC drive system to generate variable voltage, variable frequency supply to feed a 3-phase induction motor. In such systems, voltage control is achieved at the front end converter side and frequency control is achieved at the inverter side. Therefore, it is mandatory to use two converters before the power is fed to the induction motor. Conventional 2-level converters suffer from the drawbacks of large *dv/dt* stresses across devices, more switching losses, large harmonic contents and common mode voltage generation.

The generation of common mode voltage (CMV) can damage the motor winding insulation if not properly controlled or mitigated. It results in motor bearing currents leading to bearing failures. It can also generate motor shaft voltages, bearing currents, and conducted electromagnetic interference [1], [2].

The common mode voltage generated at the front end converter side, inverter side and motor side can be controlled by adding extra hardware circuitry (such as an isolation transformer, zero-sequence impedance/common mode choke, active and passive filters, dual bridge inverter, four-leg inverter, etc.) or by modifying the control strategy [3],[4]. Adding extra hardware to the circuitry results in reduced system reliability, increased cost and a less fault tolerant system. Several authors have presented different modified control strategies based on the sinusoidal pulse width

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[†]Corresponding Author: pc220774@gmail.com
Tel: +917732893208, Maulana Azad National Institute of Technology
[*]Dept. of Electrical and Electronics Eng., Birla Institute of Technology and Science, India
[**]Energy Centre, Maulana Azad National Institute of Technology, India
[***]Department of Electrical Engineering, Maulana Azad National Institute of Technology, India

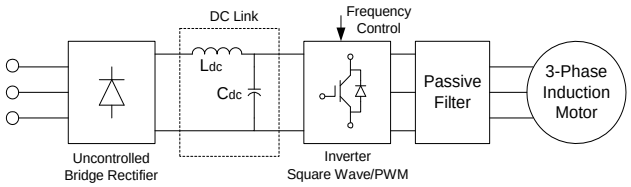



Fig. 1. Voltage and frequency control in AC-DC-AC induction motor drive.

modulation (SPWM) technique [5],[6] and the space vector pulse width modulation (SVPWM) technique. These SVPWM techniques include the nearest three vector selection (NTV) SVPWM, radial state SVPWM, zero common mode voltage SVPWM [7]-[11], etc. However, the SVPWM based CMV reduction techniques require comparatively complex algorithms [2], [9], and [12]-[14]. Simple carrier based techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD) and the addition of offset to the modulating signal have been presented in [15], [16] for controlling CMV in the output of inverter terminals. However, the techniques presented in these papers are used for multilevel inverters (MLI).

This paper investigated the effect of the amount of phase shift between the carriers and modulating signal, and the impact of the modulation index on inverter performance in terms of CMV. The amount of phase shift between the carriers and the modulating signal plays a very important role in determining inverter performance. This paper investigates the effect of the phase shift angle between the carrier and the modulating signal on the inverter output voltage and CMV (in terms of the number of switching per cycle) performance and implements the concept of adding an offset to the modulating signal as presented in [15] to reduce CMV and its rate of change for AC-DC-AC drive systems. The impact of change of the modulation index in terms of CMV is presented which effectively improves the system efficiency.

The paper is organized in five Sections. Section II presents a mathematical model to explain the causes of CMV generation in AC-DC-AC drive systems. It also provides the relation of CMV with leakage current. Section III presents the proposed concept to control CMV and its rate of change along with the effects of phase shift between the carriers and the modulating signal on inverter performance. The simulation performance of the proposed control technique is given in Section IV. Experimental verification of proposed technique is presented in Section V, followed by some conclusions and advice in Section VI.

## II. CAUSES OF COMMON MODE VOLTAGE

Fig. 2(a) shows a general block diagram of an AC-DC-AC induction motor drive system. The front end converter may be an uncontrolled or controlled voltage source or a current source rectifier, while the motor side converter can be a conventional two-level or multilevel VSI, CSI. In the VSI fed drive, the DC link capacitor $C_d$ ($C_1$ and $C_2$) is sufficiently large and a DC link inductor $L_d$ is not required, whereas in the CSI fed drive, $L_d$ is sufficiently large and $C_d$ is not needed.

In Fig. 2(a),

$V_{PG}$& $V_{NG}$: Voltages at the positive and negative dc link with respect to the ground

$V_{OG}$: Common mode voltage produced by the rectifier

$V_{nO}$: Voltage between the neutral of the stator winding and the midpoint of the dc link (common mode voltage produced by the inverter)

The total common mode voltage (i.e. the motor neutral to utility ground voltage, $V_{nO}$) generated by the rectification and inversion process is given by:

$$V_{nG} = V_{cm} = V_{cm}(\text{Re } ctifier) + V_{cm}(Inverter) \quad (1)$$

where,

$$V_{cm}(\text{Re } ctifier) = V_{oG} = (V_{PG} + V_{NG})/2 \quad (2)$$

$$V_{cm}(Inverter) = V_{no} = (V_{nP} + V_{nN})/2 \quad (3)$$

The total common mode voltage can also be represented as,

$$V_{nG} = V_{no} + V_{oG} \quad (4)$$

The motor line-to-ground voltage is:

$$V_{RG} = V_{Rn} + V_{nG} = V_{Rn} + V_{cm} \quad (5)$$

Fig. 2(b) shows block diagram of a AC-DC-AC NPC VSI fed ASD with a 12-pulse front end diode bridge rectifier. The input transformer has two secondary with 30° phase shift between them.

The common mode equivalent circuit of a NPC inverter is shown in Fig. 2(c) for common mode voltage analysis. The common mode voltage at motor terminals is,

$$V_{cm} = \frac{V_{Rg} + V_{Yg} + V_{Bg}}{3} \quad (6)$$

where,

$$\left.\begin{aligned} V_{Rg} &= V_{Ro} + V_{og} \\ V_{Yg} &= V_{Yo} \_ V_{og} \\ V_{Bg} &= V_{Bo} + V_{og} \end{aligned}\right\} \quad (7)$$

Therefore,

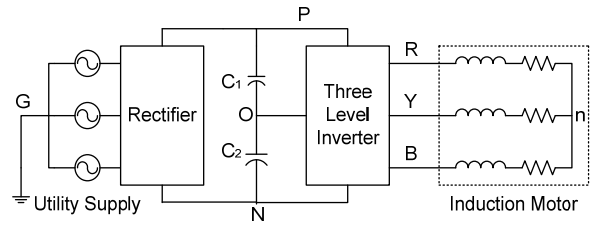
$$V_{cm} = \frac{V_{Ro} + V_{Yo} + V_{Bo}}{3} + V_{og} \quad (8)$$

Now $V_{og}$ is the common mode voltage at the rectifier terminals, which can be calculated from Fig. 2(c) as,

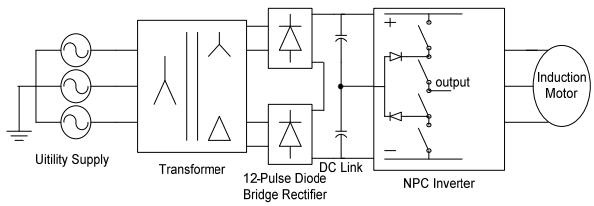
$$V_{ab} = V_{aP} - V_{bP} \quad (9)$$

$$V_{bc} = V_{bN} - V_{cN} \quad (10)$$

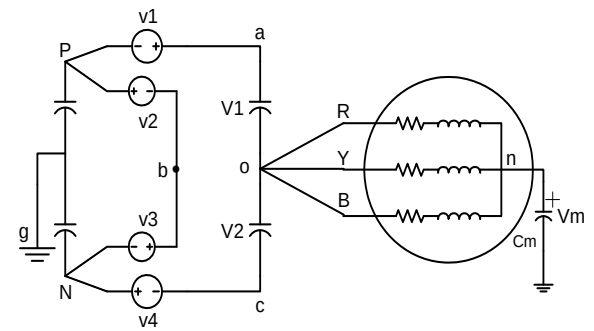
$$V_{ac} = V_{ab} - V_{bc} \quad (11)$$



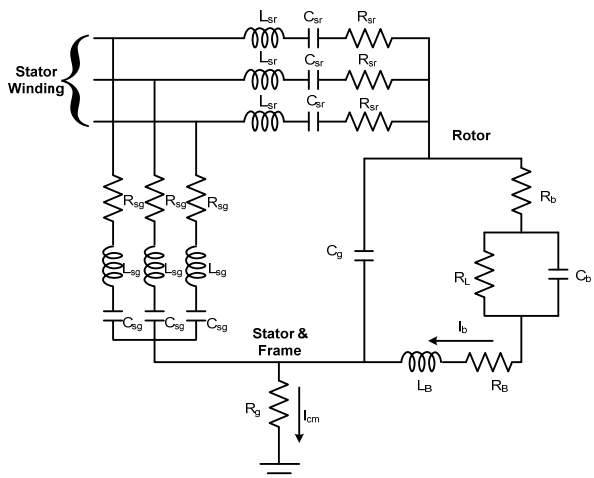

(a)



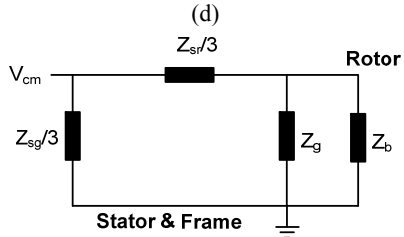

(b)




(c)




(d)




(e)

Fig. 2. (a) General block diagram of AC-DC-AC VSI fed ASD. (b) Block diagram of AC-DC-AC NPC VSI fed ASD with 12-pulse front end diode bridge rectifier. (c) Common mode equivalent circuit of medium voltage NPC inverter fed ASD system. (d) High frequency model of 3-phase induction motor (17). (e) Simplified per phase model of induction motor.

$$V_{ao} = \frac{V_{ac}}{2} = \frac{V_{ab} + V_{bc}}{2} \tag{12}$$

Substituting (9) and (10) into (12) yields,

$$V_{ao} = \frac{V_{aP} - V_{bP} + V_{bN} - V_{cN}}{2} \tag{13}$$

$$V_{Pg} = \frac{V_{Pb} + V_{bN}}{2} \tag{14}$$

$$V_{og} = V_{pg} + V_{aP} - V_{ao} \tag{15}$$

$$V_{og} = \frac{V_{aP} + V_{cN}}{2} \tag{16}$$

This is the common mode voltage at the rectifier terminals. The common mode voltage (CMV) can damage the motor winding insulation if not properly mitigated. In addition, the CMV between the motor neutral and the ground may cause induced shaft voltages, bearing currents and circulating bearing currents.

The relation between the CMV and the leakage current can be deduced considering the high frequency model of a 3-phase induction motor shown in Fig.2(d). The distributing parameters representing the HF coupling between the stator and rotor assembly are $R_{sr}$, $L_{sr}$ and $C_{sr}$. Considering the insulation effect of the bearing grease and the electric discharge (EDM) effect between the bearing balls and the races, the capacitance $C_b$ in parallel to the non-linear resistive circuit ($R_L$) and in series with the bearing ball and race contact resistance $R_b$ can be modelled for the motor bearings. The bearing current $I_b$ flows through the modelled wire impedance used for measuring the bearing current ($L_B$ and $R_B$). The capacitance between the stator and the motor lamination across the motor air gap is represented by $C_g$. $R_{sg}$, $L_{sg}$ and $C_{sg}$ are considered as the couplings between the stator winding and the frame (stator) since it mainly contributes the total leakage current to the ground. The frame is modelled as the resistance of $R_g$ to the ground.

The shaft voltage can be calculated by considering the simplified per phase model of the induction motor shown in Fig. 2(e).

$$V_{sh} = V_{CM} \times \frac{Z_{rg}}{\frac{Z_{sr}}{3} + Z_{rg}} \tag{17}$$

Where $Z_{sr}$ is the impedance between the stator windings and the rotor, and the impedance between the rotor and the frame ($Z_{rg}$) is defined as:

$$Z_{rg} = \frac{Z_g \times Z_b}{Z_g + Z_b}, Z_{sr} = R_{sr} + JL_{sr}\omega + \frac{1}{JC_{sr}\omega} \tag{18}$$

Where Zb and Zg can be calculated as,

$$Z_b = \frac{R_L \times \frac{1}{JC_b\omega}}{R_L + \frac{1}{JC_b\omega}} + R_b + R_B + JL_B\omega \tag{19}$$

$$Z_g = \frac{1}{JC_g\omega} \tag{20}$$

Therefore, the bearing current can be calculated as,

$$I_b = \frac{V_{sh}}{Z_b} \tag{21}$$

As a result, the leakage current can be calculated as,

$$I_c = \frac{V_{CM}}{Z_{sg}/3} + \frac{V_{sh}}{Z_g} + \frac{V_{sh}}{Z_b} \tag{22}$$

Where Zsg is the impedance between the stator winding and the ground which is given as,

$$Z_{sg} = R_{sg} + JC_{sg}\omega + \frac{1}{JC_{sg}\omega} \tag{23}$$

From equation (17) and (22), the following equation is obtained:

$$I_c = V_{cm} Z_T \tag{24}$$

where ZT is given as,

$$Z_T = \left[ \frac{\left[ Z_g Z_b \left( Z_{sr}/3 + Z_{rg} \right) + Z_{sg} Z_{rg} \left( Z_g + Z_b \right) \right]}{Z_{sg} Z_g Z_b \left( Z_{sr}/3 + Z_{rg} \right)} \right] \tag{25}$$

Equation (24) clearly shows that the smaller the CMV, the smaller the losses and higher the system efficiency.

## III. Common Mode Voltage (CMV) Control

A schematic of the three-phase, neutral point clamped inverter fed induction motor drive system is shown in Fig. 3. The basic principles of the pulse generation for 3-level PD and POD SPWM techniques are shown in Fig. 4(a) and Fig. 4(b). Fundamental frequency three-phase sinusoidal reference waves $V_a$, $V_b$ and $V_c$ are compared with two high frequency triangular carrier waves "Car1" and "Car2." Each intersection gives the control pulses for the switching devices of the inverter. These reference sinusoidal waves $V_{(a,b,c)}$ can be represented by,

$$\left.\begin{aligned} V_a &= V_m \sin(\omega t) \\ V_b &= V_m \sin(\omega t - 120^o) \\ V_c &= V_m \sin(\omega t - 240^o) \end{aligned}\right\} \tag{26}$$

The control pulses generated by a comparison of the reference voltage wave with "Car1" are given to the upper switches ($Q_{a1}$, $Q_{b1}$,$Q_{c1}$) of the inverter shown in Fig. 3. The corresponding complementary signals of these pulses are given to ($Q'_{a1}$, $Q'_{b1}$, $Q'_{c1}$). The control pulses generated by a comparison of the reference voltage wave with "Car2" are given to the switches ($Q_{a2}$, $Q_{b2}$,$Q_{c2}$). The corresponding complementary signals of these pulses are given to ($Q'_{a2}$, $Q'_{b2}$, $Q'_{c2}$).The modified SPWM based CMV control techniques and the effect of a phase shift between the carriers and the modulating wave are explained in following sections.

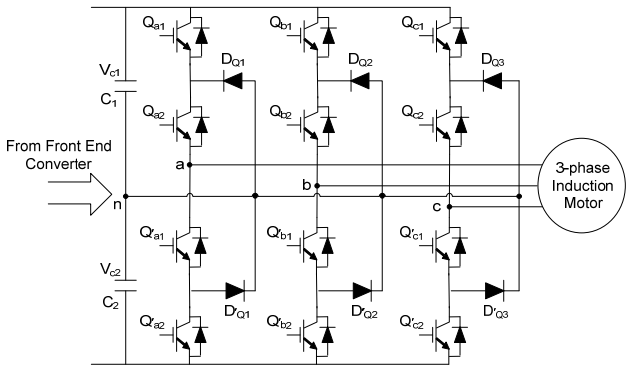



Fig. 3. Schematic of neutral point clamped inverter fed induction motor drive system.

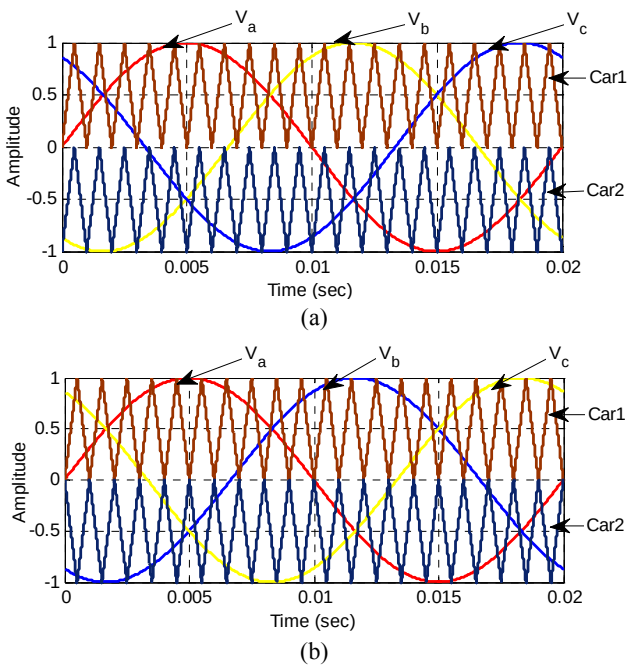



Fig. 4. (a)Generation of control pulses with PD SPWM technique.(b) Generation of control pulses with POD SPWM technique.

### *A. Modified SPWM Based CMV Control Technique*

The magnitude and rate of change of common mode voltage depend on the control pulse width, the number of commutations and its frequency, which can be modified by adding a variable offset voltage signal to the reference voltage wave [15]. The off-set voltage signal plays an important role in modifying the modulating or reference signal. This section presents the basic concept of calculating and adding the variable offset signal to the PD and POD SPWM techniques as shown in Fig. 5 (a) and Fig. 5 (b). Common mode voltage is essentially the zero sequence voltage in the output voltage of an inverter and can be

represented by,

$$V_{cm} = (V_a + V_b + V_c)/3 \quad (27)$$

Where $V_a$, $V_b$ and $V_c$ are the phase voltages of the inverter. The magnitude of common mode voltage is approximately equal to the DC link voltage in a conventional 2-level inverter and half of the DC link voltage in a 3-level inverter with the PD SPWM technique. To reduce CMV, a variable common mode offset voltage signal is added to the reference voltage signal which can be estimated as,

$$V_{off} = -\left[\min(V_a, V_b, V_c) + \max(V_a, V_b, V_c)\right]/2 \quad (28)$$

where min($V_a$, $V_b$, $V_c$) and max($V_a$, $V_b$, $V_c$) are the minimum and maximum functions of the reference voltage wave. A new reference or modulating wave can be derived by adding this common mode variable offset voltage signal to the original reference voltage wave as,

$$V^*(a,b,c) = V(a,b,c) + V_{off} \quad (29)$$

where V(a,b,c) is given by (26). Fig. 5 (a) and Fig. 5 (b) show the 3-phase reference waves as given in (29). The 'max', 'min', one phase voltage $V_a$, and off-set voltage signal, as given by (26) to (29), are shown in Fig. 6 for the PD SPWM technique. This common mode voltage off-set signal controls the CMV in the inverter output. The new 3-phase reference waves with the addition of an offset signal for the PD SPWM technique is given in Fig. 5 (a). The new 3-phase reference waves with the addition of an offset signal for the POD SPWM techniques is shown in Fig. 5 (b).

### *B. Effect of the Phase Shift between the Carriers and the Modulating Signal*

The phase shift angle between the modulation signal and the carrier signals plays an important role in multilevel inverters in terms of the number of switching ($N_{SW}$) within each fundamental cycle. The effect of this phase angle shift on $N_{SW}$ is being studied in this section for 3-level neutral point clamped inverter. The modulating signal, $V_a$ of a phase, can be represented by,

$$V_a^* = |V|\cos(\theta - \alpha) \quad (30)$$

Where, $|V|$ is the magnitude of the phase voltage, and α is the phase shift angle between the modulating signal and the carrier signal. In 2-level PWM inverters, with a single carrier signal, the number of switching $N_{SW}$ is 84 for a frequency modulation index of $m_f = 41$ regardless of the value of α and for all values of the amplitude modulation index $m_a < 1$. In this section, the reduction of $N_{SW}$ is studied by using the offset voltage signal addition technique as described in sub-section *A*. The techniques presented previously by different authors considered only two cases for study i.e. (i) when the carrier is at its maximum, and the modulating signal is at its minimum, and (ii) when the carrier is at its minimum, and the modulating signal is at its maximum. Other possibilities which are important for exploring the capabilities of the

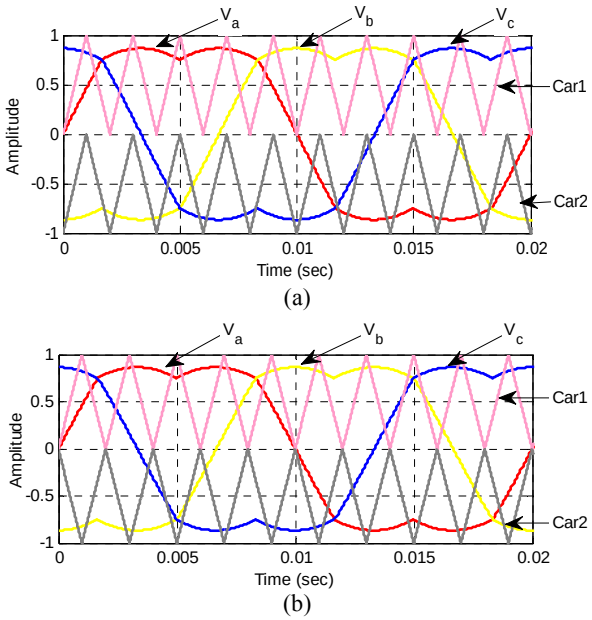



Fig. 5. (a) Generation of control pulses with addition of variable offset signal in PD SPWM technique.(b) Generation of control pulses with addition of variable offset signal in POD SPWM technique.

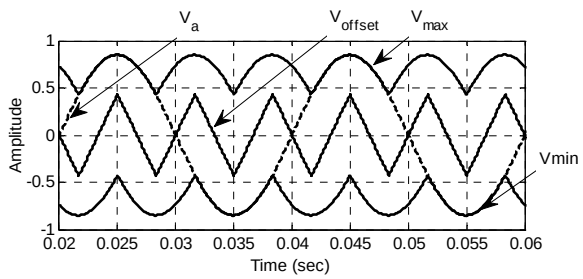



Fig. 6. Variable off-set voltage signal generation in PD SPWM technique.

offset signal addition technique have not been covered such as the effect of the phase shift between the carriers and the modulating wave. The value of α is now varied and the effect of this shift on the total number of switching of the active devices and the output voltage waveform distortion have been observed. Fig. 4 (a) and Fig. 4 (b) show the principle of the generation of pulses for a 3-level NPC with the conventional PD and POD SPWM techniques. The offset addition technique with $m_f = 41$, $m_a = 1$ is given in Fig. 5 (a) and Fig. 5 (b). It is clear that, in offset addition PWM technique, again of 15 % in output voltage is achieved before going into the over-modulation region.

Total number of switching, $N_{SW}$ (the active device transition from on-to-off or off-to-on), during a modulation period can vary from84 to 116 whenα is varied from 0° to 8°. Tables I and II show the total number of switching per modulating cycle with a varying α with $m_f = 41$, $m_a = 0.8$ with these techniques. It is clear that the number of switching decreases with the phase shift α in the offset addition PWM

TABLE I

NO. OF MAIN DEVICE SWITCHING PER MODULATING CYCLE FOR 3-LEVEL DCMLI WITH CONVENTIONAL SPWM TECHNIQUE (MF = 41, MA = 0.8)

| Carrier Phase Angle ($\alpha$) | No. of Switching per Cycle | | |
|---|---|---|---|
| | $Q_{a1}$, $Q_{a1}'$ | $Q_{a2}$, $Q_{a2}'$ | $N_{sw}$ |
| 0° | 42 | 42 | 84 |
| 2° | 46 | 46 | 92 |
| 4° | 50 | 50 | 100 |
| 6° | 54 | 54 | 108 |
| 8° | 58 | 58 | 116 |

TABLE II

NO. OF MAIN DEVICE SWITCHING PER MODULATING CYCLE FOR 3-LEVEL DCMLI WITH SFO-PWM TECHNIQUE (MF = 41, MA = 0.8)

| Carrier Phase Angle ($\alpha$) | No. of Switching per Cycle | | |
|---|---|---|---|
| | $Q_{a1}$, $Q_{a1}'$ | $Q_{a2}$, $Q_{a2}'$ | $N_{sw}$ |
| 0° | 52 | 52 | 104 |
| 2° | 48 | 48 | 96 |
| 4° | 44 | 44 | 88 |
| 6° | 40 | 40 | 80 |
| 8° | 36 | 36 | 72 |

technique. At a particular phase shift i.e. 8°, the number of switching is even lesser than that in the conventional SPWM technique.

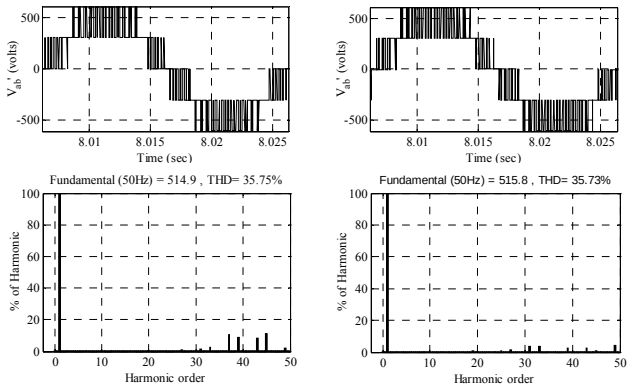
Fig. 7 shows the line voltages with the conventional PD SPWM and with the offset addition PD SPWM techniques. If the individual harmonic contents in the line voltages are investigated, it is determined that the lower order harmonics i.e. 39$^{th}$ and 43$^{th}$ have been drastically reduced in the offset addition PD SPWM when compared with the conventional PD SPWM technique. Therefore, the offset addition PD SPWM technique introduces the 3$^{rd}$ order harmonics in the phase voltage (eliminated from the line voltages), reduces the lower order harmonics from the line voltage and reduces the number of switching within each half of a cycle of inverter voltage, which reduces the switching losses.

## IV. SIMULATION RESULTS

A simulation study of the neutral point clamped inverter fed 3-phase squirrel cage induction motor has been carried out in MATLAB, and the simulation results are presented to validate the mathematical model presented for the CMV control. The simulation parameters for the common mode voltage control are given in Table III.

The CMV in a NPC inverter when compared to a 2-level inverter fed induction motor drive with $m_f = 41$ and $m_a = 0.8$ is considered in this section.

The inverter line voltage ($V_{ab}'$), the stator current drawn by the induction motor ($i_s$), and the speed of the machine ($N_r$) are shown in Fig. 8.




(a) (b)

Fig. 7. Line voltages with (a) conventional PD SPWM and (b) offset addition PD SPWM techniques.

TABLE III

SIMULATION PARAMETERS

| **DC Link Parameters** | | |
|---|---|---|
| DC Link Voltage | $V_{dc}$ | 620 V |
| DC Link Capacitance | $C_1$ and $C_2$ | 2200 µF |
| **Load Parameters** | | |
| Load type | 3-ϕ, Squirrel Cage Induction Motor | |
| Line Voltage | 400 V | |
| Speed | 1440 RPM | |
| Frequency | 50 Hz | |
| Rated Power | 5 H.P | |
| Power Factor | 0.84 | |

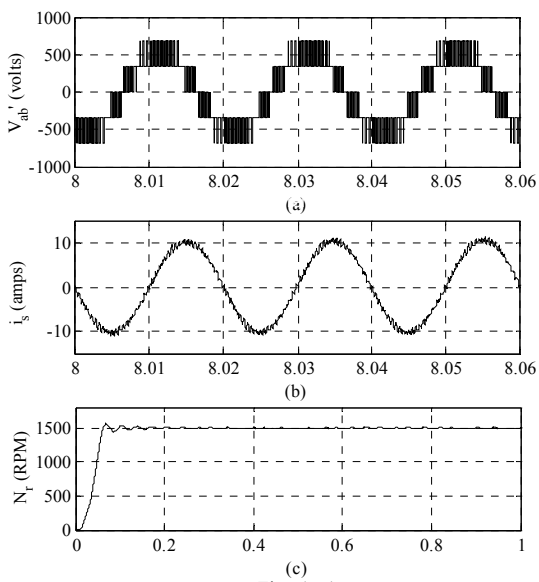



Fig. 8. (a) Inverter line voltage ($V_{ab}'$), (b) stator current ($i_s$), and (c) speed ($N_r$).

Fig. 9 shows the CMV at the inverter terminals when fed by a 2-level inverter. Fig. 10 presents the CMV with 3-level SPWM techniques such as PD, POD, PD with an offset

signal, and POD with an offset signal as discussed in Section II. It is observed that the magnitude of the CMV is considerably reduced in the NPC 3-level inverter fed induction motor drive when compared with the2-level inverter fed induction motor drive. This is another important feature of the multilevel structure for high power drives applications.

Fig. 11(a) shows the line voltages for the PD and the PD with off-set signal addition techniques. It is observed from these figures that the overall % THD remains almost same. However, it can also be seen that the low order harmonics are reduced considerably when an off-set signal is added to the modulating signal. The % THD in the line voltages is high for the PD and the PD with off-set signal addition techniques. The issue of the higher %THD in the line voltages can be easily handled by incorporating a well-designed LC filter as shown in Fig. 11(b).Fig. 11(b) clearly shows that the % THD is well below the limit of IEEE 519 in both cases.

The line voltage $V_{ab}^{'}$ for the POD and the POD with addition of an off-set signal to the modulating wave without a filter is shown in Fig. 12(a). This clearly shows that the harmonic profile is deteriorated in the POD with an off-set signal with increased harmonics contents around the carrier frequency. Fig. 12(b) shows improved line voltage profiles when a filter is included.

Table IV gives a comparison of these techniques in terms of the rate of change of the CMV (p.u) with its corresponding number of commutations, the magnitude of the CMV and the %THD in the line voltage. The rate of change of the CMV of higher magnitude will obviously have more adverse effects on the motor windings and bearings (equation 24). It can be clearly observed from Table IV that rate of change of the CMV of higher magnitude has been reduced when an off-set is added to the PD modulating technique. Meanwhile, when an off-set signal is added to the POD modulating technique the rate of the change of the CMV of higher magnitude becomes zero. Therefore, the POD with the addition off-set signal technique gives better CMV performance for a 3-levelinverter fed induction motor drive but at the cost of an increased %THD in the line voltage which can be easily mitigated with a properly designed LC filter. On the other hand, the PD SPWM with the off-set signal technique gives better line voltage harmonic performance (reduced lower order harmonic) with sharp edges in the CMV when compared to the PD SPWM.

The performance of the system has also been evaluated for different modulation schemes both with and without an offset signal by considering the linear range of the modulation index. The variation of the rms value of the CMV with the modulation index is shown in Fig. 13 with and without an offset signal. It has been observed that the POD with an offset provides a lower rms value of the CMV for the linear

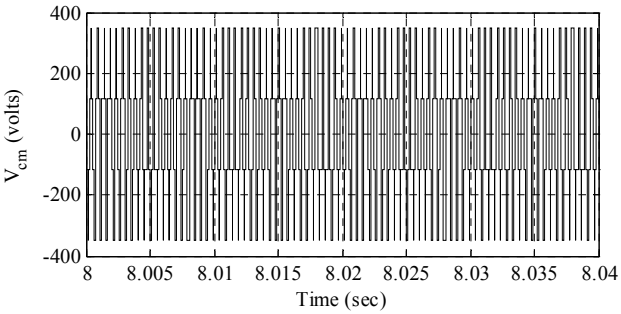



Fig. 9. Common mode voltage with 2-level inverter.

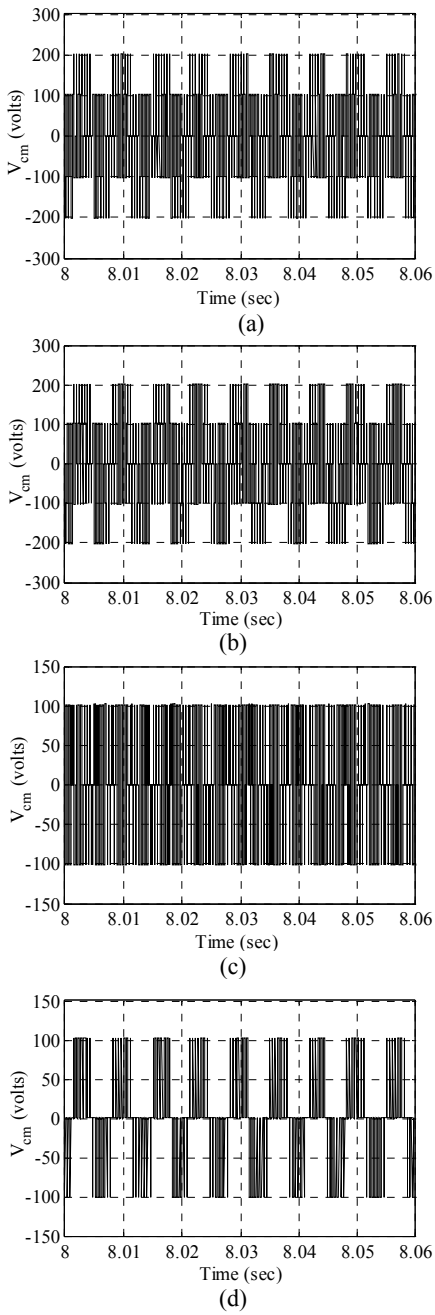



Fig. 10. Common mode voltage with: (a) PD, (b) PD with off-set signal, (c) POD, and (d) POD with off-set signal.

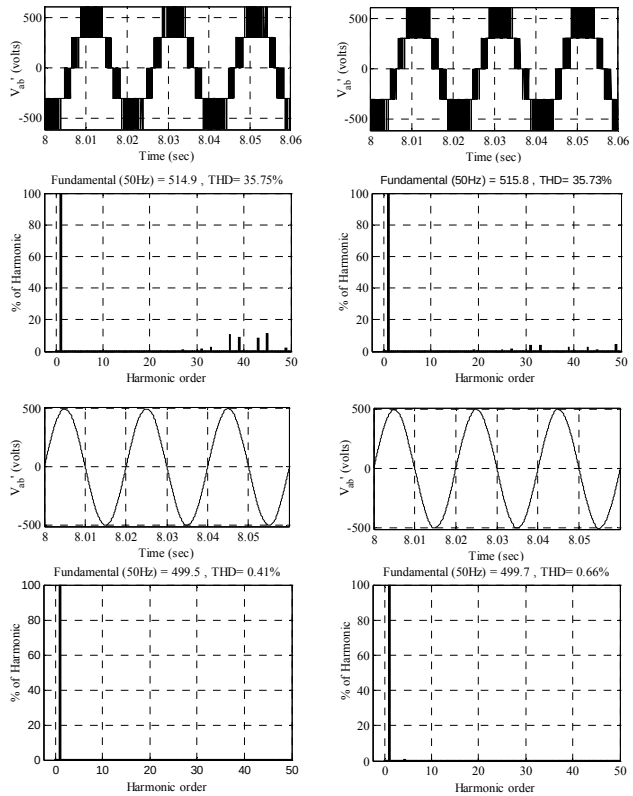



Fig. 11. Line voltage without filter ($V_{ab}$') with (a) PD and (b) PD with off-set signal.

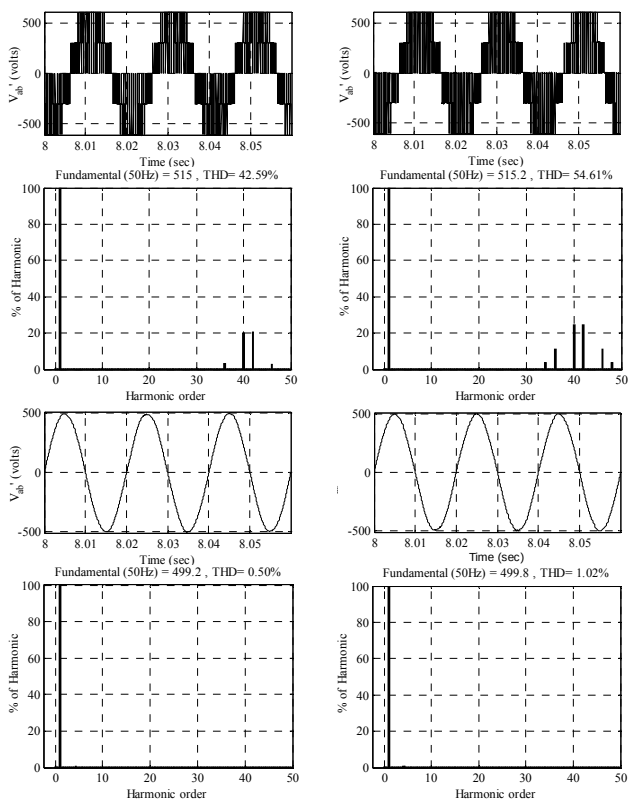



Fig. 12. Line voltage without filter ($V_{ab}$') with (a) POD and (b) POD with off-set signal.

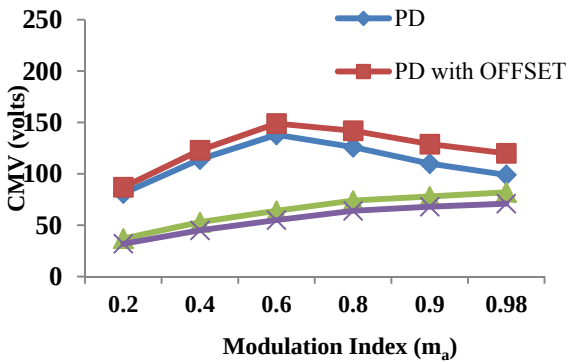



Fig. 13. Variation of CMV for PD, POD with and without offset considering different values of modulation index.

range of the modulation index as when compared to the conventional modulation schemes i.e. PD and POD.

The efficiency of the system decides the relevance of the proposed method used for improved performance.

Therefore, the efficiency has been evaluated for different modulation schemes with and without an offset signal by considering the practical data of the IGBTs ($R_{on}$=0.1 ohms) used for experimentation. The effectiveness of the POD with an offset is also observed in terms of the efficiency of the drive system as shown in Fig. 14.

## V. EXPERIMENTAL RESULTS

A laboratory prototype has been developed to verify and investigate the control of common mode voltage using the different modulation techniques explain in Section III. The prototype of a NPC 3-level inverter based AC-DC-AC drive system includes twelve STGW30N120KD IGBTs, of 1200 volts, 30 amps rating and six fast recovery diodes (16FM120) with two dc link capacitors of 2200mF, 600 V each at dc link side. The DC supply is obtained through a three-phase, six-pulse uncontrolled diode bridge rectifier. The control algorithm is implemented through the dSPACE real time interface DS1103. The DS1103 real time hardware implementation board is based upon a Texas Instruments TMS320F240, 16 bit fixed point, 250 MHz CPU, 20 MHz clock frequency digital signal processor. Fig. 15 shows the prototype developed in laboratory for experimentation. The parameters used for experiment are given in Table V for the 3-phase squirrel cage induction motor.

The common mode voltages with the PD, POD, PD with an off-set signal, and POD with an off-set signal techniques are shown in Fig. 16. These experimental results are in agreement with the corresponding simulation results for the effective control of common mode voltage.

The frequency spectrums of the line voltage $V_{ab}$ with these 3-level SPWM techniques are shown in Fig. 17. The lowest THD contents are obtained with the PD SPWM technique with an off-set signal i.e. 10.1%. The line voltages contain

TABLE IV
COMPARISON OF RATE OF CHANGE OF CMV AND ITS CORRESPONDING NUMBER OF COMMUTATION FOR DIFFERENT 3-LEVEL SPWM TECHNIQUES

| Modulating Techniques | Rate of change of CMV (in p.u) and its corresponding number of commutation in one cycle | | | | RMS Value of CMV (Volts) | Line Voltage THD Without Filter (%) | Line Voltage THD With Filter (%) |
|---|---|---|---|---|---|---|---|
| | $\lim_{\Delta t \to 0} \frac{(1/2)}{\Delta t}$ p.u | Corresponding number of commutations | $\lim_{\Delta t \to 0} \frac{(1)}{\Delta t}$ p.u | Corresponding number of commutations | | | |
| PD | 80 | 120 | 68 | 104 | 110 | 35.75 | 0.41 |
| PD with Off-set | 42 | 126 | 40 | 96 | 118 | 35.73 | 0.66 |
| POD | 120 | 360 | 40 | 60 | 78 | 42.59 | 0.5 |
| POD with Off-set | **40** | **120** | **0** | **0** | **68** | **54.61** | **1.02** |

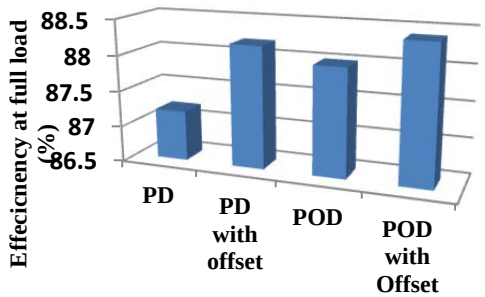



Fig. 14. Efficiency (%) at full load for PD, POD with and without offset considering the filter.

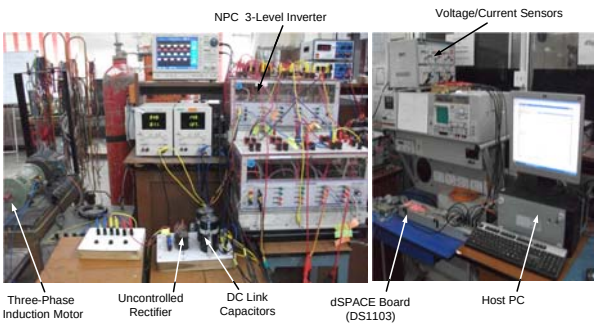
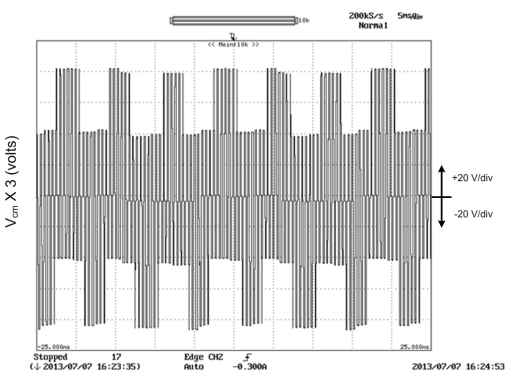
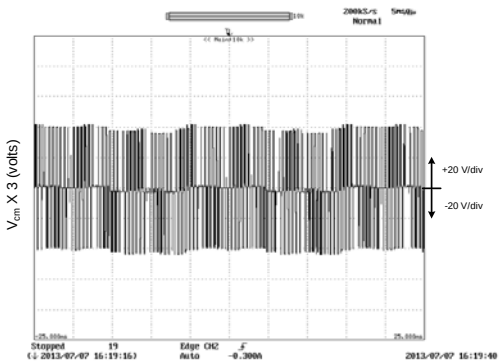


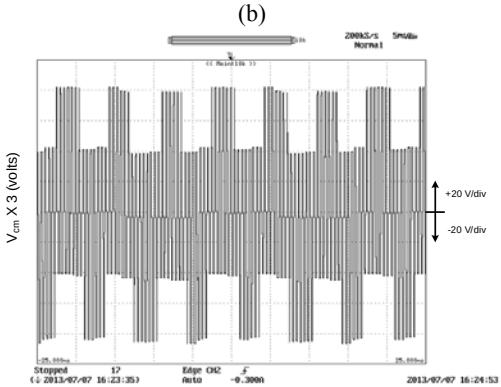

Fig. 15. Laboratory prototype of AC-DC-AC induction motor drive system.



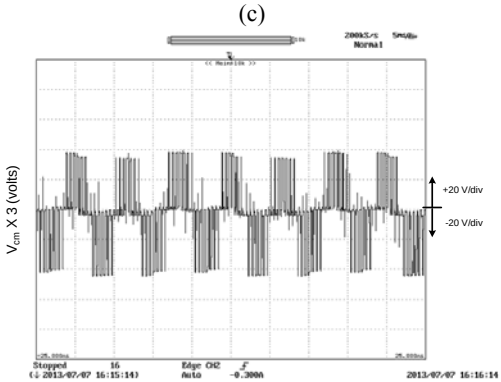

(a)




(b)




(c)




(d)

Fig. 16. Common mode voltage with: (a) PD, (b) PD with offset signal, (c) POD, and (d) POD with offset signal.

TABLE V
EXPERIMENTAL PARAMETERS

| | | |
|---|---|---|
| Line Voltage (RMS) | $V_{LL}$ | 60 V |
| Source Inductor | $L_s$ | 7.73mH |
| AC Link Resistance | R | 0.4 Ω |
| DC Link Voltage | $V_{dc}$ | 80 V |
| DC Link Capacitance | $C_1$ and $C_2$ | 2200 µF |
| Line Voltage | 415 V | |
| Frequency | 50 Hz | |
| Speed | 1440 RPM | |
| Rated Power | 1.5 kW | |
| Power Factor | 0.84 | |
| Carrier Frequency | 2050 Hz | |

(x-axis: time- 5ms/div, y-axis: $V_{cm}$ -20 V/div)

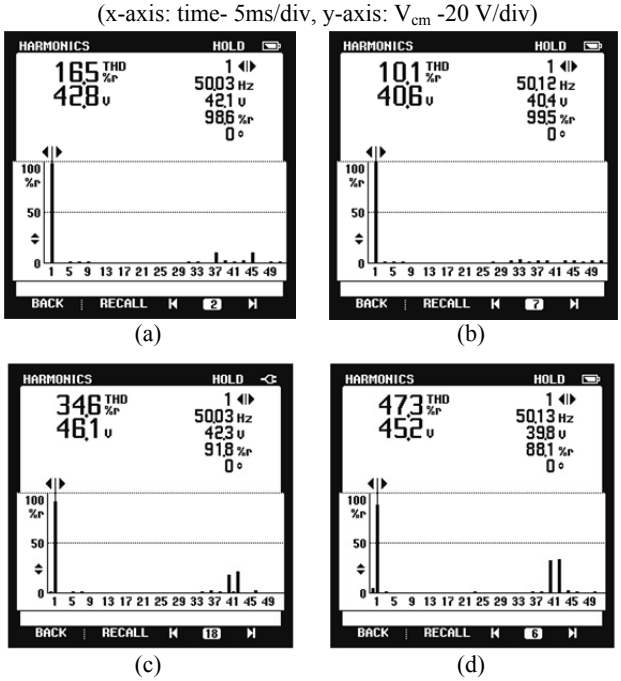



Fig. 17. Harmonic spectrums of Line voltages ($V_{ab}$) with: (a) PD, (b) PD with off-set signal, (c) POD, and (d) POD with off-set signal.

increased magnitude of the harmonics around the switching frequency and the THD contents are 34.6% and 47.3% in the POD SPWM and the POD SPWM with an off-set signal, respectively. The comparison of these techniques, as given in Table IV, is also verified experimentally.

## VI. CONCLUSION

This paper explored the opportunities of common mode voltage (CMV) control using simple SPWM techniques for a 3-level diode-clamped inverter. The CMV at the inverter terminal has been obtained with the 3-level PD SPWM and the 3-level POD SPWM techniques and compared that obtained with a 2-level inverter. Further, a method for the reduction of CMV based on the SPWM technique has been derived based on the addition of a variable CMV offset signal to the original modulating wave. This method can also be applied for a higher number of levels with better performance.

The main contribution of this paper, when compared to [15], is the experimental development of the offset signal addition technique in the SPWM based control of a 3-level inverter for CMV control. The effect of the phase shift between the carriers and the modulating wave on the CMV and the number of commutations per cycle is also investigated. Simulation results show the effectiveness of the CMV control techniques, giving improved performance with a reduction of the magnitude and the number of commutations per cycle in the CMV.

The important conclusion from the obtained results is that the POD SPWM technique with an offset addition gives better CMV performance. It increases the THD in the output line voltage of the inverter. However, the lowest dominant harmonics decreased significantly. The improvement in the efficiency also confirms the results given in Table IV, for a system that has a lower rate of change of the CMV (p.u) with a corresponding number of commutations and a low magnitude of the CMV.

The investigations made in this paper give an idea for the selection of an appropriate modulation technique to control the CMV in AC-DC-AC drive systems for improving the duty life of the bearings of induction motors for critical high performance applications. Further, a technique for SPWM based CMV elimination may be derived. Experimental validation has been obtained and found comparable to simulated results.

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**Amit Ojha** was born in India, in 1974. He received B.E degree in Electrical Engineering from MACT, Bhopal, India, in 1998. He received M. Tech. and Ph. D. degrees from Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2002 and 2013, respectively. He studied multilevel converter fed induction motor drives while working towards his Ph. D.. He has had more than 14 years of teaching experience and more than 5 years of research experience. He is presently working as an Assistant Professor in Department of Electrical Engineering, MANIT. His current research interests include electrical machines, power electronics, electric drives, high-power-factor converters, and multilevel converters.

**Pradyumn Chaturvedi** received B.E. degree in Electrical Engineering from Barkatullah University, Bhopal, India, in 1996; M.E. degree in Power Electronics from the Rajiv Gandhi Technical University, Bhopal, India, in 2001; and Ph.D. degree from the National Institute of Technology, Bhopal, India, in 2010. He has had 14 years of teaching experience. He is presently working as an Assistant Professor in the Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, India. He has published more than 45 research papers in referenced national and international journals and conferences. His current research interests include electrical drives, high-power-factor converters, photovoltaic power conditioning systems, and multilevel inverters.

**Arvind Mittal** obtained B.E. degree in Electrical Engineering from Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 1991, securing first position in the university (Gold Medallist). He is a post graduated in Power Apparatus and Electrical Drives (PAED) at the Indian Institute of Technology Roorkee, Roorkee, India, in1993, and obtained Ph.D. degree from Barkatullah University, Bhopal India, in 2002. He is presently an Associate Professor in the Energy Centre, MANIT, Bhopal, India. He has had more than 23 years of experience in teaching undergraduate and postgraduate students. He is a life member of the ISTE and an Associate Member of the Institution of Engineers. He has guided two Ph.D. candidates and published several papers in various national and international conferences and journals. He has also authored seven engineering books.

**Shailendra Jain** received B. E. degree in Electrical Engineering from Samrat Ashok Technological Institute (SATI), Vidisha, India, in 1990; M.E. degree in Power Electronics from the Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 1994; Ph.D. degree from the Indian Institute of Technology, Roorkee, India, in 2003; and Post-Doctoral Fellowship from the University of Western Ontario, London, ON, Canada, in 2007. He is presently a Professor in the Department of Electrical Engineering, National Institute of Technology, Bhopal, India. His current research interests include power electronics and electric drives, power quality improvement, active power filters, high-power-factor converters, and fuel-cell-based distributed generation. Dr. Jain was a recipient of the "Career Award for Young Teachers" from the All India Council for Technical Education (AICTE), New Delhi, India, for the year 2003–2004.