



# Investigation of Endurance Degradation in a CTF NOR Array Using Charge Pumping Methods

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Received October 2, 2015; Revised November 23, 2015; Accepted November 23, 2015

We investigate the effect of interface states on the endurance of a charge trap flash (CTF) NOR array using charge pumping methods. The endurance test was completed from one cell selected randomly from 128 bit cells, where the memory window value after  $10^2$  program/erase (P/E) cycles decreased slightly from 2.2 V to 1.7 V. However, the memory window closure abruptly accelerated after  $10^3$  P/E cycles or more (i.e. 0.97 V or 0.7 V) due to a degraded programming speed. On the other hand, the interface trap density (Nit) gradually increased from  $3.13 \times 10^{11} \text{ cm}^{-2}$  for the initial state to  $4 \times 10^{12} \text{ cm}^{-2}$  for  $10^2$  P/E cycles. Over  $10^3$  P/E cycles, the Nit increased dramatically from  $5.51 \times 10^{12} \text{ cm}^{-2}$  for  $10^3$  P/E cycles to  $5.79 \times 10^{12} \text{ cm}^{-2}$  for  $10^4$  P/E cycles due to tunnel oxide damages. These results show good correlation between the interface traps and endurance degradation of CTF devices in actual flash cell arrays.

**Keywords:** Charge-trap flash (CTF), SONOS, NOR array, Charge pumping method

## 1. INTRODUCTION

In the past decade, embedded NOR-type flash memories used for code storage and execution have become a key electronic device in mobile applications [1]. The mainstream market is currently dominated by the floating gate (FG) technology in NOR-type flash. Yet, the scale down of FG memory device is placed in an extremely dire situation due to the physical limits of gate length and tunneling oxide thickness [2]. In order to replace traditional FG devices, a polysilicon-oxide-nitride-oxide-silicon (SONOS) structure is being developed for commercial applications [3-10]. In general, the NOR-type SONOS flash memories are selectively programmed by the channel hot electron injection (CHEI) near the drain junction and erased by Fowler-Nordheim (F-N) tunneling or hot hole injection (HHI) [11-13]. These

methods generate the so-called tunnel oxide damage, including interface states, which causes serious reliability problems such as programming time delay, memory window closure, or gate/drain disturb. Therefore, monitoring the degradation of interface states between the tunnel oxide and a Si substrate during program/erase (P/E) cycling for both selected and unselected cells in a real array structure is important. Transistors in the array tend to generate more interface traps as pulse cycles are being proceeded due to their larger active edge portion than transistors in the unit cell [14]. However, this area is largely unexplored and requires careful analysis. In this paper, we evaluate the reliability degradation during program/erase (P/E) cycles in a SONOS NOR array with common source lines (CSL) using a charge pumping technique.

## 2. EXPERIMENTS

The NOR-type SONOS memory devices used in this study were fabricated using a standard  $0.35 \mu\text{m}$  complementary-metal-oxide-semiconductor (CMOS) technology. In these devices, the

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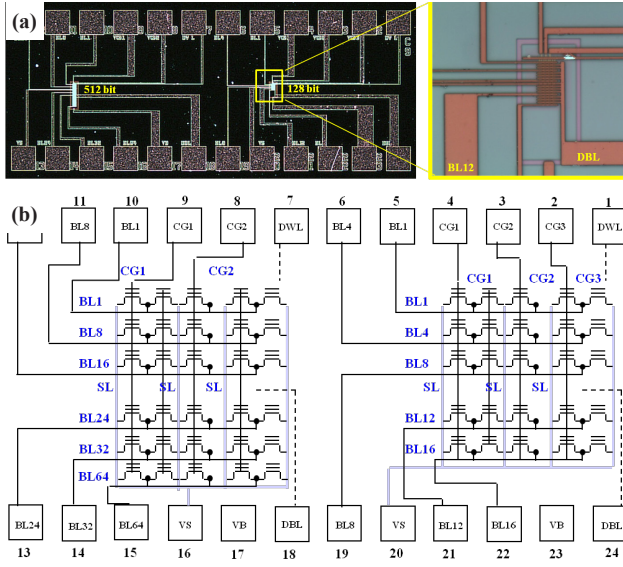


Fig. 1. (a) Optical microscope images of test patterns for NOR-type array with common source lines and (b) its corresponding array architecture.

channel length and width were  $0.5 \mu\text{m}$  and  $0.5 \mu\text{m}$ , respectively, and the ONO layer thicknesses observed by transmission electron microscopy (TEM) were  $3.4 \text{ nm}/7.3 \text{ nm}/3.4 \text{ nm}$ . The bottom oxide layer was thermally grown at  $900^\circ\text{C}$  in nitrogen diluted with oxygen. To make the ONO stack, the nitride was first deposited using low-pressure chemical-vapor deposition (LPCVD) at a low chamber pressure of  $0.5 \text{ Torr}$  at  $770^\circ\text{C}$  by reacting dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) with ammonia ( $\text{NH}_3$ ) =  $30 : 330 \text{ sccm}$ . The blocking oxide was then grown by thermal oxidation at  $950^\circ\text{C}$  with a gas flow ratio of hydrogen ( $\text{H}_2$ ) : oxygen ( $\text{O}_2$ ) =  $5 : 10 \text{ l/min}$ . Sequentially, the n-type impurity was ion implanted to form n+ diffusion layers after the field oxide was etched by self-align source (SAS). Diffusion layers of the n+ type were used for the common source line, and the salicide process was implemented to reduce the resistance of n+ diffusion layers. For all of these SONOS cells, the drains were electrically connected to the bit line (BL) while the gates and the sources were connected to the word line (WL) crossing the BL and the common source line (CSL) for every 128 memory cells

### 3. RESULTS AND DISCUSSION

Figure 2(a) shows the drain current-gate voltage ( $I_D$ - $V_G$ ) and transconductance curves as a function of drain voltages for the one cell selected within a 128 bit cell array. The transfer characteristics of the selected cell were measured at a drain voltage of  $100 \text{ mV}$  by sweeping the gate voltage from  $0 \text{ V}$  to  $7 \text{ V}$ . The threshold voltage ( $V_{\text{TH}}$ ) was measured to be  $3 \text{ V}$ . The selected cell showed a high ON/OFF current ratio ( $I_{\text{ON}}/I_{\text{OFF}}$ ) exceeding  $10^6$ . The linear transconductance ( $G_m$ ) was  $8.87 \times 10^{-6} \text{ S}$  at a turn-on voltage. The subthreshold swing (SS) was  $198 \text{ mV/decade}$ , which may be an acceptable value considering the ideal value of  $60 \text{ mV/decade}$ . Figure 2(b) shows the drain current-drain voltage ( $I_D$ - $V_D$ ) curves as a function of gate voltages applied from  $2 \text{ V}$  to  $7 \text{ V}$  with  $0.5 \text{ V}$  steps. This shows a good n-channel field effect transistor characteristic with typical saturation effects at high drain voltages.

In order to demonstrate the memory effect for the one cell selected within a 128 bit cell array, the (P/E) characteristics using

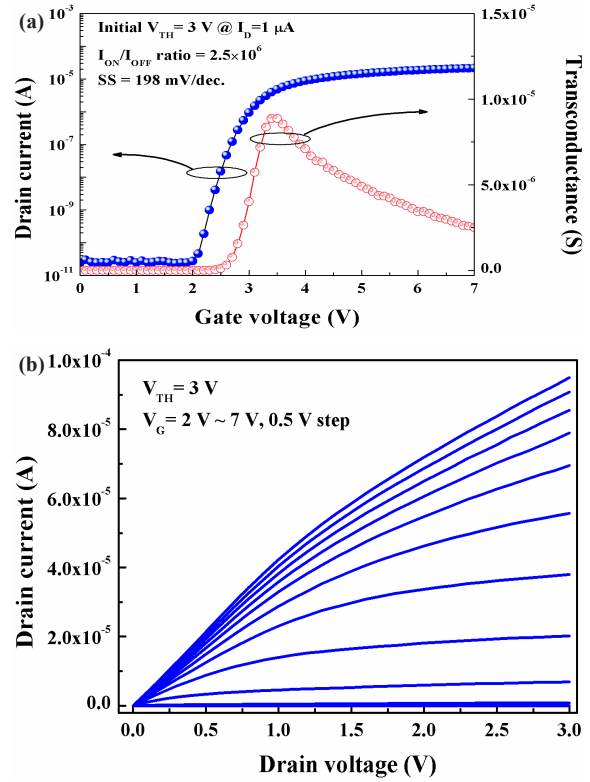


Fig. 2. (a)  $I_D$ - $V_G$  transfer and  $G_m$ , and (b)  $I_D$ - $V_D$  output characteristics measured for the one cell selected within a 128 bit cell array.

CHEI and HHI methods are shown in Fig. 3. First, the  $V_{\text{TH}}$  shifts are plotted against the program time at different drain and gate voltages after the  $V_{\text{TH}}$  of the selected cell was erased at  $2.8 \text{ V}$ , as shown in Fig. 3(a). As the program voltage and time increased, the  $V_{\text{TH}}$  increased. A  $V_{\text{TH}}$  shift of  $2 \text{ V}$ , which is large enough for program operation, was observed for the  $5 \text{ V}$  gate and  $5 \text{ V}$  drain bias conditions at a program time of  $5 \text{ ms}$ . Second, the erase characteristics are shown in Figure 3(b). The  $V_{\text{TH}}$  shifts were plotted against the erase time for various drain and gate voltages ranging from  $7 \text{ V}$  to  $7.6 \text{ V}$  with  $0.3 \text{ V}$  steps and from  $-5 \text{ V}$  to  $-7 \text{ V}$  with  $1 \text{ V}$  steps, after the cell were programmed at a  $V_{\text{TH}}$  of  $5.1 \text{ V}$ . The  $V_{\text{TH}}$  shifts in each programmed state decreased, due to the recombination of the charges injected from the substrate channel to the  $\text{Si}_3\text{N}_4$  layer through drain edges. The erasing speed increases with increasing drain or gate voltage. From these results,  $7.6 \text{ V}$  drain and  $-6 \text{ V}$  gate voltages are determined to be the most suitable erase condition at an erase time of  $10 \mu\text{s}$ .

Based on the P/E conditions in Fig. 3, we investigated the endurance characteristics, as shown in Fig. 4.

By increasing the cycling number, the initial memory window of  $2.2 \text{ V}$  gradually decreased to  $1.7 \text{ V}$ , however, after  $10^3$  P/E cycles, the sensing margin between program and erase states abruptly decreased. This endurance degradation is attributed to the interface-trap generation and the electron trapping in the tunneling oxide [15,16].

In order to verify the endurance degradation, a charge pumping method was employed [17,18]. Here, the charge pumping current ( $I_{\text{cp}}$ ) measurements were carried out as follows: A square pulse was applied to the gate of the selected SONOS cell while the source and substrate were grounded. A current meter (Keithley 4200) was used to measure the  $I_{\text{cp}}$  from the drain electrode. The gate pulse had a frequency of  $1 \text{ MHz}$ , a  $50\%$  duty cycle, rise/fall times of  $10 \text{ ns}$  and an amplitude voltage ( $V_g$ ) of  $5 \text{ V}$ .

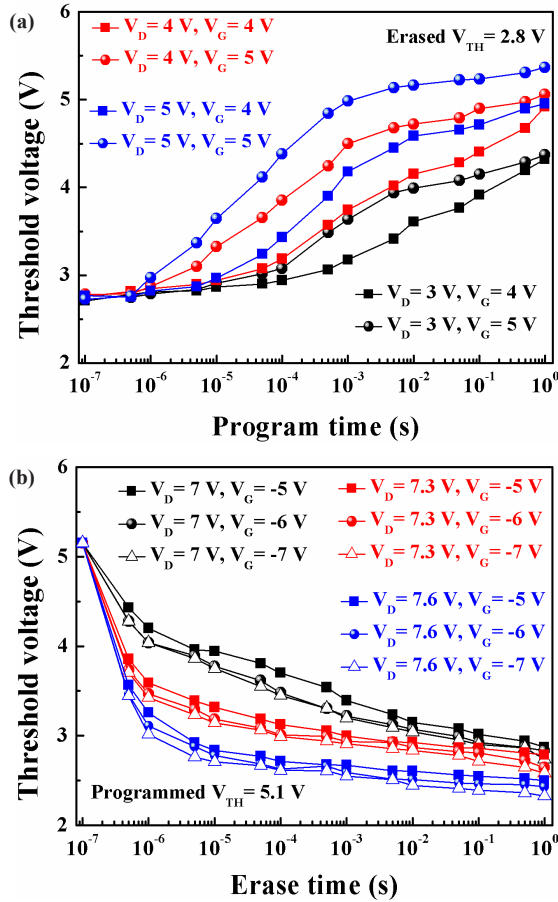


Fig. 3. (a) Program and (b) erase characteristics measured for the one cell selected within a 128 bit cell array.

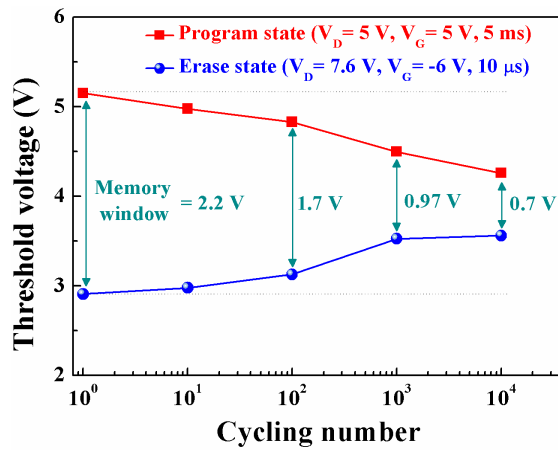


Fig. 4. Endurance characteristics measured for the one cell selected within a 128 bit cell array.

Figure 5(a) shows the charge pumping current ( $I_{cp}$ ) characteristics for the fresh and different numbers of P/E cycles at the erased state. The  $I_{cp}$  curves are plotted by the base level pulse height ( $V_b$ ) from -4 V to 3 V as a function of the fresh and cycling numbers. By increasing the number of cycles to 10<sup>2</sup>, the maximum  $I_{cp}$  gradually increased due to the interface-trap generation. After 10<sup>3</sup> P/E cycles, the maximum  $I_{cp}$  rapidly increased. The interface trap density (Nit) extracted from the  $I_{cp}$  curves versus

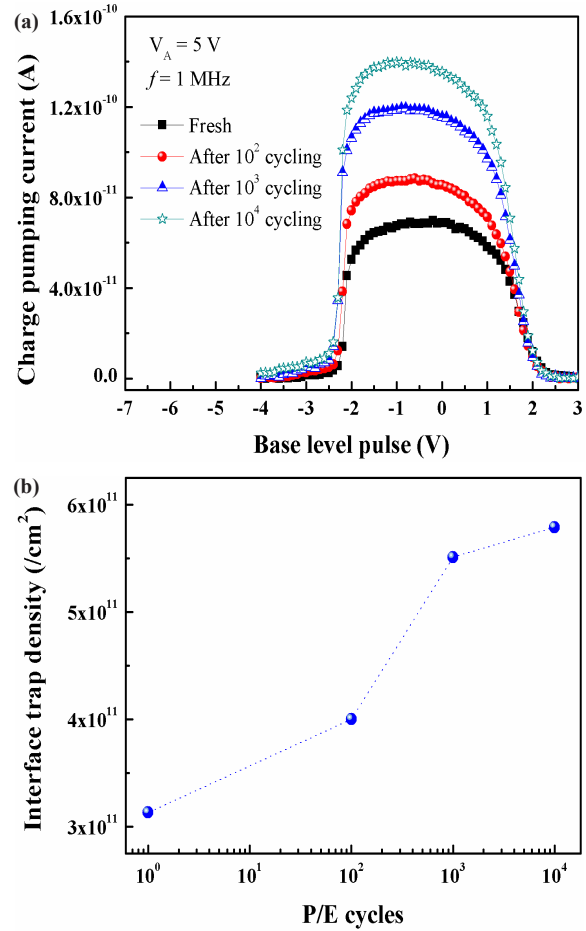


Fig. 5. (a)  $I_{cp}$  curves and (b) Nit extracted from  $I_{cp}$  curves versus P/E cycle numbers obtained for the one cell selected within a 128 bit cell array.

P/E cycle numbers is shown in Fig. 5(b). Compared to the Nit of initial state, the extracted Nit values of 10<sup>2</sup> cycled state slightly increased from 3.13x10<sup>11</sup> cm<sup>-2</sup> (initial state) to 4x10<sup>11</sup> cm<sup>-2</sup>. Remarkably, the Nit values from 10<sup>3</sup> to 10<sup>4</sup> cycling steeply increased from 5.51x10<sup>11</sup> cm<sup>-2</sup> to 5.79x10<sup>11</sup> cm<sup>-2</sup>, as compared to the Nit for 10<sup>2</sup> cycling. The steep increase of the Nit for 10<sup>3</sup> P/E cycles are consistent with the abrupt endurance degradation for 10<sup>3</sup> P/E cycles. Consequently, the relationship was determined between the endurance degradation and interface traps using charge pumping methods in actual flash cell array. The endurance properties of 10<sup>4</sup> cycles may not be enough for memory operation, but could be improved if we used thicker tunnel oxide layer or SiN-layer optimization, as indicated in previous work [19,20].

#### 4. CONCLUSIONS

The relation between the interface traps and the endurance degradation in SONOS devices has been successfully investigated using charge pumping methods, from the one cell selected within a 128 bit cell array. After 10<sup>3</sup> P/E cycles and above, the memory window abruptly reduced from 2.2 V for initial state to 0.7 V for 10<sup>4</sup> P/E cycles as well as extracted Nit was steeply increased from 3.13x10<sup>11</sup> cm<sup>-2</sup> for initial state to 5.79x10<sup>11</sup> cm<sup>-2</sup> for 10<sup>4</sup> P/E cycles due to tunnel oxide damage. We conclude P/E-cycling-induced trap generation leads to memory window closure and eventual device degradation is strongly dependent on Nit.

## ACKNOWLEDGMENT

This work was supported by Gyeongnam National University of Science and Technology Grant 2015.

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