Low-Power Fully Digital Voltage Sensor using 32-nm FinFETs

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Abstract: In this paper, a design for a fully digital voltage sensor using a 32-nm fin-type field-effect transistor (FinFET) is presented. A new characteristic of the double gate p-type FinFET (p-FinFET) is examined and proven appropriate for sensing voltage variations. On the basis of this characteristic, a novel technique for designing low-power voltage-to-time converters is presented. Then, we develop a digital voltage sensor with a voltage range of 0.7 to 1.1V at a 50-mV resolution. The performance of the proposed sensor is evaluated under a range of voltages and process variations using Simulation Program with Integrated Circuit Emphasis (SPICE) simulations, and the sensor is proven capable of operating under ultra-low power consumption, high linearity, and fairly–frequency conditions (i.e., 100 MHz).

Keywords: FinFET, Voltage sensor, Voltage-to-time converter, ADC, Voltage variation, Low power

1. Introduction

The scaling of metal-oxide semiconductor field effect transistor (MOSFET) devices has delivered astounding improvements in transistor density and performance, leading to greater functionality at higher speeds for single chips. However, as chip sizes continue to shrink, leakage and short channel effects reduce the reliability of silicon-based transistors [1]. To solve this problem, fin-type field-effect transistors (FinFETs) have emerged as a promising substitute for bulk complementary metal-oxide semiconductor (CMOS) transistors in the 22-nm node and beyond. The additional back gate in the FinFET provides circuit designers with many new options and ample design space. The two gates of the FinFET can be either shorted for higher performance or independently controlled for lower leakage or a reduced transistor count [2].

Increasing the chip density and more-aggressive scaling affects the chip response to parameters, such as process corners, voltage, and temperature. Thus, a more accurate understanding of these parameters can provide circuit designers with insight into how to improve chip behavior. Moreover, as the supply voltages are scaled below 1 V and the voltage variation becomes a major source of uncertainty [3], accurate monitoring of voltage fluctuation becomes increasingly important.

Numerous designs have been proposed for fully digital voltage sensors and analog-to-digital converters (ADCs) because they are widely preferred to achieve noise immunity [4-7]. However, to the best of our knowledge, a FinFET-based digital voltage sensor has yet to be developed. In this study, the unique characteristics of FinFET devices are examined to develop a novel design for a FinFET-based digital voltage sensor. By exploiting the ability to independently control the two gates of a p-type FinFET (p-FinFET) in low-power mode, a voltage-to-time mechanism that effectively controls the propagation delay of clock input is presented. Simulation results show that the proposed voltage sensor can operate properly at ultra-low power with high linearity, a wide voltage range, and a fairly high conversion rate.

This manuscript is an expanded version of work by Nguyen and Kim [15]. The major additions to that work are: (1) more in-depth and accurate double-gate FinFET controllable delay element (CDE) investigation, (2) voltage and process variation analysis, and (3) power consump-tion–related analysis and comparisons with other
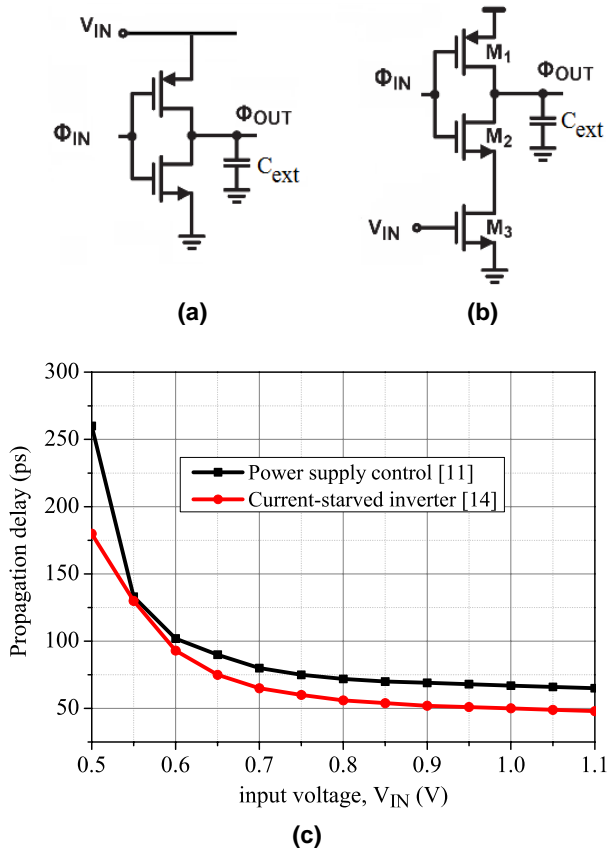
Fig. 1. Conventional controllable delay elements. (a) CDE in Watanabe et al. [6] and (b) in Taillefer and Roberts [7]. (c) Delay versus input voltage, V_{IN}.

designs. Most of Section 4 presents these additions.

The remainder of this paper is organized as follows. In Section 2, the existing research is discussed, and the characteristics of p-FinFETs are introduced. On the basis of the newly observed p-FinFET characteristics, a controllable delay element is proposed. In Section 3, the complete voltage sensor structure is shown. The design is evaluated using SPICE simulation, and results for voltage, process variation, and power consumption are presented in Section 4. The conclusion is presented in Section 5.

2. Controllable Delay Elements

2.1 Related Works

The digital voltage sensor consists of an ADC with fully digital blocks. One of the major challenges in developing digital voltage sensors is to design highly sensitive CDEs. Watanabe et al. [6] proposed an all-digital ADC in which the CDE architecture is based on the CMOS square-law behavior. Furthermore, the transistor drain current depends considerably on the supply voltage, and thus, the charging and discharging currents on the external capacitor inserted at the inverter output can be managed by controlling the supply voltage. As a result, the inverter delay can be effectively controlled, as seen in Fig. 1(a). The current-starved technique [7] is used to design a

CDE by adding a tail n-channel MOSFET (NMOS), M_3, below the conventional inverter to control the current discharge through M_2, as seen in Fig. 1(b).

Fig. 1(c) shows the characteristic of the CDEs prepared in previous works [6, 7] using a 32-nm CMOS predictive technology model (PTM) [13] supplied with 0.9-V VDD with a 10 fF capacitor. This figure shows that the delay can be well-controlled using either a power supply–control method or a current-starved inverter technique when input voltage (V_{IN}) ranges from 0.5 to 0.8 V. However, the delay controllability will be reduced significantly if V_{IN} fluctuates within the 0.1 V range around the supply voltage (i.e., 0.8 to 1.0 V). As a result, these techniques are not suitable for voltage sensor applications in which V_{IN} usually fluctuates by ±10% around the VDD. Watanabe et al. noted that the fluctuating voltage range used in the ADC is around 1.8 to 2.0 V [6], whereas VDD is 5 V; the input range is also much smaller than VDD = 2V in Taillefer and Roberts [7].

On the basis of these observations from the previous research, we can conclude that the conventional CDE design methodologies are not appropriate for digital voltage sensors at a lower VDD. Additionally, further scaling of the CMOS suffers from the inherent constraints of short channel effects. To overcome these barriers, tri-gate FinFETs with separate gate controllability and reduced leakage are a promising substitute for CMOS devices. Accordingly, this paper describes a method of using FinFET devices in the design of a fully digital voltage sensor.

2.2 P-type FinFET Characteristics

In general, FinFET devices (n-FinFETs and p-FinFETs) have three main operating modes [5], namely, shorted-gate (SG) mode (in which the front and back gates are shorted to each other), low-power (LP) mode (in which the back gate is connected to a reverse-bias voltage), and independent-gate (IG) mode (in which the front and back gates are separated). For the purposes of the work described here, a p-FinFET is chosen for sensing the voltage variations on the basis of the following.

A p-FinFET will operate in LP mode if its back gate is in the reverse bias. This operation can be achieved by connecting the back gate to an independent source voltage with a DC value equal to VDD (i.e., VDD = 0.9 V) for the 32-nm FinFET [13], as shown in Fig. 2(a). If the back gate voltage is implemented so it fluctuates around VDD with an amplitude of 200 mV, then the maximum voltage difference between the back gate and the source ($|V_{bgs}|$ = 0.2 V) will always be smaller than the threshold voltage of the back gate ($|V_{thgb}| \approx 0.5$ V) [13]. Therefore, the back gate will always be turned off while still controlling the V_{th} of the front gate and the drain current. As a result, the p-FinFET will operate in a new mode where it is simultaneously in both LP and IG modes—LPIG mode. Fig. 2(b) shows the relationship between the drain current and the front gate voltage in the p-FinFET when the back gate voltage increases steadily from 0.7 V to 1.1 V in 50-mV increments. Obviously, in each front gate voltage, the drain current gradually diminishes as the back gate voltage
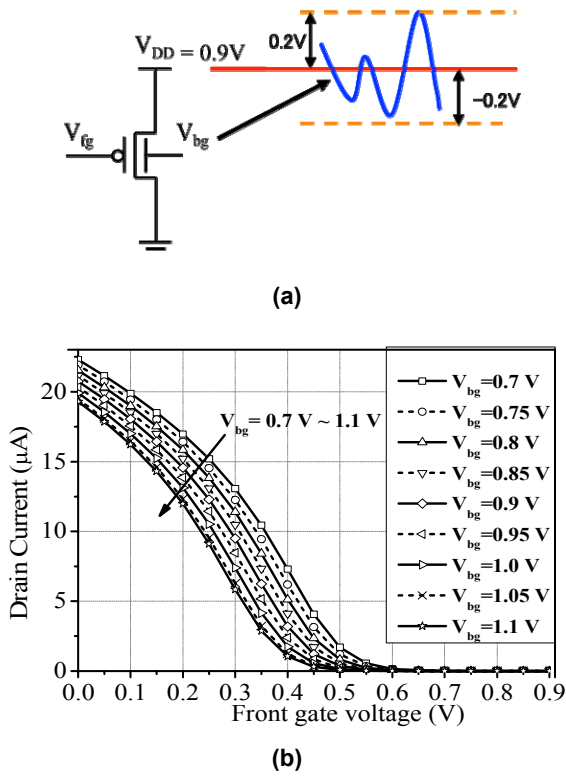
(a)

(b)

Fig. 2. (a) LPIG mode of a p-FinFET. (b) p-FinFET characteristics: drain current versus the front gate voltage with sweeping of the back gate voltage (V_{bg}: 0.7 ~ 1.1 V).

increases. This relationship is used to develop the voltage-sensing mechanism described in the next section.

2.3 Controllable Delay Element

In the LPIG CDE, the FinFET maintains low power consumption while its front and back gates are controlled by independent voltage sources. For this study, the LPIG CDE is applied to a digital voltage sensor to sense the input voltage in the range 0.7V to 1.1V at a high conversion rate (100 MHz).

Fig. 3 shows the proposed CDE, which consists of two inverters (Wn = Wp = 80 nm, and L = 32 nm) and two external capacitors, C_1 and C_2. The n-FinFETs are biased
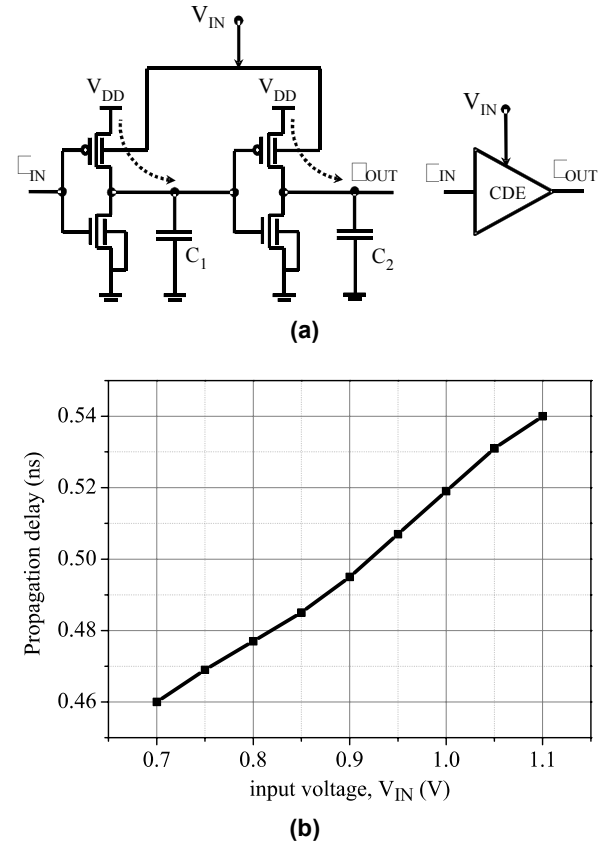

(a)

(b)

Fig. 3. Operating principle of the proposed controllable delay element. (a) Schematic and (b) propagation delay versus input voltage, V_{IN}.

in LP mode to minimize leakage. The p-FinFETs operate in LPIG mode to allow voltage measurement with minimum leakage. The operating principle of the FinFET-based CDE is described as follows. Supply voltage VDD of the 32-nm FinFET is 0.9 V. The clock signal arrives at the front gates of both n- and p-FinFETs, whereas the measured voltage (V_{IN}) within the range 0.7 V to 1.1 V is connected to the back gates of the p-FinFETs. The relationship in the FinFET between the threshold voltage at the front gate (V_{thgf}) and the voltage from back gate to the source (V_{bgs}) was explained clearly by Trivedi et al. [8] and can be simplified using the following equation for a p-FinFET:
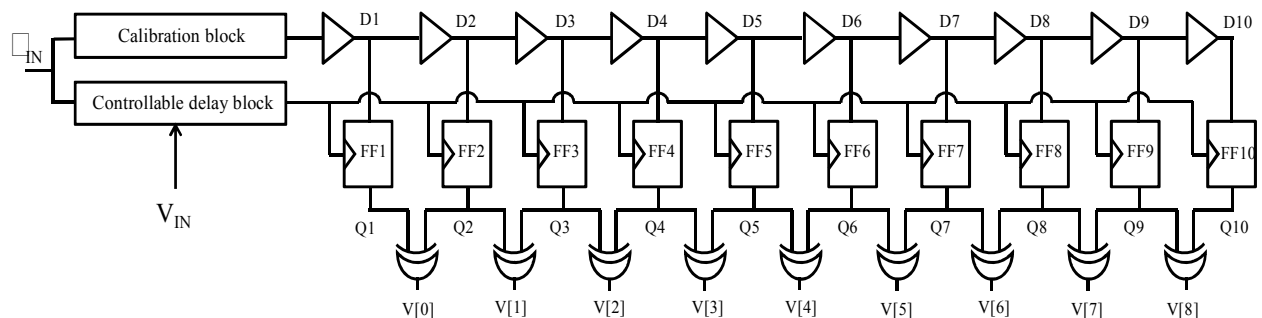

Fig. 4. A schematic of the proposed voltage sensor.

$$V_{thgf} = \begin{cases} V_{thgf}^0 - \delta\left(V_{bgs} - V_{thgb}\right), if \left|V_{bgs}\right| < \left|V_{thgb}\right| \\ V_{thgf}^0 \qquad\qquad\qquad\qquad otherwise \end{cases} \quad (1)$$

where δ is a positive value determined by the ratio of the gate and body capacitance; V_{thgf}^0 is the minimum observed V_{thgf}, and V_{thgb} is the back gate threshold voltage. We note two important points here: first, according to (1), V_{thgf} depends on V_{bgs} because $\left|V_{bgs}\right| < \left|V_{thgb}\right|$. Second, as the voltage biased at the back gate of the p-FinFET (V_{IN}) increases, V_{thgf} will be reduced, and therefore, drain current I_D will become smaller. If the external capacitors ($C_1 = C_2 = 14$ fF) are inserted behind each inverter, as shown in Fig. 3(a), the charging time of the capacitors can be managed effectively by controlling I_D through the back gates of the p-FinFET. Therefore, by varying the charging time of C_1 and C_2, the propagation delay of the clock input can also be controlled. Fig. 3(b) shows the relationship between V_{IN} and the propagation delay of the CDE as V_{IN} increases gradually from 0.7 V to 1.1 V in increments of 50 mV. The propagation delay of the CDE is linearly proportional to V_{IN}. The measured sensitivity of the CDE is $\Delta t_p / \Delta V_{IN} \approx 180 \; ps \cdot V^{-1}$, where t_p is the propagation delay of the clock through the CDE.

3. Proposed Digital Voltage Sensor

In the new CDE architecture proposed in Section 2, the CDE linearity region ranges from 0.7 V to 1.1 V, where VDD = 0.9 V is in the middle of this voltage range. This feature is important in on-chip voltage sensor applications in which the voltage varies around VDD by $\pm10\%$. In the sensor described in this paper, the voltage increases to $\pm 22\%$—a large range that can be used with dynamic voltage scaling (DVS) applications. Therefore, the voltage sensor is selected as the first application to test the new CDE technique. The proposed 32-nm FinFET-based voltage sensor shown in Fig. 4 consists of a controllable delay block, a calibration block, positive-edge flip-flops, and XOR gates. The operating principle of the proposed structure is as follows. Input clock signal Φ_{IN} is sent to the controllable delay (CDE) block and to the calibration block. In the CDE block, input voltage V_{IN} is sampled at each rising edge of the clock cycle. The change in V_{IN} is converted to a clock delay measured by the flip-flops (FFs). To calibrate the delay relative to the CDE block of the input to the flip-flops, the calibration block serves as a delay reference from which the output signal is also routed to the FFs' input. A series of buffers is inserted to separate the consecutive inputs, so that the delay difference for each FF between the input and the clock can be detected.

XOR gates are employed at the FFs' Q output to detect the differences between adjacent outputs. Only one XOR gate output will have a high value. The lookup table for output from the XOR gates is seen in Table 1, which shows the corresponding nine-bit digital codes of the sensor output for several values of V_{IN}. The calibration block, shown in Fig. 5, is a chain of six LP-FinFET

Table 1. Voltage sensor digital code table.

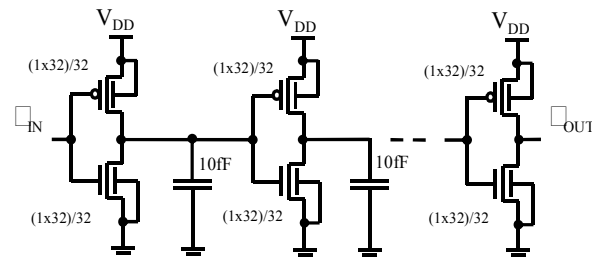| V_{IN}	Digital code								
(V)	V[0]	V[1]	V[2]	V[3]	V[4]	V[5]	V[6]	V[7]	V[8]
0.7	1	0	0	0	0	0	0	0	0
0.75	0	1	0	0	0	0	0	0	0
0.8	0	0	1	0	0	0	0	0	0
0.85	0	0	0	1	0	0	0	0	0
0.9	0	0	0	0	1	0	0	0	0
0.95	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	0	0
1.05	0	0	0	0	0	0	0	1	0
1.1	0	0	0	0	0	0	0	0	1

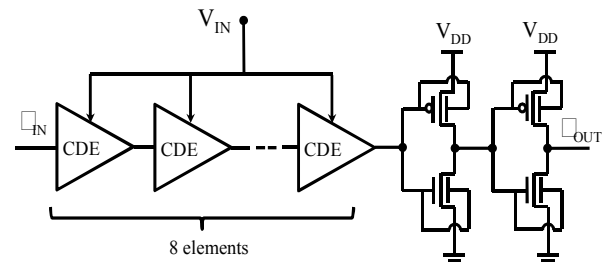**Fig. 5. A schematic of the calibration block with LP-FinFETs.**

Fig. 6. A schematic of the controllable delay block with CDEs.

repeaters. Each repeater is connected to a 10 fF external capacitor. Fig. 6 shows the structure of the controllable delay block in which the arrangement of the eight CDEs in series controls the rising edge of the input clock, depending on input voltage V_{IN}. The number of CDEs is determined by the lag between two adjacent D ports of the FFs. The clock signal is enhanced by the SG-FinFET repeater inserted at the end of the block. The FinFET-based FFs are designed to reduce the size [9], and thus, the power consumption.

4. Simulation Results

Several SPICE [16] simulations were conducted to test the operation of the proposed sensor under a range of voltages and process variations. A predictive technology model of the 32-nm FinFET [13] is adopted, and the actual
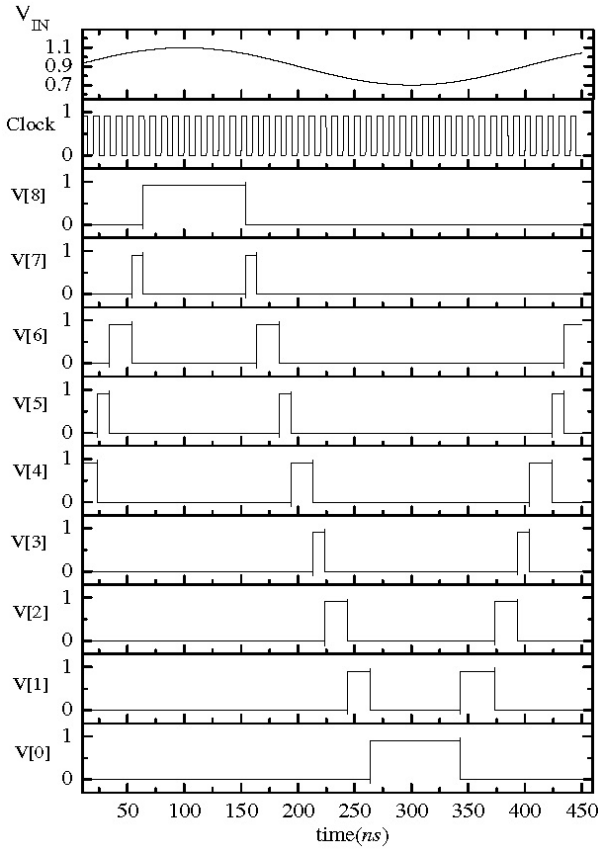
Fig. 7. Simulation results of voltage sensor under input voltage variation.

transistor sizes were described in the previous sections.

4.1 Voltage Variation

To generate voltage variations, a 2.5-MHz sinusoidal signal is used as V_{IN}, in conjunction with a 100-MHz sample clock. The waveform of V_{IN} and the corresponding V_{OUT} waveform are seen in Fig. 7, which shows that the sensor can correctly capture dynamic input. For each clock cycle, only one bit of output—indicated by value "1"—is being generated; otherwise, the value is set to "0". From this condition, the linearity characteristic of the proposed sensor is extracted, as shown in Fig. 8. The characteristic line of the output is quite close to the ideal curve, indicating that the proposed sensor works properly. In addition to the nominal supply voltage (0.9 V), several supply voltage variations are investigated as well. Even under a 50 mV variation in supply voltage (i.e., 0.85 V and 0.95 V), the proposed voltage sensor works properly, presenting different linearity.

4.2 Process Variation

Because process variation in chip manufacturing is one of the crucial causes of productivity and reliability degradation, it must be taken into account in the simulation. In the SPICE simulation, channel length L of the transistor
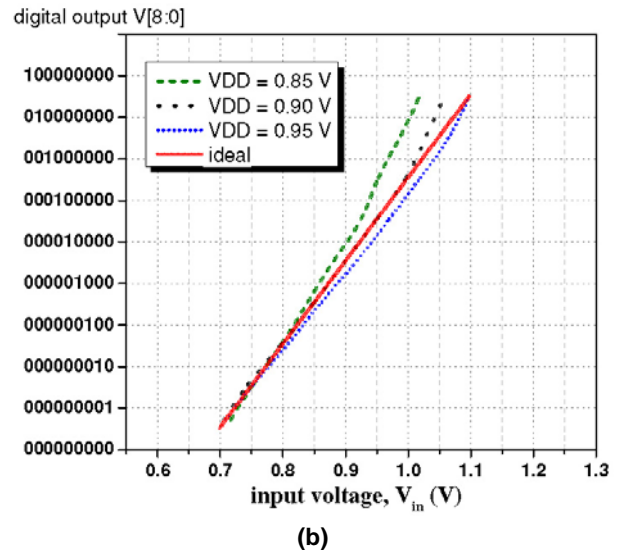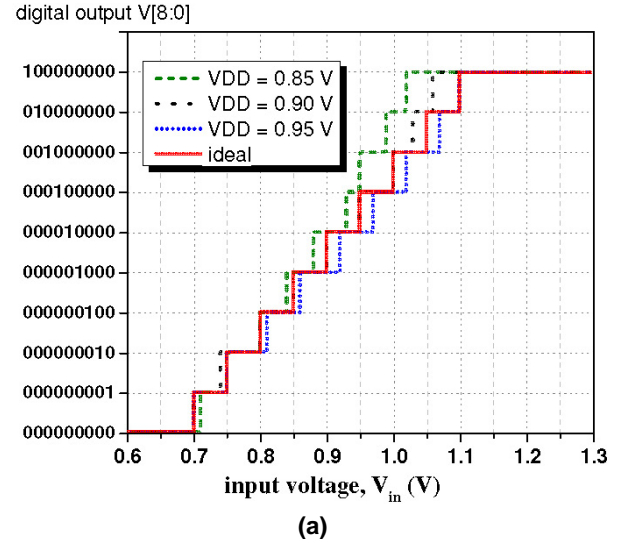

(a)

(b)

Fig. 8. (a) Digital output versus input voltage, V_{IN} at various supply voltage values. (b) Linearity charac-teristic.
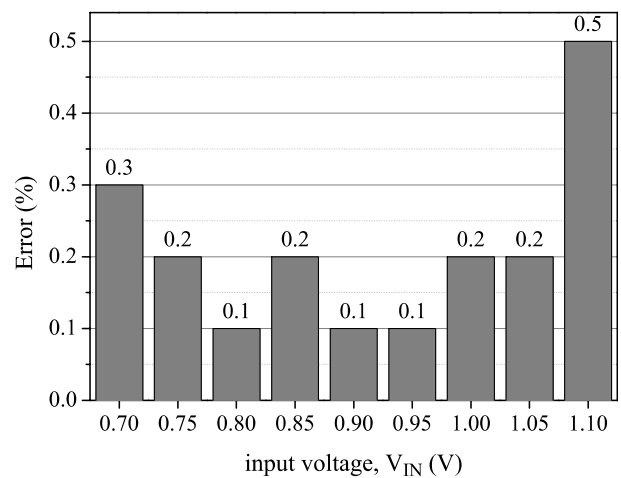

Fig. 9. Number of voltage sensor errors under process variation.

Table 2. Voltage sensor comparison.

parameters	[12]	[17]	[18]	Proposed Sensor
Supply Voltage (V)	1.2	1.8	1.0	0.9
Power (μW)	2100	400	780	21
Process	65 nm	180 nm	90 nm	32 nm
	CMOS	CMOS	CMOS	FinFET
Measurement range (V)	$0.8 - 1.8$	$0.0 - 1.2$	$0.2 - 1.0$	$0.7 - 1.1$
Resolution (mV)	200	~ 43	10 - 50	50
Frequency (MHz)	20.83	1.1	-	100

is randomly varied using a standard distribution with a mean of 32 nm and a 3σ range that includes all results within 10% of the mean. Then, the number of errors from 1000 Monte Carlo simulations is investigated. The results are seen in Fig. 9, which shows that the maximum error percentage is 0.5% (for $V_{IN} = 1.1$ V). Within the range 0.75 V to 1.05 V, the sensor returns a minimal number of errors ($\leq 0.2\%$). On the basis of these observations, the proposed sensor is determined to be reliable under process variation.

4.3 Power Consumption

The LPIG mode of the p-FinFET was discussed thoroughly in Section 3. To confirm whether the low-power mode of the FinFET device is maintained within LPIG mode, the power consumption levels of the various voltage sensors were assessed. Table 2 compares the proposed sensor with other design techniques. To the best of our knowledge, this design is the first approach using double-gate FinFET devices to develop an ADC. Although the other processes shown in Table 2 are not quite compatible, their measured power consumptions are significantly high. Table 2 shows that, at 21 μW, the power dissipation of the design proposed here is approximately 100 times smaller than that of Farahat et al. [12] and nearly 22 times and 37 times smaller than for Valero et al. [17] and Shang et al. [18], respectively, even though it operates at a high conversion rate (100 MHz) with comparable resolution. Under this condition, the voltage sensor that we developed can be seen as a low-power design.

5. Conclusion

In this paper, a novel design for a digital voltage sensor based on 32-nm FinFET devices was presented. By exploiting the characteristics of p-FinFETs in low-power mode, a new technique for using CDEs that effectively controls the propagation of the clock input was developed. On the basis of this condition, a design for a digital voltage sensor with a voltage range of 0.7 V to 1.1 V and a 50-mV

resolution was proposed. The performance of this sensor under voltage and process variations was evaluated using SPICE simulations. The simulation results confirm that the proposed voltage sensor can operate at ultra-low power consumption and a fairly high frequency with high linearity.

Acknowledgement

References

[1] B. Swahn, H. Soha, "Gate sizing: FinFETs vs. 32 nm bulk MOSFETs," *Design Automation Conference, 43rd ACM/IEEE*, pp. 528-531, 2006. Article (CrossRef Link)

[2] J. Muttreja, N. Agarwal, N. K. Jha, "CMOS logic design with independent-gate FinFETs,' *25th International Conference on Computer Design, ICCD* 2007, pp. 560-567, 7-10 Oct. 2007. Article (CrossRef Link)

[3] B.H. Calhoun, Yu Cao, Xin Li, Ken Mai, L.T. Pileggi, R.A. Rutenbar, K.L. Shepard, "Digital circuit design challenges and opportunities in the era of nanoscale CMOS," in *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343-365, Feb. 2008. Article (CrossRef Link)

[4] G. W. Roberts, M. Ali-Bakhshian, "A brief introduction to time-to-digital and digital-to-time converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 3, pp. 153-157, Mar. 2010. Article (CrossRef Link)

[5] S. W. Chen, M. H. Chang, W. C. Hsieh, W. Hwang, "Fully on-chip temperature, process, and voltage sensors," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 897-900, May 2010. Article (CrossRef Link)

[6] T. Watanabe, T. Mizuno, Y. Makino, "An all-digital analog-to-digital converter with 12-μV/LSB using moving-average filtering," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 120-125, Jan. 2003. Article (CrossRef Link)

[7] S. Taillefer, G. W. Roberts, "Delta Sigma A/D conversion via time-mode signal processing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 9, pp. 1908-1920, Sep. 2009. Article (CrossRef Link)

[8] V. P. Trivedi, J. G. Fossum, W. Zhang, "Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra thin devices," *Solid State Electronics*, pp. 170-178, Jan. 2007. Article (CrossRef Link)

[9] S. A. Tawfik, V. Kursun, "Characterization of new static independent-gate-biased FinFET latches and flip-flops under process variations," in *Proceedings of 9th International Symposium on Quality Electronic Design, ISQED* 2008, pp. 311-316, Mar. 2008.

Article (CrossRef Link)

[10] Y. J. Cho, S. H. Lee, "An 11b 70-MHz 1.2-mm2 49-mW 0.18μm CMOS ADC with on-chip current/voltage references," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1989-1995, Oct. 2005. Article (CrossRef Link)

[11] H. Farkhani *et al*., "A fully digital ADC using a new delay element with enhanced linearity," *IEEE International Symposium on Circuits and Systems, ISCAS* 2008, pp. 2406-2409, May 2008. Article (CrossRef Link)

[12] M. A. Farahat, F. A. Farag, H. A. Elsimary, "Only digital technology analog-to-digital converter circuit," in *Proceedings of IEEE 46th Midwest Symposium on Circuits and Systems*, 2003, pp. 178-181, Dec. 2003. Article (CrossRef Link)

[13] Y. Cao, PTM, [Online]. Available: Article (CrossRef Link)

[14] T. Watanabe, Y. Makino, Y. Ohtsuka, S. Akita, T. Hattori, "A CMOS time-to-digital converter LSI with half-nanosecond resolution using a ring gate delay line," *IEICE Transaction on Electron*, pp. 1774-1779, Dec. 1993.

[15] H. V. Nguyen and Y. Kim, "32nm FinFET-based 0.7-to-1.1 V Digital Voltage Sensor with 50mV Resolution", in *IEEE Proceedings of the ICICDT'12*, May 2012.

[16] HSPICE, F-2011.09-SP1, Article (CrossRef Link)

[17] M. R. Valero, S. Celma, B. Calvo and N. Medrano, "CMOS Voltage-to-Frequency Converter with Temperature Drift Compensation," in *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 9, pp. 3232-3234, Sept. 2011. Article (CrossRef Link)

[18] D. Shang, F. Xia and A. Yakovlev, "Wide-range, reference free, on-chip voltage sensor for variable Vdd operations," *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, Beijing, 2013, pp. 37-40. Article (CrossRef Link)

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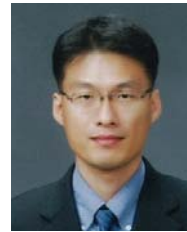
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