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Device Coupling Effects of Monolithic 3D Inverters

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Abstract

The device coupling between the stacked top/bottom field-effect transistors (FETs) in two types of monolithic 3D inverter (M3INV) with/without a metal layer in the bottom tier is investigated, and then the regime of the thickness T_{ILD} and dielectric constant ε_r of the inter-layer distance (ILD), the doping concentration N_d (N_a), and length L_g of the channel, and the side-wall length L_{SW} where the stacked FETs are coupled are studied. When N_d (N_a) < 10^{16} cm^{-3} and L_{SW} < 20 nm, the threshold voltage shift of the top FET varies almost constantly by the gate voltage of the bottom FET, but when N_d (N_a) > 10^{16} cm^{-3} or L_{SW} > 20 nm, the shift decreases and increases, respectively. M3INVs with $T_{ILD} \geq 50$ nm and $\varepsilon_r \leq 3.9$ can neglect the interaction between the stacked FETs, but when T_{ILD} or ε_r do not meet the above conditions, the interaction must be taken into consideration.

Index Terms: 3D integrated circuit (3D IC), Coupling, Monolithic 3D IC, Parasitic extraction, Threshold voltage

I. INTRODUCTION

Three-dimensional (3D) integrated-circuits (ICs) have better performance and energy efficiency, and a smaller footprint in electronic systems than two-dimensional (2D) ICs because of their smaller form factor due to 3D stacking and 3D interconnections [1]. Compared with the currently available through-silicon via (TSV)-based 3D ICs [2], the monolithic 3D IC (M3IC) [3-12], in which each circuit layer is thin and is fabricated directly over the previous circuit layers on the same substrate, is a promising technology that enables ultrafine-grained vertical integration of devices and interconnections with the conventional monolithic inter-tier vias (MIVs) to connect the various layers.

There have been extensive studies of process, device, and circuit technologies for the M3IC [3-12]. SRAM and inverters utilizing dynamic threshold voltage (V_{TH}) modification thanks to the electrical coupling between stacked top and bottom metal-oxide-semiconductor field-effect transistors (MOSFETs) have been demonstrated when the inter-layer dielectric (ILD) is very thin (tens of nanometers) [12]. However, to our knowledge, no studies have been published that evaluate a regime in which the electrical coupling between the stacked FETs is either considered or not. Therefore, to design and analyze M3ICs precisely with an ultra-thin ILD, regimes in which the electrical coupling between the stacked FETs is included must be systematically investigated.

In this paper, the electrical coupling between the stacked top/bottom FETs in two types of monolithic 3D inverter (M3INV), of which one includes a metal layer (ML) in the bottom tier and the other does not include a ML, will be systematically investigated using a 3D device simulator. Device characteristics of the two types of M3INV will be surveyed in terms of electrical coupling between the stacked top/bottom FETs (Section II). Next, the regime of the sizes

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and materials of the ILD, as well as the doping concentration and length of channel where the stacked FETs are coupled will be studied (Section III). Finally, Section IV will conclude this paper.

II. DEVICE CHARACTERISTICS OF THE M3INV

Fig. 1 shows the schematics of two examples of types of M3INV structure. Fig. 1(a) and (b) show Structure A [9,10], which includes the MLs between the top and bottom tiers and Structure B [3, 6], which excludes them, respectively. Fig. 1(c) shows the cross-section of A-A′ in Structure A shown in Fig. 1(a). The cross-section of A-A′ in Structure B is the same as that shown in Fig. 1(c) except that MLs (Part A) and contacts (Part B) would be added. Here L_g, L_{sw}, L_{ldd}, L_c, T_g, T_{ox}, T_{si}, T_{sw}, T_{BOX}, T_{sub}, T_c, T_{ILD}, T_{cg}, and T_m denote gate length, sidewall length, lightly-doped drain length, contact length, gate thickness, gate-oxide thickness, silicon-channel thickness, side-wall thickness, buried-oxide thickness, silicon-substrate thickness, contact thickness, ILD thickness, bottom-gate contact thickness, and ML thickness, respectively. To compensate for the hole/electron mobility skew, the width of the PMOSFET is larger than that of the corresponding NMOSFET. To increase the cell footprint by allowing for extra space for MIVs (or contacts) connecting the top and bottom tiers, the PMOSFET and NMOSFET are placed on the bottom and top tiers, respectively [9]. Each MOSFET consists of a source (S)/drain (D) highly doped with 10^{21} cm^{-3} and lightly-doped with 10^{18} cm^{-3}, the gate-oxide (SiO_2), and the polysilicon gate (G). L_{sw}, L_{ldd}, L_c, T_{BOX}, T_{sub}, T_c, T_{cg}, and T_m are fixed as 10, 10, 50, 30, 50, 6, 100, and 100 nm, respectively. According to the technology roadmap of the fully-depleted silicon-on-insulator (FDSOI) [1, 13], L_g ($\approx T_g$), T_{ox}, T_{si}, and T_{sw} ($=T_g+T_{ox}$) are varied, and T_{ILD} is also varied to investigate the coupling effect.

Fig. 2 shows the DC/AC coupling between the bottom and top MOSFETs with L_g = 30 nm, T_{si} = 6 nm, and T_{ox} = 1 nm [13] in the M3INV cells with the ultra-thin ILD (T_{ILD} = 10 nm), using the 3D technology computer-aided design (TCAD) numerical simulator, ATLAS [14]. Fig. 2(a), (b), and (c) show the drain-source current (I_{nds}), trans-conductance ($g_m = dI_{nds}/dV_{ngs}$), and capacitances (C_{ngng}, C_{nsng}, C_{dng}, C_{pgng}) versus the top-gate voltage V_{ngs} of the top NMOSFET at different bottom-gate voltages V_{pgs}'s (0 and –1 V), respectively. The drains in both the bottom and top MOSFETs are common and can be operated as the output. The sources and gates in the bottom and top MOSFETs are grounded and separated, respectively. The drain-source voltage V_{ds} is biased as 0.1 V. In Fig. 1(b) and (c), frequency f = 1 MHz is applied for AC characterization. The electrical coupling of the bottom PMOSFET due to the gate of the top NMOSFET can be ignored [11].

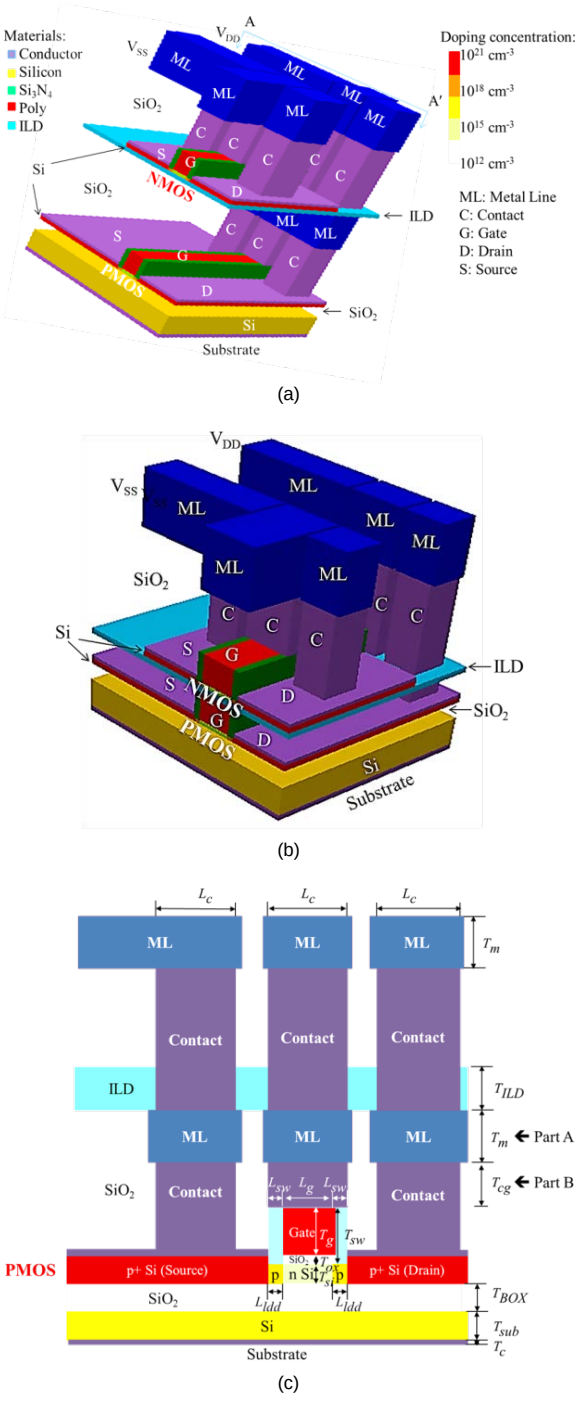
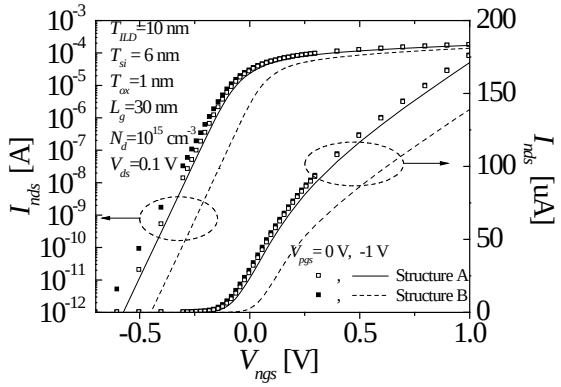
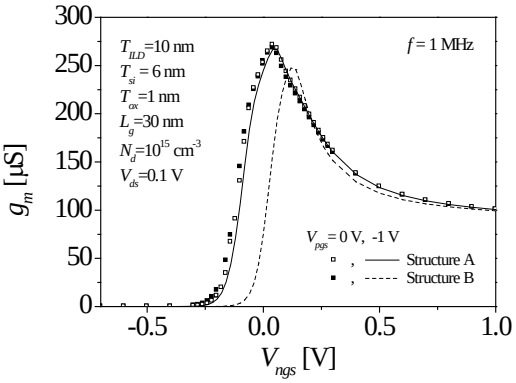


Fig. 1. Schematics of two types of monolithic 3D inverter cells. (a) 3D schematic of Structure A with a metal layer in the bottom tier, (b) 3D schematic of Structure B without the metal layer, and (c) cross-section of A-A′ in Structure A shown in Fig. 1(a). ML, C, G, D, and S denote the metal layer, contact, gate, drain, and source, respectively. Materials in the structure and doping concentration in the silicon body are denoted by color.

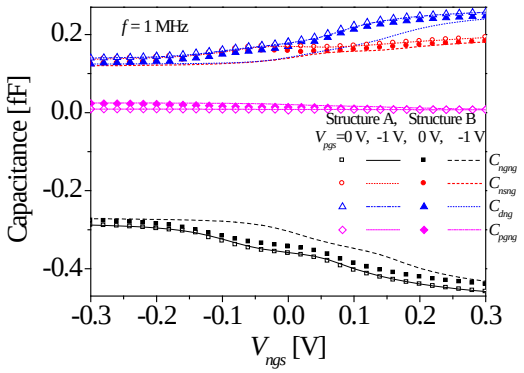
In this paper, the electrical coupling of the top NMOSFET will be quantified when the gate of the bottom PMOSFET is biased as two different voltages (0 and –1 V).



(a)

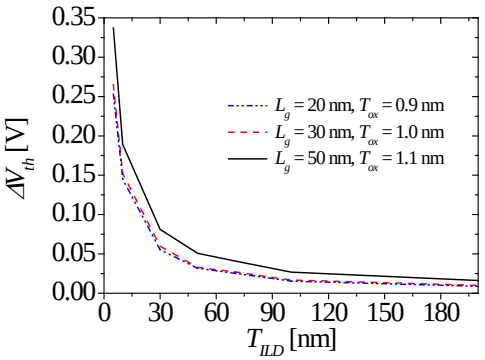


(b)

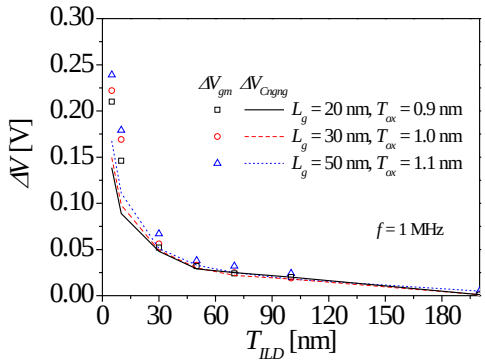


(c)

Fig. 2. (a) I_{nds}-V_{ngs} characteristics (linear and logarithmic), (b) transconductance ($g_m = dI_{nds}/dV_{ngs}$), and (c) capacitance (C_{ngng}, C_{nsng}, C_{dng}, C_{pgng}) of the top transistor in the M3INV cells (Structure A and B) as shown in Fig. 1(a) and (b). Symbols and lines denote V_{pgs} = 0 and -1 V, respectively. Empty and filled symbols denote Structure A and B, respectively. Here, L_g = 30 nm, T_{Si} = 6 nm, T_{ox} = 1 nm, T_{ILD} = 10 nm, N_d (N_a) = 10^{15} cm^{-3}, and V_{ds} = 0.1 V. f = 1 MHz is applied for AC characterization. The subscripts nds, ngs, pgs, ngng, nsng, dng, and pgng denote drain-to-source of the NMOSFET, gate-to-source of the NMOSFET, gate-to-source of the PMOSFET, gate-to-gate of the NMOSFET, source-to-gate of the NMOSFET, drain-to-gate of the NMOSFET, gate of the PMOSFET-to-gate of the NMOSFET, respectively.



(a)



(b)

Fig. 3. (a) Threshold voltage shift and (b) voltage shift of transconductance (g_m) and transcapacitance (C_{ngng}) of the top transistor in the M3INV cell (Structure B) as shown in Fig. 1(b). Here, N_d (N_a) = 10^{15} cm^{-3} and V_{ds} = 0.1 V. Frequency f = 1 MHz is applied for AC characterization.

Empty and filled symbols denote Structure A and B, respectively, and symbols and lines denote V_{pgs} = 0 and –1 V, respectively. I_{nds}–V_{ngs}, g_m, C_{ngng}, C_{nsng}, C_{dng}, and C_{pgng} of the top NMOSFET in Structure A and B have small and large differences between V_{pgs} = 0 and –1 V, respectively. As shown in Fig. 2, the electrical coupling can be ignored when the distance between the channel of the top NMOSFET and the gate of the bottom PMOSFET is over 100 nm (e.g., 210 nm at Structure A) and the electrical coupling should be considered when it is below 100 nm (e.g., 10 nm at Structure B).

III. DEVICE COUPLING IN THE M3INV

Under what geometry or process conditions may the electrical coupling between the bottom and top MOSFETs be neglected? In order to investigate the coupling effect in three types of Structure B, the threshold voltage shift (ΔV_{th}), the voltage shifts of transconductance g_m (ΔV_{gm}), and the top gate-to-top gate capacitance C_{ngng} (ΔV_{Cngng}) for electrical

coupling were systematically quantified for various values of T_{ILD}, the dielectric constant ε_r of ILD, while the doping concentrations N_d (or N_a) in the channel were simulated with the 3D TCAD numerical simulator, as shown in Figs. 3 and 4. Threshold voltage V_{th} is defined as V_{ngs} when $I_{nds} = 10^{-7}$ A. ΔV_{th}, ΔV_{gm}, and ΔV_{Cngng} are defined as the differences between V_{th}s and V_{ngs}s at the maximum g_m, and V_{ngs}s at maximum dC_{ngng}/dV_{ngs} of the top NMOSFET between V_{pgs} = 0 and –1 V, respectively. Among three types of Structure B, one is L_g = 50 nm, T_{si} = 10 nm, and T_{ox} = 1.1 nm, another is L_g =30 nm, T_{si} = 6 nm, and T_{ox} = 1 nm, and the third is L_g = 20 nm, T_{si} = 6 nm, and T_{ox} = 0.9 nm, which follows the FDSOI technology roadmap guideline [1, 12]. Fig. 3(a) and (b) show ΔV_{th} and ΔV_{gm} (or ΔV_{Cngng}) versus T_{ILD}, respectively. When T_{ILD} values are over 50 nm, ΔV_{th}, ΔV_{gm}, and ΔV_{Cngng} are below 50 mV, and thus the coupling in the structures can be ignored. However, when T_{ILD} values are below 50 nm, the coupling must be considered.

Figs. 4(a) and (b) show ΔV_{th} versus the dielectric constant ε_r of the ILD and ΔV_{th} versus the doping concentration N_d (or N_a) in the channel, respectively.

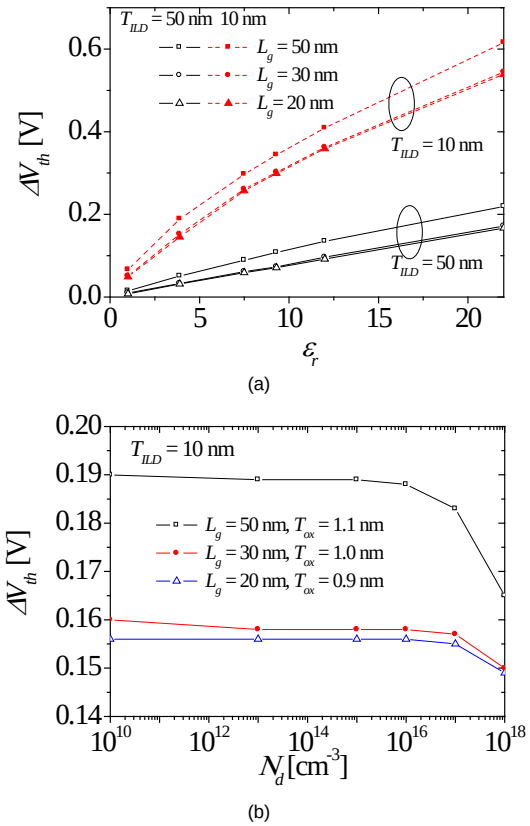


Fig. 4. Threshold voltage shift of the top transistor in the M3INV cell (Structure B) as shown in Fig. 1(b). (a) Material dependence in IML at T_{ILD} = 10 and 50 nm, and (b) doping concentration dependence in the silicon channel at T_{ILD} = 10 nm. Here V_{ds} = 0.1 V.

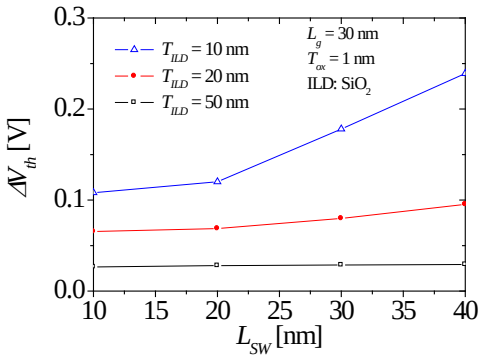


Fig. 5. Threshold voltage shift versus side-wall length of the top transistor in the M3INV cell at different T_{ILD}s. Here L_g = 30 nm and V_{ds} = 0.1 V.

In Fig. 4(a), as ε_r increases, ΔV_{th} increases in all of three types of Structure B. In Fig. 4(b), as the doping concentration increases to over 10^{16} cm^{-3}, ΔV_{th}s decreases in all three types of Structure B. Likewise, at all doping concentrations in the channel below 10^{16} cm^{-3}, ΔV_{th}s is almost constant in all of the three types of Structure B.

Fig. 5 shows ΔV_{th}s versus the side-wall length L_{SW} of the top transistor in the M3INV cell at different T_{ILD}s. As the T_{ILD} decreases, ΔV_{th} increases in all regimes of L_{SW} in all of three types of Structure B, and in all regimes of L_{SW} below 20 nm, the ΔV_{th}s are almost constant in all of the three types of Structure B.

When $T_{ILD} \geq$ 50 nm and $\varepsilon_r \leq$ 3.9 in Structure B, the interaction between the stacked MOSFETs can be neglected, but for one with an ILD thickness or material that does not fit the above conditions, the interaction must be considered.

IV. CONCLUSIONS

In this paper, we investigated the electrical coupling between the stacked top/bottom FETs in the M3INV. To investigate the coupling between the stacked devices, the drain-source currents versus the gate voltage of the bottom FET in the M3INV were simulated using a 3D device simulator with varying channel length, thickness of the ILD, material of the ILD, doping concentration in the channel, and side-wall length. When the doping concentration was below 10^{16} cm^{-3} and the side-wall length was below 20 nm, the threshold voltage shifts are almost constant in all of the three types of Structure B. The interaction between the stacked MOSFETs can be neglected in the M3INV with $T_{ILD} \geq$ 50 nm and $\varepsilon_r \leq$ 3.9, but the interaction must be taken into account with ILD thicknesses and materials with other values. Thus a new method for accurate simulation in conventional circuit simulators may be required for circuits consisting of coupled devices.

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