Journal of information and communication convergence engineering
http://jicce.org

J. Inf. Commun. Converg. Eng. 14(4): 268-271, Dec. 2016 Regular paper

Inductive Switching Noise Suppression Technique for Mixed-Signal ICs Using Standard CMOS Digital Technology

Hyungjin Im*and Ki Hyuk Kim, ***Member, KIICE***

SK Hynix Memory Solutions, San Jose, CA 95118, USA

Abstract

An efficient inductive switching noise suppression technique for mixed-signal integrated circuits (ICs) using standard CMOS digital technology is proposed. The proposed design technique uses a parallel RC circuit, which provides a damping path for the switching noise. The proposed design technique is used for designing a mixed-signal circuit composed of a ring oscillator, a digital output buffer, and an analog noise sensor node for 0.13-μm CMOS digital IC technology. Simulation results show a 47% reduction in the on-chip inductive switching noise coupling from the noisy digital to the analog blocks in the same substrate without an additional propagation delay. The increased power consumption due to the damping resistor is only 67% of that of the conventional source damping technique. This design can be widely used for any kind of analog and high frequency digital mixed-signal circuits in CMOS technology.

Index Terms: CMOS, Mixed signal, Switching noise

I. INTRODUCTION

Owing to the improvement of CMOS technology, single-chip integrations of complex mixed-signal systems have been widely studied. Such system-on-chips (SOCs) consist of a large-area digital signal processing block and a small-area but crucial analog block. Highly doped silicon substrates are a strong candidate for SOC applications because the latch-up problems of the large-area digital block can be abated. However, it is difficult to suppress propagations of the inductive switching noise in a highly doped substrate using conventional noise suppression techniques such as guard ring structures and physical isolation techniques, because the highly doped silicon substrate acts as an electrical single node [1]. In order to suppress the propagation of the switching noise in the highly doped substrate, several expensive structural approaches such as triple-well, SOI, and backside-etched substrates have been proposed [2, 3].

The propagation of the switching noise can also be suppressed by minimizing the generation of the inductive switching noise using several circuit-level techniques such as source damping resistors [4], lossy on-chip decoupling capacitors [5], and resonant forward-biased guard rings [6]. However, their applications are limited by the increased propagation delay and power consumptions, the sensitivity to integrated circuit (IC) process variations, and the narrow operating bandwidth. In this letter, we present a simple and efficient on-chip switching noise suppression technique using a parallel RC damping path.

Received 06 December 2016, **Revised** 08 December 2016, **Accepted** 10 December 2016
***Corresponding Author** Hyungjin Im (E-mail: hyungjin.im@skhms.com, Tel: +1-408-876-7198)
SK Hynix Memory Solutions, San Jose, CA 95118, USA.

Open Access http://doi.org/10.6109/jicce.2016.14.4.268 print ISSN: 2234-8255 online ISSN: 2234-8883

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/3.0/) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Copyright ⓒ The Korea Institute of Information and Communication Engineering

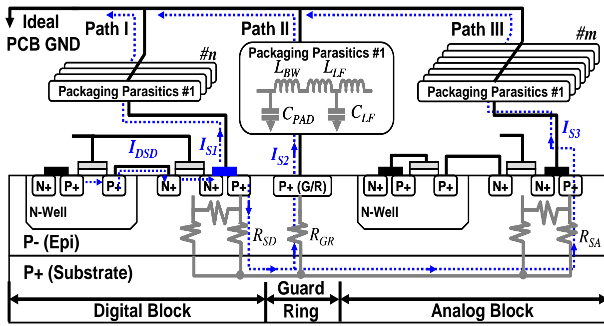

Fig. 1. Comparison between service disruption periods in each protocol: impact of link delay between local mobility anchor (LMA) and mobile access gateway (MAG).

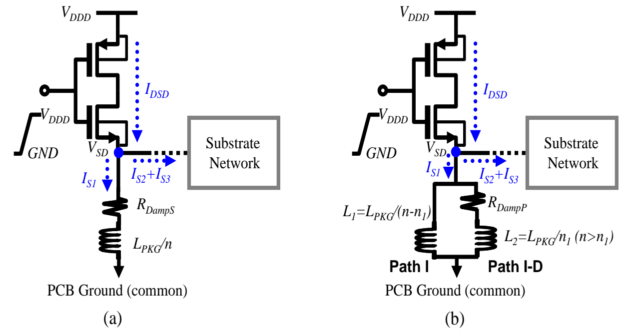

Fig. 2. (a) Equivalent circuit of conventional resistive source damping technique. (b) Equivalent circuit of proposed damping technique.

II. PROPOSED ON-CHIP INDUCTIVE NOISE SUPPRESSION TECHNIQUE

Fig. 1 shows a schematic representation of a simplified mixed-signal IC and the parasitic components related to the inductive switching noise. For the sake of brevity, only the parasitic components of the ground paths are shown in Fig. 1. R_{SD}/R_{SA} and R_{GR} are the P+ to substrate resistances of the NMOS transistor in the digital/analog block and the guard ring, respectively. The “packaging parasitics” block consists of the bonding wire self-inductance, L_{BW}; the lead-frame self-inductance, L_{LF}; the bonding pad to the ground capacitance, C_{PAD}; and the lead frame to the ground capacitance, C_{LF}. Here, n and m denote the numbers of the assigned package pins for the digital and analog blocks, respectively. Note that R_{SD}, R_{GR}, and R_{SA} are proportional to their areas and perimeters, and the impedance of the “packaging parasitics” blocks is inversely proportional to the number of blocks. Typically, the digital block has the largest area and the analog ground path has the lowest impedance in order to address RF grounding and thermal dissipating issues. I_{DSD} denotes the wide bandwidth transient current in the digital block, and I_{S1}, I_{S2}, and I_{S3} represent the currents in each return path for I_{DSD}. There are three current return paths for I_{DSD}: one is the intended digital ground path (Path I) composed of the *n* parallel “packaging parasitics” blocks, and the other two parasitic paths are the guard ring path (Path II) composed of R_{SD}, R_{GR}, and a single “packaging parasitics” block and the analog ground path (Path III) composed of R_{SD}, R_{SA}, and the *m* parallel “packaging parasitics” blocks. On the basis of this equivalent circuit model, note that the noise generation, propagation, and injection processes are not sequential but quasi-static. Further, note that the transient current finds the lowest impedance path, which means that the wide bandwidth switching current can flow not only through the digital ground path but also through the analog ground path, which has the lowest package parasitic impedance due to the largest number of “packaging parasitics” blocks. Because the impedance of the guard ring is the highest among the paths, the guard ring structure is of no use in such substrates.

The proposed on-chip inductive switching noise suppression technique is a method that damps the inductive switching noise with negligible power consumption and no additional propagation delay caused by the damping resistors.

Fig. 2(a) and (b) show the equivalent circuits of the conventional resistive source damping [4] and the proposed damping techniques, respectively. L_{PKG} denotes the summation of L_{BW} and L_{LF} and the capacitances of the “packaging parasitics” blocks, and V_{DDD} stands for the power supply voltage for the digital block. R_{DampS} and R_{DampP} represent the resistance of the conventional resistive source damping and that of the proposed techniques, respectively. In Fig. 2(b), the current return path is divided into the original digital ground and the proposed parallel damping paths. During the switching time, most of the switching current flows through Path I because of its lower impedance. After the switching activity, Path I-D provides the resistive damping path for the inductive switching noise. If the high frequency responses of V_{SD} is ignored ( ), then the optimal value of R_{DampP} is given by

$$R_{DampP} \approx \left[(L_1 + L_2)^2 / (4 C_{out} L_1) \right]^{0.5}, \qquad (1)$$

where L_1 and L_2 denote the total inductance of Path I and that of Path I-D, respectively, and C_{out} represents the total output capacitance of the switching logic gates in the digital block.

III. SIMULATION RESULTS

The proposed on-chip switching noise suppression technique is applied to the design of a mixed-signal IC. The digital block consists of a 7-stage ring oscillator and a

stepped output buffer, and the analog block is simplified as a P+ noise sensor node, as shown in Fig. 3. The mixed-signal circuit is designed using UMC 0.13-μm digital CMOS design kits. The published values of the packaging parasitic components are used [7], and C_{INT} represents the on-chip interconnection capacitance to the digital ground path. The resistances of the P+ contact to the substrate are numerically simulated using Maxwell 2D SV, a commercial 2D quasi-static R, L, and C extractor from Ansoft Corp. A commercial circuit-level simulator, Spectre from Cadence Design Systems, Inc., is used for simulating the performances of the mixed-signal circuit.

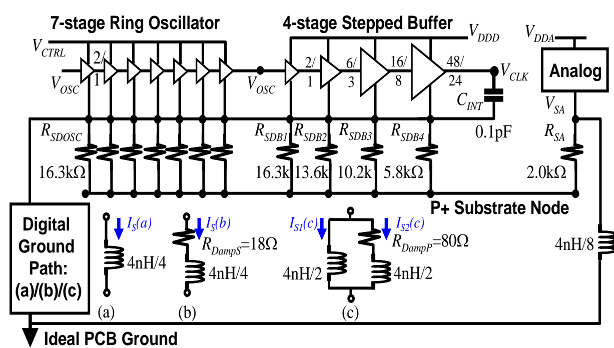

Fig. 3. Schematic representation of simulated mixed-signal IC in standard 0.13-μm CMOS technology.

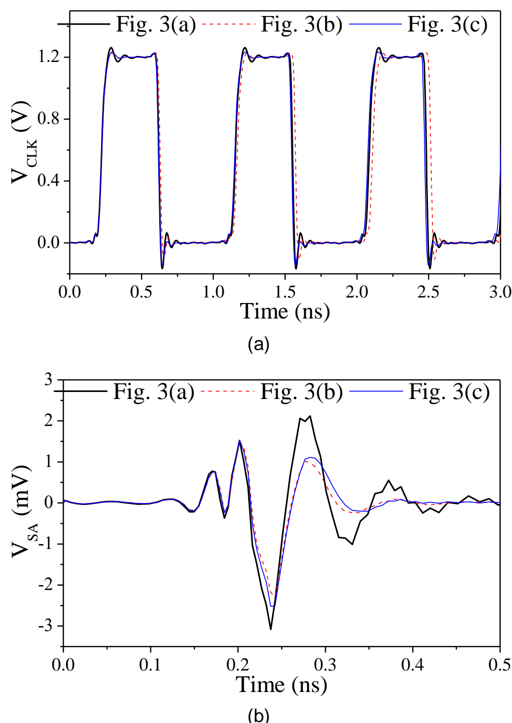

Fig. 4. (a) Output voltage waveform of stepped buffer. (b) Propagated voltage waveform to analog block. (c) Transient currents of each ground path.

Fig. 4(a) and (b) show the simulated output voltage waveforms of the stepped buffer (V_{CLK}) and the propagated voltage waveforms to the analog block (V_{SA}), respectively. R_{DampS} is selected to ensure that the noise damping characteristics of the digital ground path (b) and (c) are identical to each other. In both cases, the propagated noise voltages, V_{SA}, are reduced by more than 47% of that of the ground path (a), as shown in Fig. 4(b). However, the source damping resistor brings degradations of the rising/falling time and, consequently, the accumulated time delay of the V_{CLK}, which results in the time domain jitter observed in Fig. 4(a). The peak values of I_S(b) and I_{S2}(c) are 3.03 mA and 0.911 mA, respectively, and the calculated power consumption ($P = I^2R$) of R_{DampP} is only 67% of that of R_{DampS}.

IV. DISCUSSION AND CONCLUSION

An inductive switching noise suppression technique for the CMOS digital IC technology is proposed, and its noise suppression characteristics are compared with previous structures in terms of the noise suppression level, additional propagation delay, and increased power consumption. The proposed noise suppression technique shows more than 47% reduction of the propagated noise voltage without an additional propagation delay, and the increased power consumption is only 67% of that of the conventional source damping technique.

REFERENCES

[1] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, “Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits,” *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 420-430, 1993.

[2] P. Basedau and Q. Huang, “A post processing method for reducing substrate coupling in mixed-signal integrated circuits,” in *Proceedings of 1995 Symposium on VLSI Circuits (Digest of Technical Papers)*, Kyoto, Japan, pp. 41-42, 1995.

[3] S. Ardalan and M. Sachdev, “An overview of substrate noise reduction techniques,” in *Proceedings of 5th International Symposium on Quality Electronic Design (ISQED),* San Jose, CA, pp. 291-296, 2004.

[4] R. Senthinathan, J. L. Prince, and S. Nimmagadda, “Noise immunity characteristics of CMOS receivers and effects of skewing/damping CMOS output driver switching waveform on the ‘simultaneous’ switching noise,” *Microelectronics Journal*, vol. 23, no. 1, pp. 29-36, 1992.

[5] P. Larsson, “Resonance and damping in CMOS circuits with on-chip decoupling capacitance,” *IEEE Transactions on Circuits and*

Systems I: Fundamental Theory and Applications, vol. 45, no. 8, pp. 849-858, 1998.

[6] L. Forbes, B. Ficq, and S. Savage, "Resonant forward-biased guard-ring diodes for suppression of substrate noise in mixed-mode CMOS circuits," *Electronics Letters*, vol. 31, no. 9, pp. 720-721, 1995.

[7] B. E. Owens, S. Adluri, P. Birrer, R. Shreeve, S. K. Arunachalam, K. Mayaram, and T. S. Fiez, "Simulation and measurement of supply and substrate noise in mixed-signal ICs," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 382-391, 2005.

Hyungjin Im

received his B.Eng. and M.Sc. in Electrical and Electronic Engineering from Korea University, Seoul, South Korea, in 2001 and 2003, respectively. Since then, he has worked with Samsung Electronics Inc., and SK Hynix Memory Solutions, USA, where he is currently the principal engineer in the R&D department.

Ki Hyuk Kim

The second author's biography is not available at the time of the publication.