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# Crystallization and Characterization of GeSn Deposited on Si with Ge Buffer Layer by Low-temperature Sputter Epitaxy

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**Abstract—Recently, GeSn is drawing great deal of interests as one of the candidates for group-IV-driven optical interconnect for integration with the Si complementary metal-oxide-semiconductor (CMOS) owing to its pseudo-direct band structure and high electron and hole mobilities. However, the large lattice mismatch between GeSn and Si as well as the Sn segregation have been considered to be issues in preparing GeSn on Si. In this work, we deposit the GeSn films on Si by DC magnetron sputtering at a low temperature of 250°C and characterize the thin films. To reduce the stresses by GeSn onto Si, Ge buffer deposited under different processing conditions were inserted between Si and GeSn. As the result, polycrystalline GeSn domains with Sn atomic fraction of 6.51% on Si were successfully obtained and it has been demonstrated that the Ge buffer layer deposited at a higher sputtering power can relax the stress induced by the large lattice mismatch between Si substrate and GeSn thin films.**

***Index Terms*—GeSn, group IV, optical interconnect, Si CMOS, Sn segregation, DC magnetron sputtering, low temperature, polycrystalline GeSn**

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## I. INTRODUCTION

In recent days, near-infrared (NIR) Si photonics is gaining great deal of attention for on-chip optical interconnect as one of the promising solutions for overcoming the issues of conventional metallic interconnection in the very-large-scale-integration (VLSI) systems including tremendous heat dissipation and RC delay dominating the degradation of integrated circuit (IC) performances [1-3]. For realizing the optical interconnect components integrated with Si complementary metal-oxide-semiconductor (CMOS) circuitry, Ge-on-Si platform has been widely studied [4-6], owing to high Si compatibility, high electron and hole mobilities, and pseudo-direct energy-band structure of Ge where the global and local conduction band minima are located at the Γ- and L-valleys, respectively. The energy bandgap ($E_G$) of Ge is reduced by incorporation of Sn and Ge turns into a direct-bandgap semiconductor material at Sn content of near 8% [7-9]. Incorporation of Sn into Ge improves both electron and hole mobilities in the GeSn alloy and increases radiative recombination probability. For these reasons, introducing Sn into the Ge matrix substantially enhances the electrical and optical properties of Ge and provides GeSn with the virtuous features as base materials for high-speed high-efficiency passive and active devices in the Si electronics-photonics integrated system. However, Sn segregation has been widely observed during the post-deposition heat treatment regardless of processing tools such as chemical vapor deposition (CVD), molecular beam epitaxy (MBE), and evaporation [10-13]. The undesirable Sn segregation

**Fig. 1.** Schematics of the prepared GeSn films (a) Sample 1: GeSn directly on Si without Ge buffer. GeSn-on-Si samples with Ge buffers prepared at (b) 30-W (Sample 2), (c) 500-W (Sample 3) DC sputtering powers.

leading to a non-uniform vertical distribution of Sn atoms across the GeSn layer is fundamentally caused by the low equilibrium solid solubility of Sn in Ge below 1 atomic % (at. %), which demands on better methods for stable crystallization of the GeSn thin films [14].

In this work, GeSn is deposited on Si substrate by DC magnetron sputtering with low enough thermal budget for obtaining crystallinity of GeSn on Si having the Sn segregation effectively suppressed. The processed samples are closely investigated by various analysis tools in cooperation for confirming the crystallinity and the atomic distribution in the prepared GeSn layers.

## II. EXPERIMENTS

*p*-type Si (111) substrates were prepared by the standard cleaning including the native oxide removal by diluted hydrofluoric (DHF) acid. A 4-inch Ge target of 5N (99.999%) purity and a 4-inch GeSn target of 4N (99.99%) purity with Sn fraction of 12% were prepared for sputtering. A 300-nm-thick Ge buffer layer was deposited on the Si substrate to relax the lattice mismatch between Si and GeSn at DC powers of 30 W and 500 W. The base vacuum was $9.0 \times 10^{-6}$ Torr, the Ar flow rate was 30 sccm, the actual process pressure was 10 mTorr, and the temperature of chamber heater was maintained to be 250°C in performing the sputtering process.

After the two types of Ge buffer layers were deposited, 300-nm-thick GeSn layers were deposited on the samples at DC power of 500 W. Also, for the comparison sample, GeSn layer with the thickness of 300 nm was directly deposited on the Si substrate without a Ge buffer. Fig. 1(a) through (c) schematically shows the prepared samples. The samples were analyzed by various tools for evaluating the atomic compositions and crystallinity: X-ray spectroscopy (XPS), X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM), and electron diffraction patterns (EDPs).

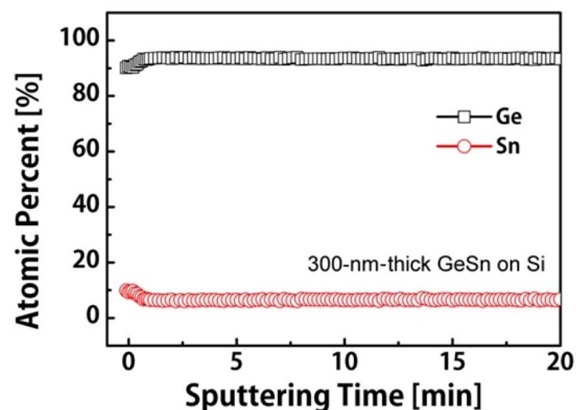


**Fig. 2.** Depth profiling of the GeSn thin film on the Si (111) substrate obtained by an XPS.

## III. RESULTS AND DISCUSSION

Fig. 2 shows the XPS depth profiling results from the GeSn thin film deposited on Si. Sn fraction was measured to be 6.51 at. % on average. The atomic weights of Ge and Sn are 72.630 g/mol and 118.710 g/mol, respectively, and Sn is 1.6 times heavier than Ge. Therefore, the number of Sn atoms which were sputtered from the thin film surface by the Ar ion bombardment and reached the Si substrate was lower than that of Ge [15-17]. Consequently, the Sn fraction at the final sample is lower than that of the original GeSn target.

However, the XPS depth profiles also reveal that Sn fraction near the surface is 3% higher than that in the bulk region. When Ge and Sn atoms are sputtered from the target, Ge atoms tend to be stabilized and settle in the film more quickly than Sn atom. This result is due to the fact that the surface energy of Sn (685 ergs/cm$^2$) is smaller than that of Ge (1,060 ergs/cm$^2$). Consequently, GeSn film has a relatively high Sn fraction ratio at the surface [18, 19]. Fig. 3 shows the XRD results obtained from Sample 1 through 3. Peaks from (111) GeSn were clearly observed from Sample 1 and Sample 2. However, there was no distinct peak from GeSn on Sample 3 where the Ge buffer layer was deposited by sputtering at a low DC power. By comparing Samples 2 and 3, it is concluded that densely prepared Ge layer substantially helps the crystallization of GeSn on top of Ge. Also, it is notable that partial crystallization of GeSn can be obtained even directly on Si by low-temperature

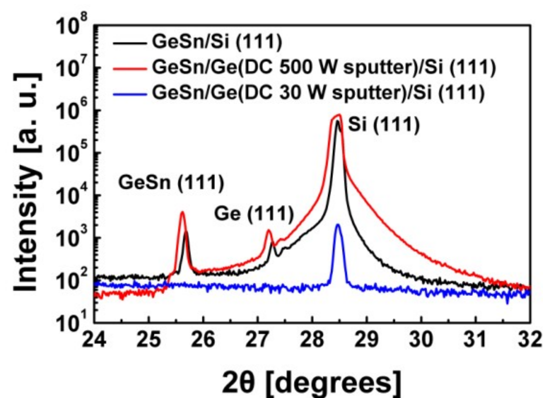


**Fig. 3.** XRD patters of the GeSn samples 1 through 3.

**Table 1.** Diffraction peak location, FWHM, and grain size converted from the experimented samples.

| Underlying Layer | GeSn (111) 2θ [°] | FWHM [°] | Grain Size [nm] |
|---|---|---|---|
| Si (111) | 25.66 | 0.12 | 67.87 |
| Ge (500W) | 25.62 | 0.18 | 45.24 |
| Ge (30 W) | - | - | - |

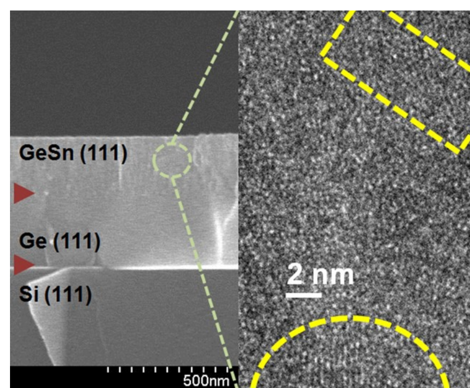


**Fig. 4.** SEM (left) and TEM (right) images showing the cross-sectional view and the poly-GeSn domains, respectively, from Sample 2.

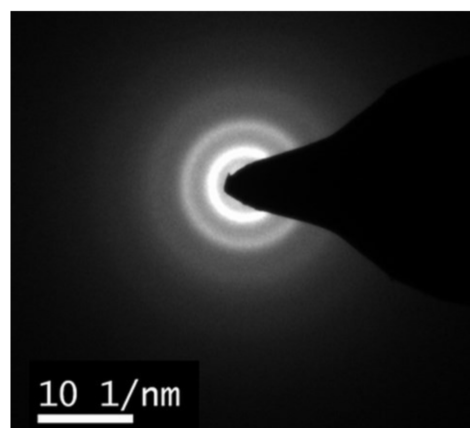


**Fig. 5.** EPDs of the GeSn films of Sample 2.

sputtering without a subsequent annealing process. Although the perfect crystalline GeSn lattices are not easily obtainable from the approach through annealing-free processing in this work and it is not suitable to implementing the light source, the poly-GeSn can be still adopted for passive optical devices such as photodetector, modulator, and resonator and for electron devices in the on-chip integrated CMOS part where the perfect crystallinity is not essentially required.

Table 1 summarizes peak locations, full-width half maximum (FWHM) values, and grain sizes obtained from the samples. The largest grain size of GeSn was observed from Sample 1. It is considered that the difference in grain size attributes to planarity of the underlying layer. In a previous report about deposition of Ge on Si by sputtering, the roughness of Ge film on top of Si decreases as the sputtering power increases. This is because higher sputtering power gives Ge atoms higher energy sufficient to move to the geometrically concave regions, which eventually helps the construction of a flat Ge film. Thus, Sample 2 with the Ge buffer layer deposited by the high DC power of 500 W has smoother surface than Sample 3 with a buffer sputtered at DC power of 30 W. Further, the perfectly flat Si surface without buffer (Sample 1) will provide more room to form the larger poly-GeSn grains. The Ge buffer layer deposited at 500-W DC magnetron power gives a higher degree of tensile strain to GeSn compared with the Ge buffer prepared by 30-W power [20], which in turn reveals that the densely deposited Ge relaxes the GeSn compressively strained by Si more effectively.

Fig. 4 shows the high-resolution transmission electron microscopy (HR-TEM) image obtained from Sample 2 along with the scanning electron microscopy (SEM) image. From the figures, it can be found that Ge (111) has been grown on Si with very fine granularity. The interface between Ge and Si appears to be distinguishable. Since the processing temperature was designed to be as low as 250°C and there was no preceded post-deposition annealing (PDA), it was rather hard to conclude that Ge was epitaxially grown on Si. However, the Ge and GeSn layers do not show a distinct interface and the GeSn layer has been smoothly grown

on Ge with a small lattice mismatch. Further, the HR-TEM image demonstrates that the GeSn layer on top has definite polycrystalline domains. Fig. 5 shows the electron diffraction patterns (EDPs) of Sample 2. Although the periodic dots are not traced due to rather weak crystallinity, the coaxially patterned bright rings are clearly observed and they are the preliminary proof for the existence of polycrystalline domains.

## IV. CONCLUSION

In this work, GeSn films were deposited on the Si substrate by using DC magnetron sputtering method. Polycrystalline GeSn thin films with a Sn fraction of 6.51% have been successfully obtained. The only process control variable was the DC sputtering power and there was no subsequent heat treatment, which was intended for designing an extremely low-thermal-budget processing with highly effective suppression of Sn segregation. GeSn grain size was affected by the surface planarity of the underlying layer and high-power-deposited Ge buffer had an effect of enlarging the grains. Furthermore, even without a buffer layer, poly-GeSn domains were obtained on the Si substrate. It is expected that DC magnetron sputtering under the optimal power condition will be a plausible processing technique with high cost-effectiveness for preparing the GeSn-on-Si platform toward integration of electronics and photonics.

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