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A Transimpedance Amplifier Employing a New DC Offset Cancellation Method for WCDMA/LTE Applications

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Abstract—**In this paper, a transimpedance amplifier based on a new DC offset cancellation (DCOC) method is proposed for WCDMA/LTE applications. The proposed method applies a sample and hold mechanism to the conventional DCOC method with a DC feedback loop. It prevents the removal of information around the DC, so it avoids signal-to-noise ratio degradation. It also reduces area and power consumption. It was designed in a 0.13 μm deep n-well CMOS technology and drew a maximum current of 1.58 mA from a 1.2 V supply voltage. It showed a transimpedance gain of 80 dBΩ, an input-referred noise current lower than 0.9 pA/√Hz, an out-of-band input-referred 3rd-order intercept point more than 9.5 dBm, and an output DC offset lower than 10 mV. Its area is 0.46 mm × 0.48 mm.**

Index Terms—**DC offset, DC feedback loop, direct-conversion receiver, LTE, sample and hold, transimpedance amplifier, WCDMA**

I. INTRODUCTION

A direct-conversion receiver (DCR) is the most competitive architecture for receiver applications, providing high integration, few bill-of-materials, reduced mixing spurs, low cost, and low power consumption. However, DC offset, which is mainly generated by the local oscillator (LO) self-mixing and device mismatches, is problematic in the DCR. The DC offset is amplified along with the desired signal, and saturates the subsequent baseband analog circuits, preventing signal detection. Therefore, the DC offset should be eliminated.

Many DC offset cancellation (DCOC) methods have been published in the literatures [1-5]. AC coupling [1], a DC feedback loop (DCFL) [2-4], and a digital storage system using digital-to-analog converters (DAC) [5] are the most popular DCOC methods. The AC coupling method requires extremely large capacitors and/or resistors for the large time constant. The DCFL method produces function of high-pass filter (HPF) and rejects DC offset by utilizing an integrator or low-pass filter (LPF) in the negative feedback loop. Both the AC coupling and DCFL methods remove the desired signal around the DC as well as DC offset, degrading the signal-to-noise ratio (SNR) as a result or have large area to reduce -3-dB frequency of the HPF [6]. The other common approach for DCOC is a digital storage system to compensate the offset current with the DAC. However, this method cannot remove dynamic DC offset and requires very high resolution to achieve excellent DCOC performance.

In this paper, a new DCFL DCOC method employing a sample and hold mechanism is proposed to avoid SNR degradation and reduce area and power consumption. To verify the proposed method, a transimpedance amplifier (TIA) adopting the DCOC method was designed for WCDMA/LTE applications. Section II describes the mechanism of the proposed DCFL DCOC method.

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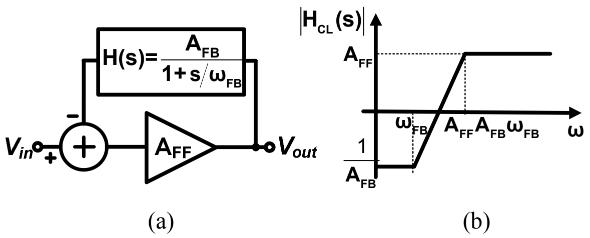

Fig. 1. (a) Block diagram, (b) frequency response of the conventional DCFL DCOC method.

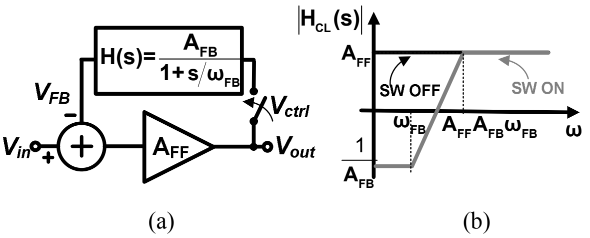

Fig. 2. (a) Conceptual block diagram, (b) frequency response of the proposed DCOC method.

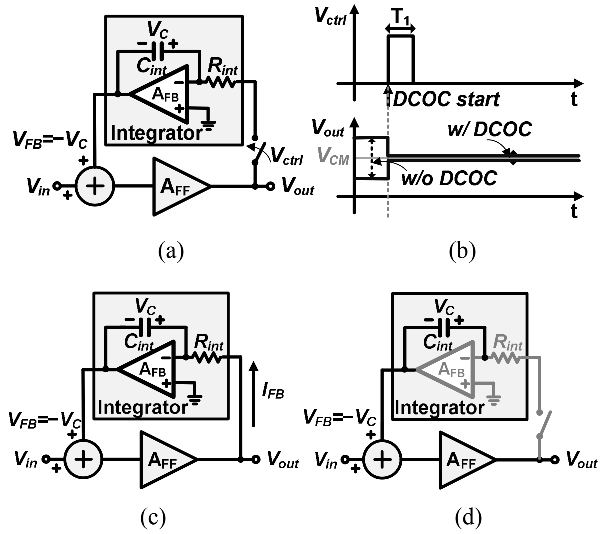

Fig. 3. (a) Detailed block diagram of the proposed DCFL DCOC method, (b) transient response of V_{ctrl} and V_{out}, (c) block diagram when DCFL is formed, (d) block diagram when DCFL is broken.

Detailed circuit designs of the TIA are presented in Section III. The post-layout simulation results are shown in Section IV. Finally, Section V concludes this paper.

II. A NEW DC OFFSET CANCELLATION METHOD

Fig. 1 shows a block diagram of the conventional DCFL DCOC method. The integrator or the LPF in the feedback path produces the HPF function in the closed-loop transfer function. The closed-loop transfer function of the amplifier with the conventional DCFL is given by

$$H_{Closed-loop}(S) = \frac{A_{FF}}{1+A_{FF}A_{FB}} \frac{1+\frac{s}{\omega_{FB}}}{1+\frac{s}{(1+A_{FF}A_{FB})\omega_{FB}}} \quad (1)$$

where $H(s)=A_{FB}/(1+s/\omega_{FB})$ and A_{FF} are the transfer function of the LPF in the feedback path and the voltage gain of the amplifier in the feed-forward path, respectively [4]. The DC gain of the closed loop transfer function and -3 dB frequency of the HPF are approximately $1/A_{FB}$ and $A_{FB}A_{FF}\omega_{FB}$, respectively. The -3 dB frequency of the HPF should be very small to avoid rejection of the desired low-frequency signal around the DC, and to avoid SNR degradation. However, the large time constant degrades transient response and increases the area.

A new DCOC method to resolve the critical drawback of the conventional DCFL method is proposed and shown in Fig. 2. The main idea of the proposed DCOC method is to form the DCFL and eliminate the DC offset for a short period, and break the DCFL to avoid SNR degradation, while the integrator or LPF in the feedback path holds the compensated voltage of V_{FB} and keeps cancelling the DC offset. That is, the proposed method adopts a sample and hold mechanism. The DCOC sequence is as follows. The receiver is powered-up, the proposed DCOC method is performed, and the desired signal is applied to baseband circuits. As a result, the amplifier with the proposed DCOC method has the frequency response shown in Fig. 2(b). For most of the time, the amplifier can avoid SNR degradation. Therefore, the proposed method does not need to have large time constant to avoid removal of the desired low-frequency signal around the DC.

Fig. 3 shows a detailed block diagram of the proposed method. The DCFL is formed by the control signal of V_{ctrl}. As shown in Fig. 3(b), the DCFL is formed in T_1 period. In DC, V_{FB} is given by

$$V_{FB} = -\frac{A_{FF}A_{FB}}{1+A_{FF}A_{FB}} V_{DCoffset,in} \quad (2)$$

Table 1. Performance comparison of the proposed method with conventional DCOC methods

Parameters	AC coupling	DCFL	Digital storage system	Proposed method
Removal of static DC offset	Yes	Yes	Yes	Yes
Removal of dynamic DC offset	Yes	Yes	No	Yes
Removal of low-frequency signal	Yes	Yes	No	No
Power consumption	None	Moderate	Small	Small
Integration level (Area)	Low (Large)	Moderate (Moderate)	High (Small)	Moderate (Moderate)

where $V_{DCoffset,in}$ is the input DC offset. C_{int} is charged by $i_{FB}=V_{DCoffset,in}A_{FF}/R_{int}$ for T_1, so V_C grows to the following value,

$$V_C = \frac{A_{FF}V_{DCoffset,in}}{R_{int}C_{int}}T_1 = A_{FF}V_{DCoffset,in}\omega_{FB}T_1 . \quad (3)$$

Because V_{FB}=-V_C, T_1 should be given by

$$T_1 = \frac{A_{FB}}{(1+A_{FF}A_{FB})\omega_{FB}} \cong \frac{1}{A_{FF}\omega_{FB}} . \quad (4)$$

The compensated output DC offset is expressed by

$$V_{DCoffset,out} = \frac{A_{FF}}{1+A_{FF}A_{FB}}V_{DCoffset,in} \cong \frac{V_{DCoffset,in}}{A_{FB}} . \quad (5)$$

After T_1, the DCFL is disconnected. Even though the DCFL is broken, C_{int} holds the charge and V_{FB} to compensate the input DC offset, while the output DC offset of $V_{DCoffset,out}$ remains cancelled. The transient response of the control signal of V_{ctrl} and output voltage of V_{out} are shown in Fig. 3(b). Table 1 compares the proposed DCOC method with conventional DCOC methods. The proposed DCOC method has lower power consumption than the conventional DCFL methods because the loop is only formed for T_1 and the loop is broken and the OPAMP in the loop is off for the rest of the time. In addition, the proposed method can remove static and dynamic DC offset without SNR degradation. It does not need to have low -3 dB frequency of the HPF and results in reducing the area.

If the proposed DCOC method is employed in the baseband circuits in the receiver, the DCOC process should be performed whenever the LO frequency is changed. This is because the DC offset at the mixer output is randomly changed whenever the LO frequency is changed.

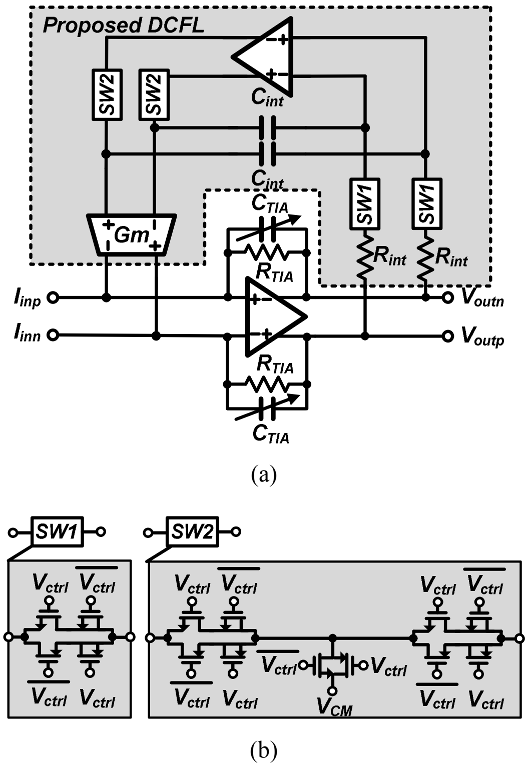

Fig. 4. (a) Schematic of the TIA with the proposed DCOC method, (b) switch networks.

III. A Transimpedance Amplifier Adopting the Proposed DCOC Method

To verify the proposed DCFL DCOC method, a TIA was designed for WCDMA/LTE applications. The TIA performs current-to-voltage conversion and attenuates undesired out-of-band blockers as the first stage of baseband analog circuits. The TIA is the most important stage for determining the DC offset of the baseband analog circuits because the preceding stage is the mixer which generates the dominant DC offset caused by LO self-mixing. In this section, a detailed circuit design of the TIA is presented, along with the proposed DCOC method shown in Fig. 4. The proposed DCOC loop is designed based on the block diagram in Fig. 3. V_{ctrl} controls the connection and disconnection of the loop. C_{int} is 30 pF and R_{int} is tunable from 400 Kohm to 1

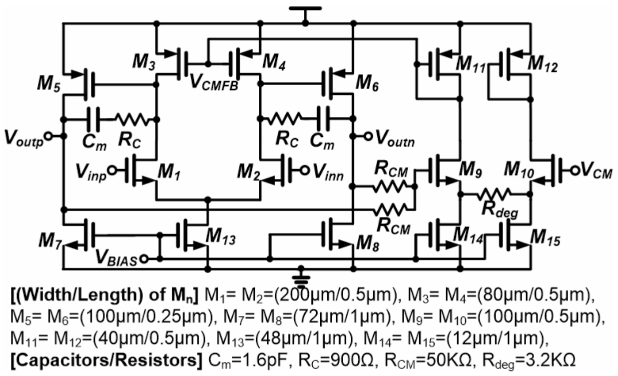

Fig. 5. Schematic of the Miller-compensated two-stage operational amplifier with common-mode feedback loop.

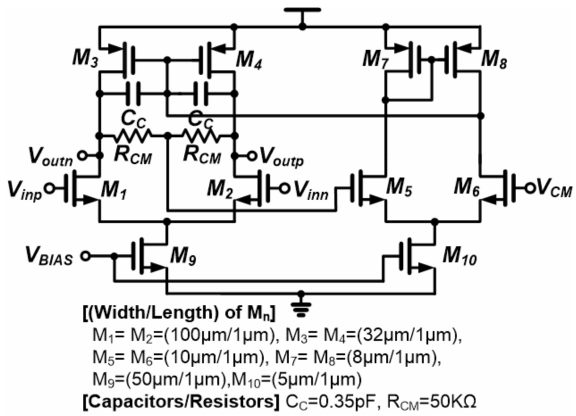

Fig. 6. Schematic of the transconductor.

Mohm.

The switch networks of SW1 and SW2 utilize transmission gates and dummy switches for clock-feedthrough cancellation as shown in Fig. 4(b) [7].

The TIA adopts an operational amplifier (OPAMP)-based architecture with negative feedback for high linearity [8]. In fact, the OPAMP of the TIA is the most critical block because it chiefly determines overall TIA performance such as input impedance, thermal/flicker noise and linearity. The conventional Miller-compensated two-stage OPAMP is used for the TIA, as shown in Fig. 5 [9]. To achieve low flicker noise performance, the OPAMP has large sized input transistors of M_1 and M_2 and load transistors of M_3 and M_4 in the first stage of the OPAMP. The output common mode voltage level of the OPAMP has to be maintained constantly. The common mode feedback (CMFB) loop of the OPAMP performs this function. The TIA has a bandwidth (BW) of 1.92 MHz for WCDMA, and 0.7 MHz, 1.5 MHz, 2.5 MHz, 5 MHz, 7.5 MHz, and 10 MHz for the LTE application, respectively. The TIA has a 5-bit capacitor array, which can be switched by a digitally controlled signal. This capacitor array will compensate variations in the process, supply voltage and temperature.

Fig. 6 presents the transconductor (Gm)-stage utilized in the DCFL [9]. It converts the output voltage of the integrator into the current to compensate the input DC offset. The Gm-stage employs the CMFB loop to set the constant output voltage.

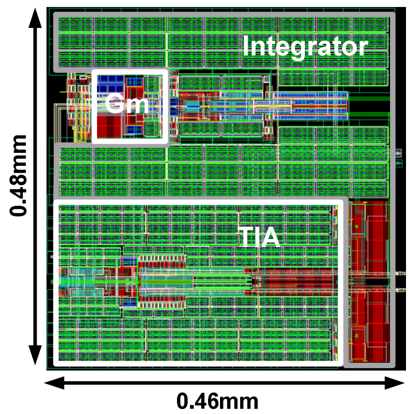

Fig. 7. Layout of the TIA with the proposed DCOC method.

IV. Simulation Results

The TIA with the proposed DCFL DCOC was designed for WCDMA/LTE applications in a 0.13 μm deep n-well CMOS process. Fig. 7 shows the layout of the proposed TIA, with an area of 0.22 mm^2. It draws a current of 1.58 mA for TIA BW of 5 MHz, 7.5 MHz and 10 MHz and 0.55 mA for the other TIA BWs from a 1.2 V supply voltage, respectively.

The Cadence Spectre-RF is used for circuit simulation. The simulated frequency response of the TIA with the proposed DCOC method is shown in Fig. 8 according to TIA BWs. When the DCFL is formed with V_{ctrl}=1, the HPF removes the DC offset and the desired signals around the DC. When the DCFL is broken with V_{ctrl}=0, the HPF function disappears, but the output DC offset remains a compensated value. Fig. 9 presents the transient response of the TIA. When the proposed DCOC is not performed, the output DC offset is more than

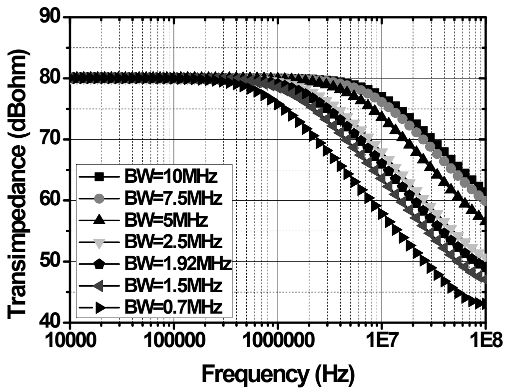

Fig. 8. Simulated frequency response of the TIA with respect to TIA BWs.

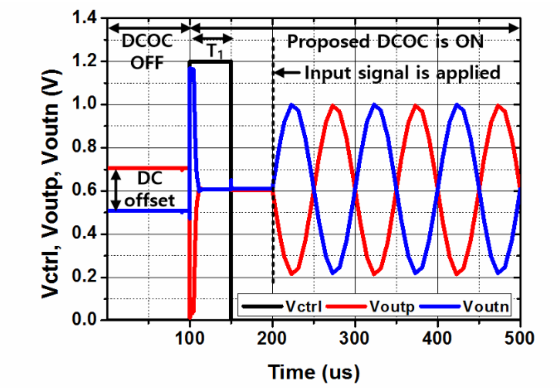

Fig. 9. Simulated transient response of the TIA with the proposed DCOC method.

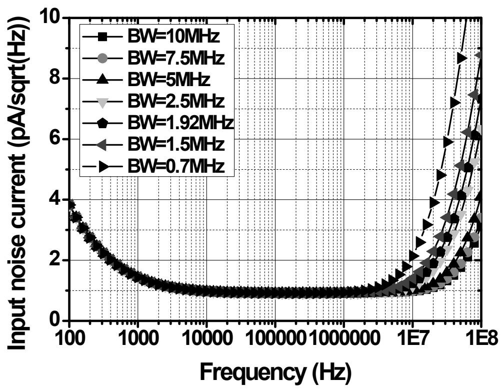

Fig. 10. Simulated input-referred noise current of the TIA.

200 mV with an input DC offset of 10 mV with the mixer output impedance of 500 ohm. When the proposed DCOC starts, the output DC offset is compensated and remains lower than 10 mV.

The simulated input-referred noise currents of the TIA with respect to TIA BWs are illustrated in Fig. 10. The minimum noise current in passband is 0.9 pA/√Hz.

Fig. 11 plots the simulated in-band (IB) and out-of-

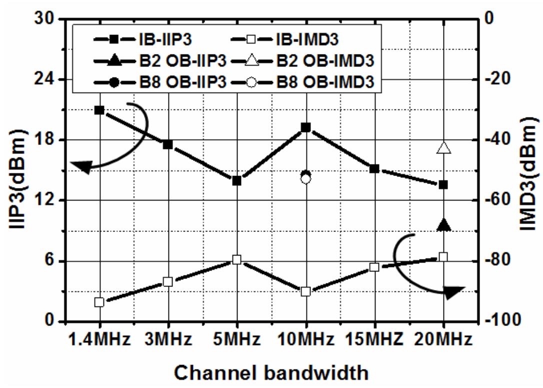

Fig. 11. Simulated IB-IIP3 and OB-IIP3 with respect to LTE CHBW.

band (OB) input-referred 3rd-order intercept point (IIP3) with respect to the LTE channel bandwidth (CHBW). The IB-IIP3 test conditions in the receiver are $f_1 = f_{LO}$ + CHBW/2 + 7.5 MHz, $f_2 = f_{LO}$ + CHBW/2 + 14 MHz and $p_1 = p_2$ = -46 dBm, respectively. If it is assumed that the voltage gain of the LNA and mixer is 20 dB, the test conditions for IB-IIP3 in the TIA with a mixer output impedance of 500 ohm are f_1 = CHBW/2 + 7.5 MHz, f_2 = CHBW/2 + 14 MHz and $p_1 = p_2$ = -26 dBm. The TIA has an IB-IIP3 of more than 13.45 dBm over all of the BWs with a mixer output impedance of 500 ohm. As shown in Fig. 11, as the LTE CHBW increases, the IB-IIP3 decreases, because the OPAMP performance is degraded at high frequency. The reason the IB-IIP3 at the LTE CHBW of 5 MHz is lower than that of 10 MHz is because the current consumption of the TIA is reduced from 1.58 mA to 0.55 mA to save power consumption. The test conditions for OB-IIP3 in the receiver are $f_1 = f_{LO} - f_{RX\text{-}TXseperation}$, $f_2 = f_{LO} - 2f_{RX\text{-}TXseperation}$ + 1 MHz, p_1 = -25 dBm, and p_2 = -60 dBm, respectively. If it is assumed that the voltage gain of the LNA and mixer is 20 dB, the test conditions for OB-IIP3 in the TIA with a mixer output impedance of 500 ohm are $f_1 = f_{RX\text{-}TXseperation}$, $f_2 = 2f_{RX\text{-}TXseperation}$ + 1 MHz, p_1 = -5 dBm, and p_2 = -40 dBm, respectively. B8 and B2 have the worst test condition in commercial LTE low band and mid-band, respectively, since TX-RX separation is the closest in each band. Fig. 11 shows that the OB-IIP3 of the TIA has more than 9.5 dBm over all of the BWs. The TIA has the minimum OB-IIP3 performance in the maximum TIA BW since the filtering effect for two input tones decreases as the TIA BW increases.

Table 2 summarizes the simulated performance of the

Table 2. Post-layout simulated performance summaries of the proposed TIA for WCDMA/LTE applications

Process	0.13 μm deep n-well CMOS technology
TIA BW [MHz] WCDMA LTE	 1.92 0.7, 1.5, 2.5, 5, 7.5, 10
Transimpedance [dBΩ]	80
Input-referred noise current[pA/√Hz]	0.9
Output DC offset [mV]	< 10
IB-IIP3/OB-IIP3 [dBm]	>13.45 / >9.5
Supply voltage [V]	1.2
Power consumption [mW] TIA BW 5 M, 7.5 M, 10 MHz TIA BW 0.7 M, 1.5 M, 1.92 M, 2.5 MHz	 1.896 0.66
Area [mm^2]	0.22

TIA with the proposed DCOC method.

V. CONCLUSIONS

A new DCFL DCOC method using a sample and hold mechanism was proposed. The main idea is verified by designing the TIA for WCDMA/LTE applications in a 0.13 μm deep n-well CMOS technology. The TIA achieved an output DC offset of lower than 10 mV without SNR degradation. It drew a maximum current of 1.58 mA from a 1.2 V supply voltage and showed a transimpedance gain of 80 dBΩ, an input-referred noise current of lower than 0.9 pA/√Hz, and an OB-IIP3 of 9.5 dBm in LTE 20MHz CHBW. Therefore, the proposed technique is expected to be suitable and effective for the DCOC method of baseband analog circuits.

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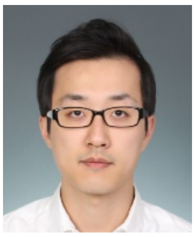

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