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A 70 MHz Temperature-Compensated On-Chip CMOS Relaxation Oscillator for Mobile Display Driver ICs

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Abstract—**A 70 MHz temperature-compensated on-chip CMOS relaxation oscillator for mobile display driver ICs is proposed to reduce frequency variations. The proposed oscillator compensates for frequency variation with respect to temperature by adjusting the bias currents to control the change in delay of comparators with temperature. A bandgap reference (BGR) is used to stabilize the bias currents with respect to temperature and supply voltages. Additional temperature compensation for the generated frequency is achieved by optimizing the resistance in the BGR after measuring the output frequency. In addition, a trimming circuit is implemented to reduce frequency variation with respect to process. The proposed relaxation oscillator is fabricated using 45 nm CMOS technology and occupies an active area of 0.15 mm^2. The measured frequency variations with respect to temperature and supply voltages are as follows: (i) ±0.23% for changes in temperature from -30 to 75°C, (ii) ±0.14% for changes in V_{DD1} from 2.2 to 2.8 V, and (iii) ±1.88% for changes in V_{DD2} from 1.05 to 1.15 V.**

Index Terms—**On-chip relaxation oscillator, temperature compensation, delay of comparator, bandgap reference, trimming circuit**

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I. INTRODUCTION

Increased demand for mobile devices with high-resolution displays is creating a need for mobile display driver ICs (MDDIs) with a high-frequency reference oscillator. The frequency of the reference oscillator is determined by the frame rate, the pixel color depth, and the number of row and column drivers for the displays, and lies in the range of tens of megahertz.

Off-chip crystal oscillators provide a stable frequency of tens of megahertz but are not suitable for MDDIs due to their cost, size, and long start-up time [1]. Several on-chip oscillators have been investigated as alternative solutions [1-3]. A relaxation oscillator with bandgap reference (BGR) generates a stable frequency using a voltage and current reference circuit [2]. However, it neglects to consider the delay of the comparator and RS-latch, thereby resulting in an inaccurate frequency of the oscillator. In [1], a voltage averaging feedback constantly maintains the oscillation frequency by adjusting the control signal but requires a long start-up time due to the feedback operation. A relaxation oscillator with a feedforward period controller in [3] achieves a short start-up time of one cycle period, which is suitable for intermittent operation systems, but generates a low frequency of 100 kHz. In addition, the feedforward period controller may increase the power dissipation needed to generate a frequency of tens of megahertz due to several power-consuming circuits, which include two comparators, an RS-F/F, and initial level generator, and a replica slew rate generator.

In this paper, an on-chip CMOS relaxation oscillator that generates a frequency of tens of megahertz for MDDIs is proposed to reduce frequency variations. The

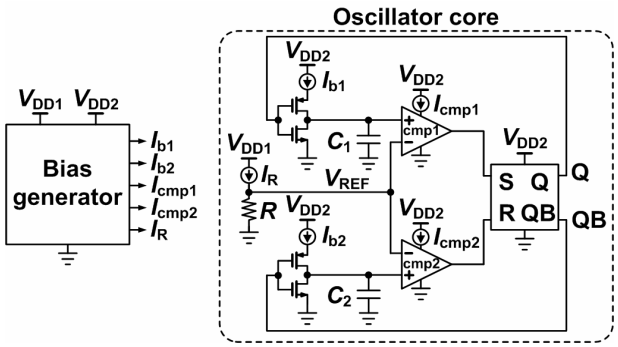


Fig. 1. Blok diagram of the proposed relaxation oscillator.

proposed oscillator compensates for frequency variation with respect to temperature by adjusting the bias currents to control the change in delay of comparators with temperature. A BGR is used to stabilize the bias currents with respect to temperature and supply voltages, and a short start-up time is accomplished by using the stable bias currents [3]. Additional temperature compensation for the generated frequency is achieved by optimizing the resistance in the BGR after measuring the output frequency. In addition, a trimming circuit is implemented to reduce frequency variation with respect to process. Section II describes the architecture and operation principles of the proposed relaxation oscillator. In section III, the experimental results are presented and compared with previous works. Finally, the conclusion is given in Section IV.

II. PROPOSED RELAXATION OSCILLATOR

Fig. 1 shows the block diagram of the proposed relaxation oscillator, which consists of a bias generator and an oscillator core, and has two different power supplies, V_{DD1} and V_{DD2}. V_{DD2} has a lower voltage level than V_{DD1} and is used to alleviate the dynamic power dissipation of the oscillator core, which is the main power-consuming block at a high oscillation frequency. Since the thin-oxide transistors with a low supply voltage, V_{DD2} of 1.1 V, are used in the oscillator core and digital circuits of the MDDI in this work, level shifters are not needed to provide the clock signals to the digital circuits. The bias generator generates stable bias currents, I_{b1}, I_{b2}, I_{cmp1}, I_{cmp2}, and I_R, with respect to temperature and supply voltages by using a BGR [4]. In [4], native NMOS transistors with a low threshold voltage are used to ensure a low input common-mode voltage of the error

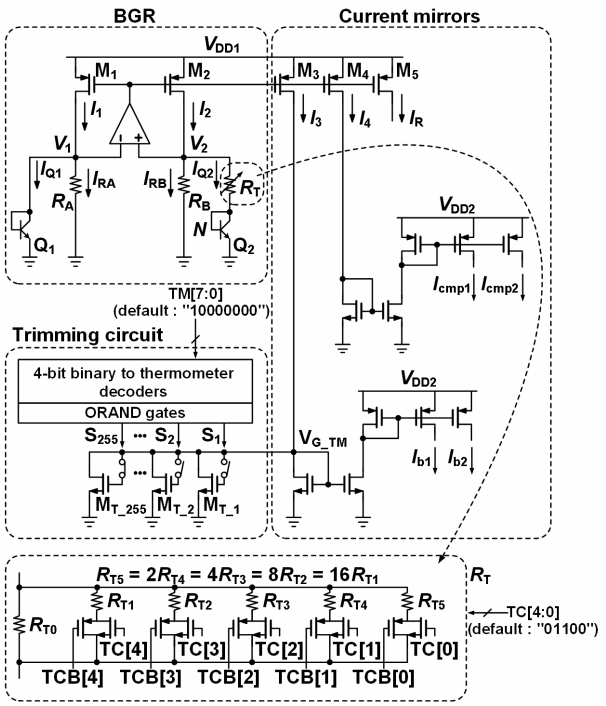


Fig. 2. Schematic of the bias generator.

amplifier, but since the native transistors are non-standard devices in CMOS technology [5], these transistors are not used in this work. Accordingly, to ensure proper operation of the error amplifier, a V_{DD1} of 2.5 V is supplied to the BGR in the bias generator, and a PMOS input stage is used for the error amplifier. In the oscillator core, the oscillation is performed by the repeated charging and discharging of two capacitors with capacitances C_1 and C_2. Assuming that I_{b1}=I_{b2}, I_{cmp1}=I_{cmp2}, and C_1=C_2, the oscillation period, T_{OSC}, is represented by

$$T_{OSC} = 2\frac{I_R \times R \times C_1}{I_{b1}} + 2t_d = 2\alpha R C_1 + 2t_d \quad (1)$$

where α and R are the current ratio of I_R to I_{b1} and the resistance in the oscillator core, respectively; t_d is the sum of delay of the comparator and RS-latch, and is mainly determined by delay of the comparator. To operate the proposed oscillator at a high oscillation frequency, α is designed to be smaller than one.

From Eq. (1), the change in T_{OSC} with temperature is expressed as follows:

$$\frac{\partial T_{OSC}}{\partial T} = 2\alpha R\frac{\partial C_1}{\partial T} + 2\alpha C_1\frac{\partial R}{\partial T} + 2\frac{\partial t_d}{\partial T}. \quad (2)$$

Accordingly, since α is temperature-independent and the changes in R and C_1 with temperature are determined by the process technology, the change in T_{OSC} with temperature can be near zero by adjusting the change in t_d with temperature to a positive or negative value. As shown in Fig. 2, the bias generator consists of current mirrors, a trimming circuit, and a BGR, which are carefully drawn using common-centroid or interdigitated techniques to reduce the device mismatches, and adjusts the bias currents, I_{cmp1} and I_{cmp2}, of the comparators to control the change in t_d with temperature. The BGR generates the reference currents, I_1 and I_2, and I_{cmp1} and I_{cmp2} are the mirrored currents of I_1 and I_2, thereby having the temperature characteristics of I_1 and I_2 multiplied by a current mirror ratio. Assuming that transistors M_1 and M_2 have the same aspect ratio and resistance R_A is equal to resistance R_B, I_1 and I_2 are expressed as

$$I_1 = I_2 = V_T \frac{\ln N}{R_T} + \frac{V_{BE}}{R_A} \tag{3}$$

where V_T is the thermal voltage; N is the emitter area ratio between Q_1 and Q_2, which are parasitic vertical NPN bipolar transistors; R_T is the resistance of an array of switchable and binary weighted resistors; and V_{BE} is the base-emitter voltage of Q_1. The derivative of Eq. (3) with respect to temperature can be given by

$$\frac{\partial I_1}{\partial T} = \frac{\partial I_2}{\partial T} = \frac{R_T \ln N \frac{\partial V_T}{\partial T} - V_T \ln N \frac{\partial R_T}{\partial T}}{R_T^2} + \frac{R_A \frac{\partial V_{BE}}{\partial T} - V_{BE} \frac{\partial R_A}{\partial T}}{R_A^2} \approx \frac{\ln N}{R_T} \frac{\partial V_T}{\partial T} + \frac{1}{R_A} \frac{\partial V_{BE}}{\partial T} \tag{4}$$

when $|\partial V_T/\partial T|$ and $|\partial V_{BE}/\partial T|$ are significantly larger than $|(V_T/R_T)(\partial R_T/\partial T)|$ and $|(V_{BE}/R_A)(\partial R_A/\partial T)|$, respectively. Since $\partial V_T/\partial T$ and $\partial V_{BE}/\partial T$ are a positive and negative value, respectively, the changes in I_1 and I_2 with temperature can be controlled by adequately adjusting $\ln N$, R_T, or R_A. In this work, R_T is selected to control the changes in I_1 and I_2 with temperature because $\ln N$ is not changed much as N increases or decreases, and R_A is assumed to be equal to R_B for generating reference currents, I_1 and I_2. Consequently, the change in t_d with temperature can be controlled by adjusting R_T, which is determined by the digital signals, TC[4:0], and the inverted signals, TCB[4:0]. When TC[4:0] is "00000", R_T becomes equal to R_{T0}, which is the maximum value of R_T. When TC[4:0] is "11111", R_T becomes equal to the parallel resistance of R_{T0}, R_{T1}, R_{T2}, R_{T3}, R_{T4}, and R_{T5}, which is the minimum value of R_T. Fig. 3 shows the simulation results of t_d normalized by t_d at a temperature of 30°C when TC[4:0] is "11111" and "00000". The simulation results for the rest of TC[4:0] are located between those at TC[4:0] of "11111" and "00000". Since R and C_1 with negative temperature coefficients are used in this work, $2\alpha R\partial C_1/\partial T$ and $2\alpha C_1\partial R/\partial T$ in Eq. (2) become negative. Accordingly, the change in t_d with temperature, $\partial t_d/\partial T$, which represents the slope of the simulation results in Fig. 3, should be positive to compensate for the change in T_{OSC} with temperature.

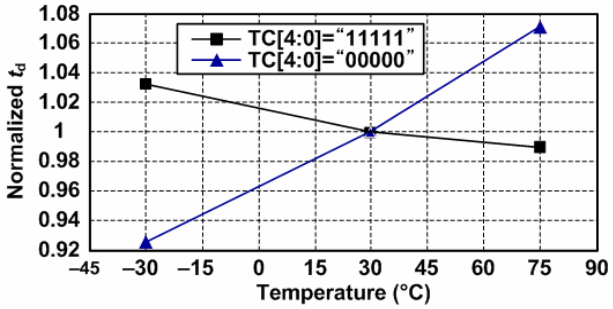


Fig. 3. Simulation results of the normalized t_d according to TC[4:0].

After the proposed oscillator is fabricated, the additional temperature compensation can be achieved by optimizing R_T with TC[4:0], where the default setting of TC[4:0] is determined by Eq. (2) and the post-layout simulation result to reduce frequency variation with respect to temperature. To optimize R_T, the output frequency of each chip is measured according to TC[4:0] and temperature, and TC[4:0], which generates the smallest frequency variation with respect to temperature, is selected. The optimized TC[4:0] is programmed to the non-volatile memory in the digital circuits of the MDDI, where the non-volatile memory is a dedicated block in a MDDI to store critical parameters such as gamma curve data and the reference voltages for analog blocks [6]. However, as R_T is changed according to TC[4:0], I_1, I_2, and α are changed, and thereby T_{OSC} is varied. In order to compensate not only for the above change in T_{OSC}, but also for frequency variation with respect to process, a decoding circuit [7] is implemented into the proposed oscillator for a trimming circuit. A trimming in [2] is

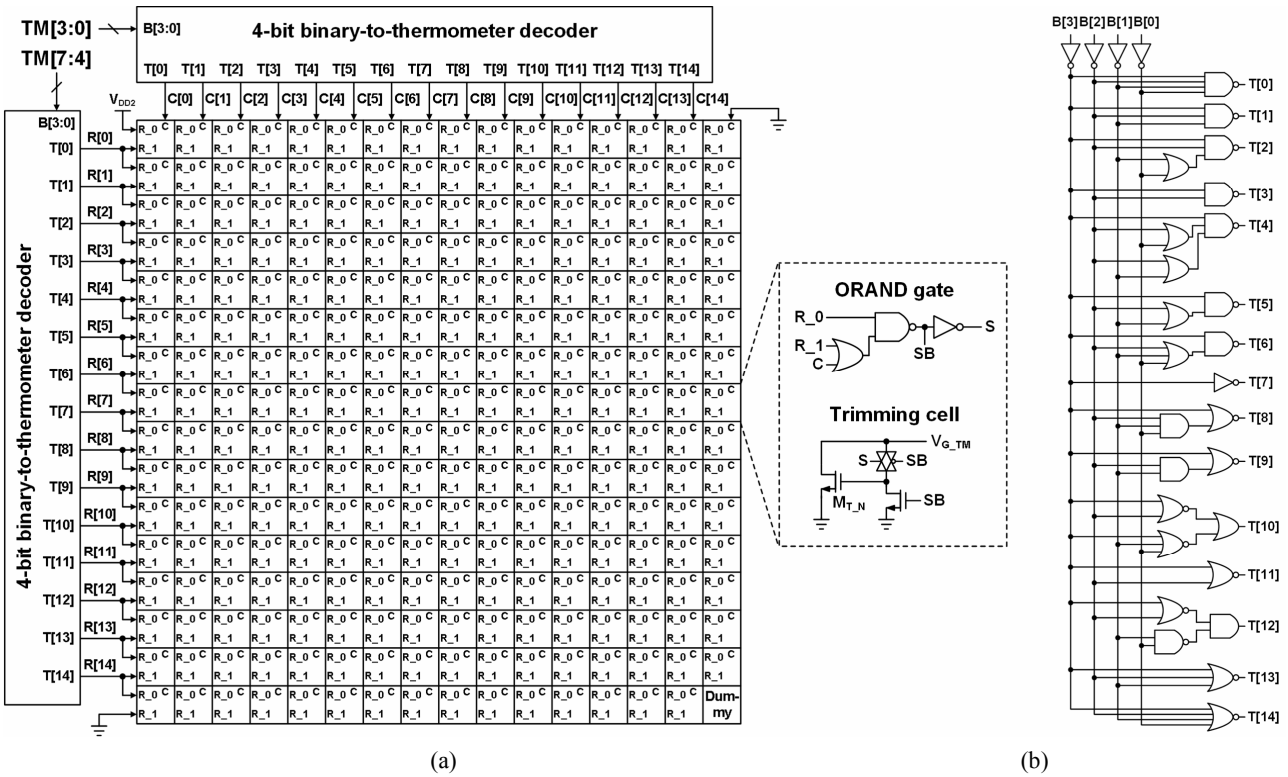


Fig. 4. (a) Block diagram of the trimming circuit, (b) schematic of 4-bit binary-to-thermometer decoder.

applied to a capacitor array, but when capacitors with small capacitances are used to generate an oscillation frequency, this method is not suitable for reducing the trimming error. The trimming error is determined by the unit capacitance of the capacitors used for trimming, and the minimum value of the unit capacitance compared with the capacitance generating an oscillation frequency is not sufficiently small enough due to the process technology. Since a small capacitance, C_1 of 0.4 pF, is used to generate the high oscillation frequency in this work, the current ratio, α, instead of the capacitance is adjusted to compensate for frequency variation with respect to process. As shown in Fig. 4(a), the trimming circuit consists of an array of ORAND gates and trimming cells and two 4-bit binary-to-thermometer decoders whose schematic is shown in Fig. 4(b). The output signals of two 4-bit binary-to-thermometer decoders, R[14:0] and C[14:0], are used for the input signals of the ORAND gates, and the trimming cells are controlled by the output signals, S and SB, of each ORAND gate. After measuring the output frequency of each chip according to TM[7:0] and comparing it with the target oscillation frequency, the optimized TM[7:0] is obtained and programmed to the non-volatile memory in

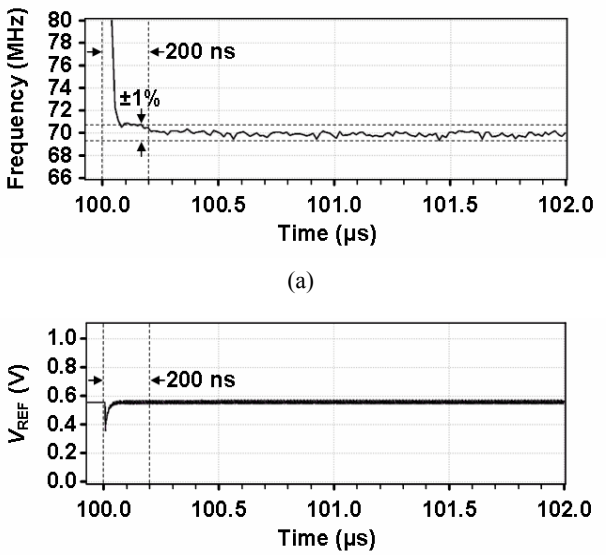
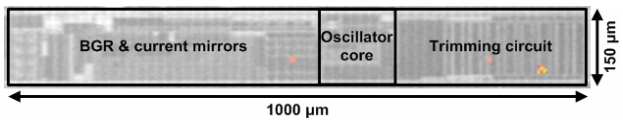
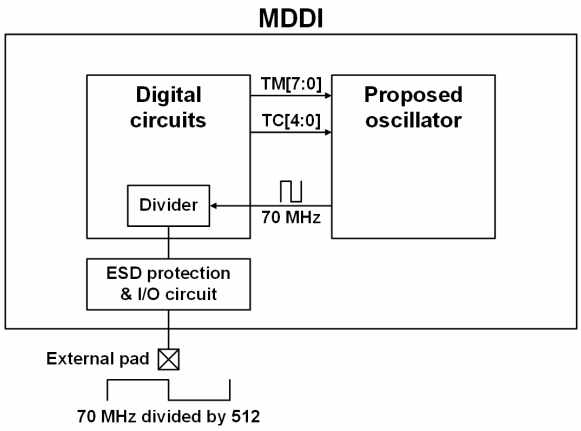


Fig. 5. (a) Simulation result of the output frequency of the proposed oscillator, (b) simulation result of V_{REF} of the proposed oscillator.

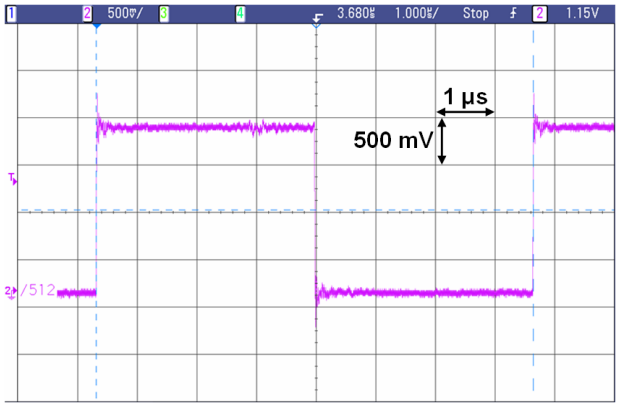
the digital circuits of the MDDI, and thereby T_{OSC} is trimmed to a desired value. In addition, the trimming circuit is designed to achieve a trimming error of less than ±0.2% after trimming at a temperature of 30°C.



(a)



(b)



(c)

Fig. 6. (a) Microphotograph of the proposed oscillator, (b) block diagram for measurement, (c) measured waveform at an oscillator frequency of 136.72 kHz.

The start-up time of the proposed oscillator is dominated by the time needed for stabilizing V_{REF}, which is mainly determined by I_R. Fig. 5(a) and (b) show the post-layout simulation results of the oscillation frequency and V_{REF}, respectively, at the slow process corner and an operating temperature of -30°C with trimming applied. Since the bias generator is turned on before the oscillator core is enabled, V_{REF} and V_{G_TM} have each settled initial value. If the low limit of operating temperature is -30°C, I_R, which is generated by the BGR in the bias generator, has the smallest value at the slow process corner and -30°C, and thereby the proposed oscillator has the slowest start-up time. The oscillation frequency in Fig. 5(a) is

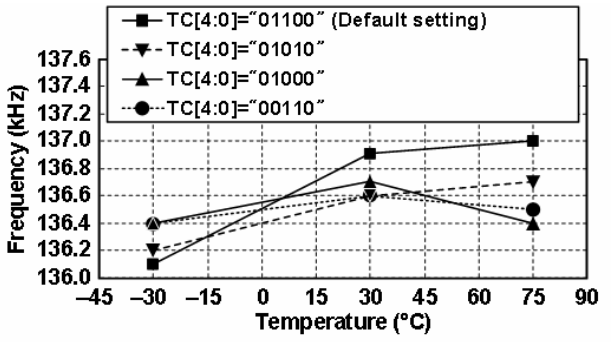
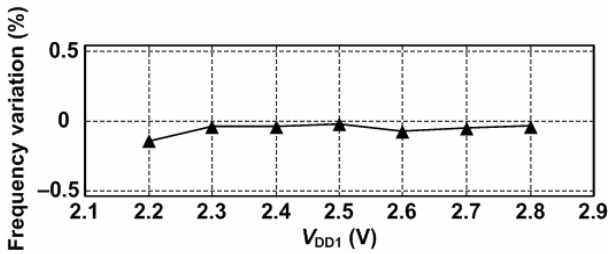
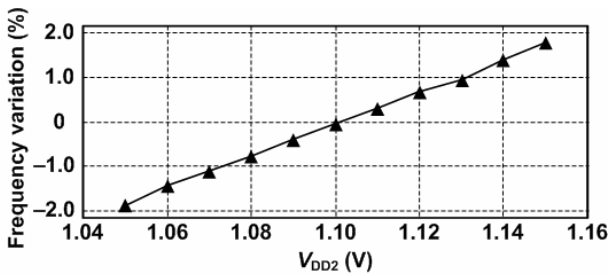


Fig. 7. Measured frequency with respect to temperature.



(a)



(b)

Fig. 8. (a) Measured frequency variation with respect to V_{DD1}, (b) measured frequency variation with respect to V_{DD2}.

stabilized within ±1% before 100.2 μs when the oscillator core is enabled at 100 μs.

III. Experimental Results

Fig. 6(a) shows a microphotograph of the proposed oscillator, which is fabricated using 45 nm CMOS technology and occupies an active area of 0.15 mm^2. Capacitors with capacitance C_1 and C_2 and resistors with resistance R, R_A, R_B, and R_T are implemented using metal-oxide-metal capacitors and high sheet-resistance poly resistors, respectively, and Q_1 and Q_2 are made of parasitic vertical NPN bipolar transistors. As shown in Fig. 6(b), the proposed oscillator is included as part of the MDDI for the measurement. The digital circuits in the MDDI, which include a timing controller, circuits for

Table 1. Performance comparison

	[1]	[2]	[3]	[8]	[9]	This Work
Technology	0.18 μm CMOS	0.5 μm CMOS	90 nm CMOS	0.18 μm CMOS	65 nm CMOS	45 nm CMOS
Area (mm^2)	0.04	0.19	0.12	0.22	0.11	0.15
Start-up Time (μs)	10*	10	10	N.A.	N.A.	0.2*
Frequency (MHz)	14	21.4	0.1	10	0.1	70
Power (μW)	45	400	0.28	80	41	757.6
FoM (μW/MHz)	3.2	18.69	2.8	8	410	10.82
Variation with Temperature (%)	±0.19 @-40-125°C	±2.5 @-40-125°C	±0.68 @-40-90°C	±0.4 @-20-100°C	±1.1 @-22-85°C	±0.23 @-30-75°C
Variation with Supply Voltage (%)	±0.16 @1.7-1.9V	±0.8 @3-5.5V	±0.82 @0.725-0.9V	±0.05 @1.2-3V	±0.1 @1.12-1.39V	±0.14 @2.2-2.8V (V_{DD1}) ±1.88 @1.05-1.15V (V_{DD2})

* Simulation result

image processing, and a non-volatile memory, are used as a divider for measuring the output frequency of the proposed oscillator and as a buffer for transferring TM[7:0] and TC[4:0] stored in the non-volatile memory to the proposed oscillator. The output frequency is measured at the external pad through a divider in the digital circuits, an ESD protection circuit, and an I/O circuit with a supply voltage of 1.8 V. Fig. 6(c) shows the measured waveform at an oscillation frequency of 136.72 kHz, which is equal to the target oscillation frequency of 70 MHz divided by 512.

Fig. 7 shows the measurement results of the output frequency with respect to temperature with a V_{DD1} of 2.5 V and a V_{DD2} of 1.1 V. The measured frequency variation at the default setting, TC[4:0] of "01100", is ±0.45% for changes in temperature from -30 to 75°C, where the operating temperature range and the measured results are well suited for MDDIs. Additional compensation, which optimizes R_T at TC[4:0] of "01000" or "00110", reduces the frequency variation to ±0.23%. The output frequency is trimmed at 30°C, and the calculated trimming error with TC[4:0] of "01000" is -0.02% at a frequency of 136.72 kHz. Fig. 8(a) and (b) show the measurement results of the frequency variations with respect to V_{DD1} and V_{DD2}, respectively. The measured frequency variations are ±0.14% for changes in V_{DD1} from 2.2 to 2.8 V and ±1.88% for changes in V_{DD2} from 1.05 to 1.15 V. The current consumptions are 98 μA for a V_{DD1} of 2.5 V and 466 μA for a V_{DD2} of 1.1 V. The total power consumption is 757.6 μW, and the calculated figure of merit (FOM), which is defined as the ratio of power consumption to oscillation frequency, is 10.82 μW/MHz.

Table 1 shows the performance summary of the proposed oscillator compared with previous works in [1-3, 8, 9]. This comparison shows that the proposed oscillator operates at the highest frequency and achieves the shortest start-up time, but consumes large power due to large bias currents needed for high-frequency operation. In addition, its frequency variations with respect to temperature and supply voltages are comparable to those of previous works.

IV. CONCLUSIONS

An on-chip CMOS relaxation oscillator for MDDIs is proposed to reduce frequency variations due to process, voltage, and temperature variations. The frequency variations are compensated for by using a trimming circuit and BGR, and adjusting the bias currents to control the change in delay of comparators with temperature. Compared with previous works, the proposed oscillator operates at the highest frequency and achieves the shortest start-up time, and its frequency variations with temperature and supply voltages are comparable. Therefore, the proposed oscillator is suitable for the generation of on-chip clocks in MDDIs for high-resolution displays, which require a stable frequency of tens of megahertz and a short start-up time.

ACKNOWLEDGMENTS

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