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A Flyback-Assisted Single-Sourced Photovoltaic Power Conditioning System Using an Asymmetric Cascaded Multilevel Inverter

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Abstract

This paper proposes a power conditioning system (PCS) for distributed photovoltaic (PV) applications using an asymmetric cascaded multilevel inverter with a single PV source. One of the main disadvantages of the cascaded multilevel inverters in PV systems is the requirement of multiple isolated DC sources. Using multiple PV strings leads to a compromise in either the voltage balance of individual H-bridge cells or the maximum power point tracking (MPPT) operation due to localized variations in atmospheric conditions. The proposed PCS uses a single PV source with a flyback DC-DC converter to facilitate a reduction of the required DC sources and to maintain the voltage balance during MPPT operation. The flyback converter is used to provide input for low-voltage H-bridge cells which processes only 20% of the total power. This helps to minimize the losses occurring in the proposed PCS. Furthermore, transient analyses and controller design for the proposed PCS in both the stand-alone mode and the grid-connection mode are presented. The feasibility of the proposed PCS and its control scheme have been tested using a 1kW hardware prototype and the obtained results are presented.

Key words: Asymmetric cascaded multilevel inverter, Flyback converter, H-bridge cell, Isolated DC sources, Photovoltaic applications.

I. INTRODUCTION

Small-scale distributed energy resource (DER) systems using photovoltaic (PV) sources for domestic and utility purposes have seen a drastic increase of interest in the literature coupled with an increase in market share [1]-[8]. Since the efficiency of PV panels is somewhere between 15-25%, which is relatively low compared to other conventional sources, the emphasis of a lot of research is related to the power conditioning systems (PCS) handling of the power produced by PV panels [9]-[11]. Traditionally, photovoltaic systems connected to the grid have three different configurations: centralized, string and module-integrated topologies. Centralized and string topologies are generally used in large and medium-scale PV systems, respectively. In the case of small-scale PV systems, module-integrated topologies are preferred due to their modularity and optimal maximum power point tracking (MPPT) capability even under partial shading conditions compared to other topologies. In the case of module-integrated topology losses, the voltage stress on switches, size, output quality and efficiency have become focal points of interest in research. In this paper, a novel PCS for small-scale PV systems using an asymmetric cascaded multi-level inverter with a single source is presented.

Traditionally, multi-level inverters were confined to high-power industrial applications [12]-[14]. However, the recent trend optimization in PV systems has been shown to be the implementation of PCS using multi-level inverters [15]-[17]. Among the various MLI topologies, the cascaded H-Bridge (CHB) topology has been preferred in PV systems due to its simplicity and ease of integration with PV systems [18], [19]. In CHB topologies, several H-Bridge cells are connected in series to provide an enhanced output from a low input voltage. These topologies effectively help in the elimination of the step-up DC-DC converters used in module-integrated PV PCS. In addition, the staircase output from CHB multi-level inverters improves the output quality and helps in reducing

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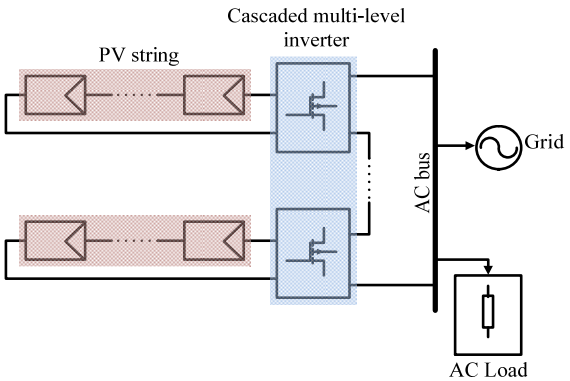


Fig. 1. Block diagram of the conventional PV PCS scheme using CHB multi-level inverter.

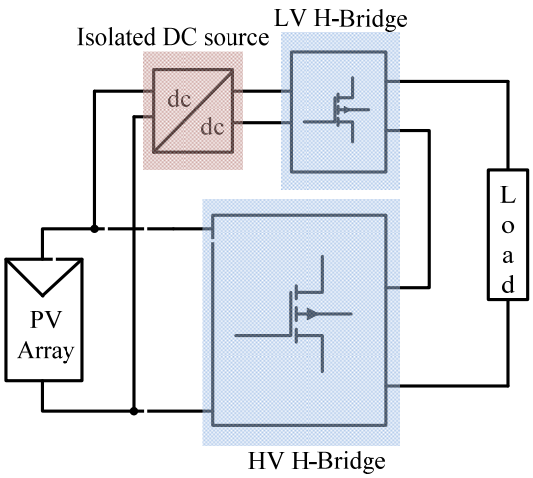


Fig. 2. Block diagram of the proposed single-source PV PCS.

the filters which are present in the load-side. However, one of the main disadvantages of CHB topologies is the requirement for some individual isolated PV sources for each of the H-bridge cells, which leads to voltage unbalancing during MPPT operation.

Previous implementations of CHBs in PV systems employed multi-string topologies as the source for individual H-Bridge cells [20]-[21]. In these methods, the MPPT scheme requires some separate sensors for individual PV strings and increases the size and cost of the PCS. Hence, it is preferable for multi-level inverter based PV PCS to reduce the number of PV strings to counter the voltage imbalance and to reduce the number of sensors.

Localized changes in the insolation and temperature due to the partial shading phenomenon results in variations in the MPP voltage among the PV strings. This sacrifices the voltage balancing between the H-bridge cells, since the MPP algorithm individually determines the input voltage output of the PV strings. This imbalance in CHB inverter outputs is not desirable, since it degrades the quality of the staircase output which is one of the main attributes of CHB inverters. A block diagram of the conventional CHB-based PV PCS is shown in Fig. 1. The number of PV strings should match the number of voltage levels. In this paper, a new multi-level inverter PCS using a single PV-string fed topology is proposed, which eliminates the imbalance during individual MPPT operations.

Previously, symmetric CHB inverters with a single DC-source for motor drive applications have been discussed in [22]-[24]. Transformers with multiple outputs operating at a high frequency have been a reasonable approach in motor drive applications. However, a similar approach is not suitable for small-scale PV systems since the high number of H-bridge cells and their corresponding transformers increases the size and cost of the PV PCS. Hence, an asymmetric CHB multi-level inverter is chosen for the proposed PCS because it provides a higher number of voltage levels with a relatively smaller number of H-bridge cells compared to symmetric CHB multi-level inverters.

In this paper, a 7-level asymmetric CHB PV PCS fed by an individual PV source is proposed. Instead of using the distributed MPPT PV modules as individual sources for each of the high-frequency H-bridge cells, a flyback converter is used to provide an auxiliary input for the low-voltage (LV) upper H-bridge cell as shown in Fig. 2. The asymmetric CHB inverter includes two H-bridge cells with varying voltage levels and operates under different switching frequencies. The high-voltage H-bridge cell operates under a fundamental switching frequency of the output for around 80% of the total power process, which ensures a high efficiency for the entire system. The flyback converter and LV H-bridge operates under a high switching frequency. However, only 20% of the power is processed by the stage, thereby assuring a high efficiency of the combined PCS compared to the conventional single 2-level H-bridge systems. In addition, the low-power transformer required by the flyback converter is considerably smaller in size compared to the high inductance of the filter required by conventional 2-level inverters. However, it brings additional complexity of the controller design due to the different input voltage levels, which complicates the PV PCS organization. Therefore, a transient analysis of the PCS to derive the small-signal model has been presented and verified using a numerical model in PSIM. In this paper, PI controllers have been employed based on the small-signal model under both the stand-alone and grid-connected operations. They have also been tested using a 1kW hardware prototype.

II. Operating Principle

The proposed single-source PV PCS consists of two converter stages namely: the flyback converter and the asymmetric CHB inverter. The complete circuit diagram of the PCS under the stand-alone mode is depicted in Fig. 3. The PCS operates under the stand-alone mode thereby providing power to domestic AC loads when a fault occurs in the grid.

A. Multilevel Inverter Modulation

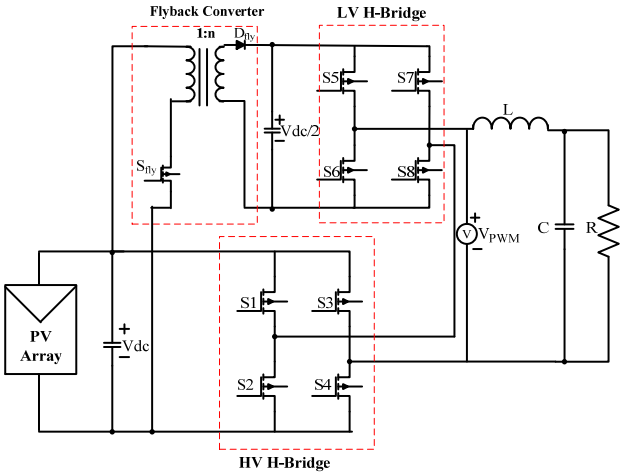


Fig. 3. Circuit figure of the proposed photovoltaic power conditioning systems with a standalone resistive load.

There are two different groups of cascaded multilevel inverters namely: the symmetric and asymmetric inverters. In conventional symmetric CHB MLI, the voltage levels of the isolated DC sources are equal. Meanwhile, in asymmetric inverters, the sources are not equally distributed. Although symmetric multilevel inverters have the advantage of a simple controller, asymmetric multilevel inverters can produce a higher number of voltage levels with the same number of H-bridge modules [25]. In the case of symmetric multilevel inverters, the number of voltage levels obtained with a given N number of H-bridge modules is given by:

$$L=2N+1. \quad (1)$$

Whereas, the number of voltage levels of asymmetric multilevel inverters is given by:

$$L=2^{N+1}-1. \quad (2)$$

Since this paper focuses on reducing the required number of isolated DC sources for a specific number of voltage levels, the asymmetric multilevel inverter is desirable for this work. A conventional discontinuous PWM strategy has been used to produce the 7-level output voltage [26]. Under this modulation strategy, the high-voltage (HV) main H-bridge inverter operates in the fundamental frequency of the output, whereas the low-voltage (LV) upper H-bridge operates with high frequency switching. Fig. 4 shows the reference and output waveforms of individual H-bridge cells as well as the combined 7-level output waveform during a single cycle. The HV H-bridge cell is modulated using a reference sine waveform with a maximum magnitude of $3/2V_{DC}$. During the positive (and negative) half-cycle, the main H-bridge turns ON to produce V_{DC} when the reference > $V_{DC}/2$, and turns OFF to produce 0V in other cases. The low-voltage H-bridge cell is modulated in a 3–level. The LV H-bridge reference is produced by the difference between the main H-bridge output and the full magnitude reference.

In this paper, the DC-link voltage for the base HV H-bridge is twice the LV H-bridge voltage. The HV H-bridge processes 80% of the output power while the remaining 20% is processed by the LV H-bridge. Thus, most of the main power goes through the low-frequency base H-bridge inverter, which experiences negligible power-processing losses. The switching devices in both of the H-bridge cells experience different levels of voltage stress and operate under different frequencies. Ideally, MOSFETs with a low conduction resistance $R_{ds,ON}$ are preferred for the HV stage compared to IGBTs. This is due to the fact that MOSFETs provide a low conduction loss for a specified current in this PCS.

B. Flyback Converter

One of the main requirements for designing the auxiliary PV-bridge interfacing converter in this architecture is to provide a galvanic isolation between the PV source and the LV H-bridge with a reasonable cost and size. As a feasible solution, a flyback converter is applied. It provides isolation and an energy transfer with a small part count. In addition to the isolation, the flyback converter regulates tightly the DC-link voltage to the LV H-bridge. For the MPPT operation of the PV source, the DC-links of both the HV and LV H-bridges should be perturbed periodically. Even under a step-change of the HV DC-link, the LV DC-link should accurately track half of the HV DC-link. Otherwise, unbalancing between the H-bridge DC-link voltages affects the quality of the inverter output waveform. Hence, the instantaneous balance in the inverter-input voltage should be guaranteed by regulation of the flyback converter output. In addition, due to the low part count in the flyback converter, it ensures cost competiveness and high reliability which contributes to extensive usage in the commercial product market [27]-[31]. Therefore, in this paper, an asymmetric MLI is combined with a flyback converter to provide a cost effective solution for single-source MLI based PV systems.

The transformer in the flyback converter stores energy when the switch is turned ON and delivers power to the load when the switch is turned OFF. Hence, the leakage inductance of the transformer should be kept at a minimum to avoid a loss of energy in heat dissipation. The value of the magnetizing inductance of the transformer determines the peak value of the ripple current and the position of the RHP zero. Hence, the design of the transformer affects the size, losses and closed-loop bandwidth of the controller. Since there is an output voltage closed loop present in the flyback converter of the PCS, the design process can be made flexible to operate the converter in both the CCM and DCM operating modes. It is also advisable to choose a critical region that is close to the full-load since the flyback converter is most efficient near the zero-crossing region. This ensures higher efficiency in the higher-power operating regions. This condition also ensures that the magnetizing inductance is not very large to make the transformer size small and to reduce the conduction losses. The critical load for the flyback converter was chosen to be 160W. As a result, during full-

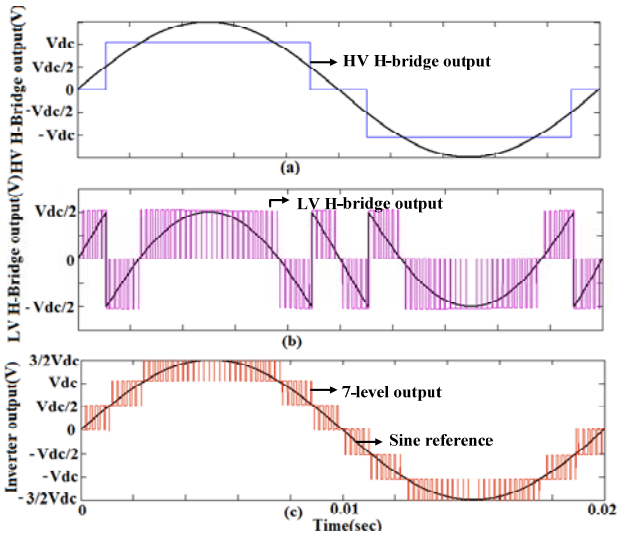


Fig. 4. Reference and output waveforms for (a) HV H-bridge, (b) LV H-bridge, and (c) Inverter output waveform.

load operation at 200W the converter is operated above the zero-crossing region in the CCM. Then the following is obtained:

$$R_{crit} = 2n^2 \frac{L_m}{(1-D)^2 T_s} \quad (3)$$

The switching frequency is chosen as 50kHz. Then L_m= 625μH.

The output capacitor provides the function of smoothing the voltage ripple for the dc-link of the LV H-bridge cell. Then the following is obtained:

$$\Delta \frac{1}{2} V_{dc} = \frac{1}{C} \frac{\frac{1}{2} V_{dc}}{R} DT_s \quad (4)$$

Since the output capacitance should also eliminate the ripple from the LV H-bridge, a large value of 2200μF is chosen.

C. *Evaluation of the Leakage Current*

A circuit diagram of the PV PCS is shown in Fig.3. It can be seen that there is galvanic isolation present between the LV H-bridge and the PV array due to the presence of the flyback converter. However, there is no galvanic isolation present between the HV H-bridge and the PV array. Hence, there is a leakage current flow in the circuit due to the presence of a stray capacitance between the PV panel and the ground. This provides a path for the leakage current flow. The stray capacitance values vary depending on the atmospheric conditions (high as 200nF/kW during damp conditions) and the material of the PV panel (100nF/kW for crystalline silicone cells and 1μF/kW in case of thin-film cells). There is a limitation of 300mA for the leakage current flow based on the German VDE0126-1-1 standard. Fig.5 shows a circuit diagram with the stray capacitance added to the PV array and the HV H-bridge cell to calculate the leakage current flow.

The HV H-bridge cell is operated under the unipolar

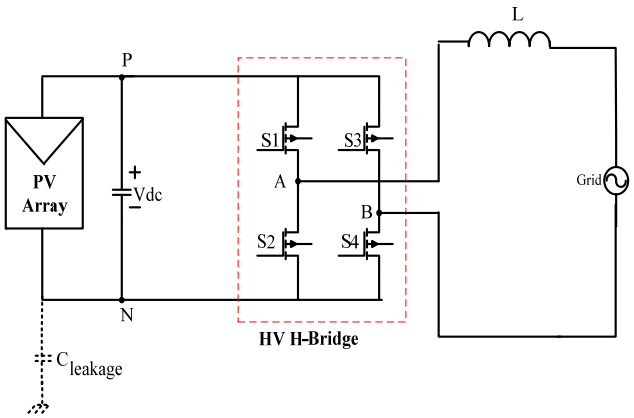


Fig. 5. PV array with stray capacitance ($C_{leakage}$) and HV H-bridge in the PV PCS.

switching operation (0 to V_{dc} to 0 to $-V_{dc}$ to 0) under the grid frequency. The leakage current can be calculated from the common-mode voltage (V_{cm}) as follows:

$$V_{cm} = (V_{AN} + V_{BN})/2 = V_{dc}/2 \quad (5)$$

$$i_{leakage} = C_{leakage} \frac{dV_{cm}}{dt} \quad (6)$$

From (6), it can be seen that the leakage can be eliminated by keeping the common-mode voltage at a constant value. In the case of unipolar switching, the common-mode voltage drops to zero from V_{dc} /2 during the freewheeling mode. Hence, there is leakage current flow in the circuit. However, in the case of the 7-level asymmetric inverter used in the PCS, the HV H-bridge operates under the grid-frequency switching, not the high-frequency switching. In addition, the magnitude of the common mode voltage is 1/3rd of the total dc-link voltage ($V_{total\ dc\text{-}link}$ =3/2 V_{dc}) instead of 1/2 of the dc-link voltage as in single H-bridge inverters. These two features combined yield very little leakage current and EMI in the circuit. Hence, the 7-level asymmetric inverter combined with a flyback converter, as proposed in the PV PCS, is suited for transformerless operation. Modified H-bridge topologies like H5 inverter, REFU inverter and HERIC inverter have been suggested for transformerless PV applications due to their common-mode voltage varying under the grid frequency, which results in little leakage current and EMI.

III. Dynamic Characteristics Analysis under Standalone and Grid-connected Modes

For the proposed asymmetric multilevel inverter, there are four operating modes, depending on the voltage levels. The switching states to obtain the different voltage levels are shown in Table I [32]. Fig. 6 illustrates the current flow path based on the switching operation under a couple of different voltage levels. The state equations of the asymmetric multilevel inverter under the stand-alone mode of operation are given below [32]:

TABLE I
SWITCHING STATES UNDER DIFFERENT MODES OF OPERATION

Mode	VPWM	S1	S2	S3	S4	S5	S6	S7	S8
1	0	0	1	0	1	0	1	0	1
2	$V_{dc}/2$	0	1	0	1	1	0	0	1
3	V_{dc}	1	0	0	1	0	1	0	1
4	$3/2V_{dc}$	1	0	0	1	1	0	0	1

$$L\frac{di_L}{dt} = -v_o \ , \quad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 1)}$$

$$L\frac{di_L}{dt} = \frac{1}{2}v_{DC} - v_o \ , \ C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 2)}$$

$$L\frac{di_L}{dt} = v_{DC} - v_o \ , \quad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 3)}$$

$$L\frac{di_L}{dt} = \frac{3}{2}v_{DC} - v_o \ , \quad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 4)}$$

Then, the transfer functions for the control-to-output (G_{vd}) and control-to-inductor current (G_{id}) are derived as:

$$G_{vd} = \frac{\widehat{v_o}}{\widehat{d}} = \frac{V_{DC}}{2+2\frac{sL}{R_o}+2s^2LC} \qquad (7)$$

$$G_{id} = \frac{\widehat{i_L}}{\widehat{d}} = \frac{\frac{1}{2}V_{DC}(sR_oC+1)}{R_o+sL+s^2LCR_o} \ . \qquad (8)$$

The derived transfer functions are verified by comparing the bode plots of the derived averaged model in MATLAB with those of the exact PWM-switching model using PSIM as shown in Fig. 7. From this figure, it can be seen that the average model from the small-signal modeling agrees with the exact PWM-switching model from the PSIM simulation.

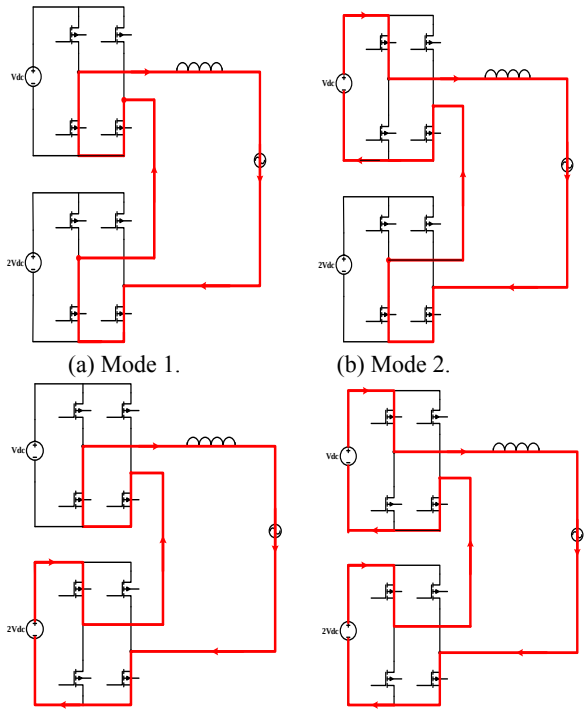
A. Stand-Alone Operation

The power conditioning control strategy is implemented with a two-loop digital PI controller for the H-bridge inverter part. A simplified block diagram of the control scheme is shown in Fig. 8 [32]. The designed controller was built and tested in PSIM software, and the result for a step-response of 50% load current is shown in Fig. 9. It can be seen that the load voltage is able to track the reference quickly and accurately even after a step change in the load. It can also be seen that the voltage balance is maintained ensuring the waveform quality.

Another part of the controller for the flyback converter consists of a single voltage-loop to maintain the DC-link voltage balance. The control-to-output transfer function derived for the flyback converter is shown in equation (10). The derived transfer function can be validated by comparing it with an exact model of the PSIM plot as shown in Fig. 10.

$$G_{vd} = \frac{\widehat{V_{DC}}}{\widehat{d}} = \frac{\frac{D'(V_{pv}+\frac{V_{DC}}{n}-IR_{pv})}{n(sL+DR_{pv})}\frac{I}{n}}{\frac{1}{R}+sC+\frac{D'}{n(sL+DR_{pv})}} \qquad (10)$$

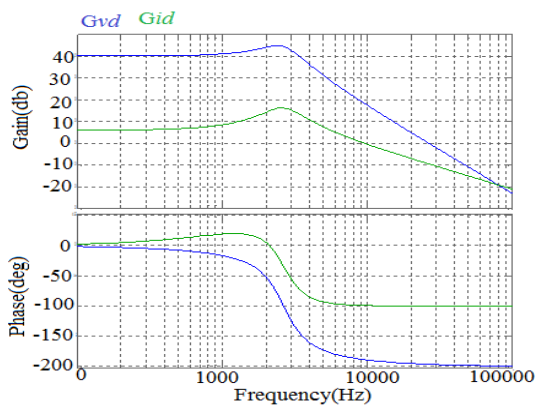
From the transfer function, it is evident that the presence of the RHP zero makes controller design with a high-frequency bandwidth a complicated process. Since the primary purpose of the flyback voltage loop is to track the variance in the base PV voltage during MPPT-voltage step changes corresponding to external weather condition, a flyback controller with a low



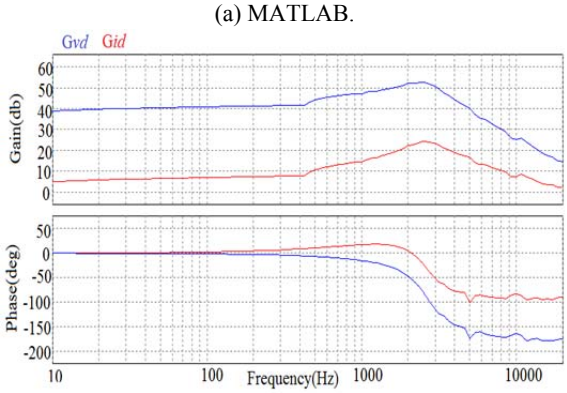
(a) Mode 1. (b) Mode 2.

(c) Mode 3. (d) Mode 4.

Fig. 6. Current flow based on the output voltage levels (a) Mode 1 (Vo=0), (b) Mode 2 ($V_o=V_{DC}/2$), (c) Mode 3 ($V_o=V_{DC}$), (d) Mode 4 ($V_o=3V_{DC}/2$).



(a) MATLAB.



(b) PSIM.

Fig. 7. Frequency responses of G_{vd} and G_{id} (a) Derived transfer function, (b) Exact switching model.

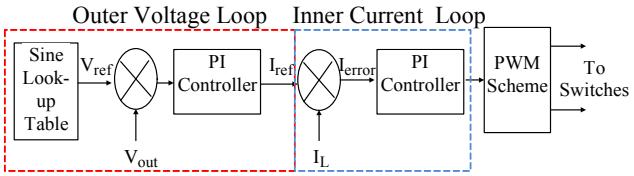


Fig. 8. Block diagram for the two-loop controller for H-bridge.

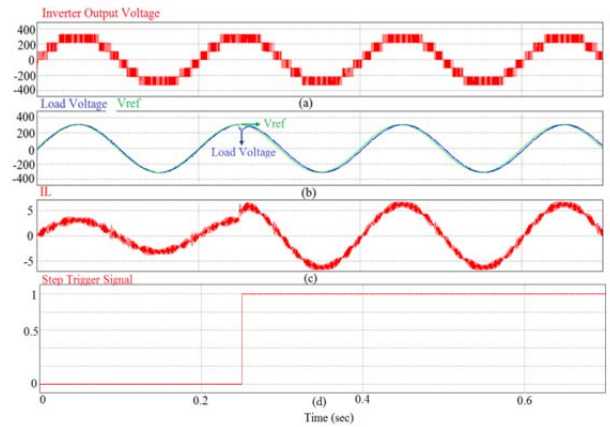
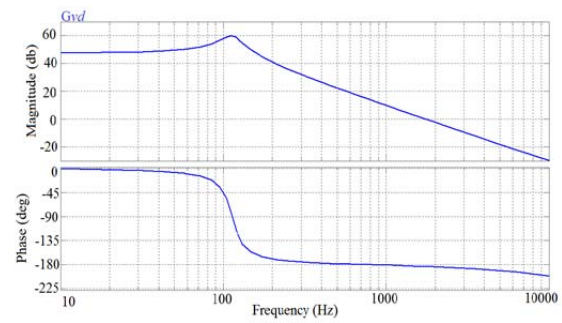
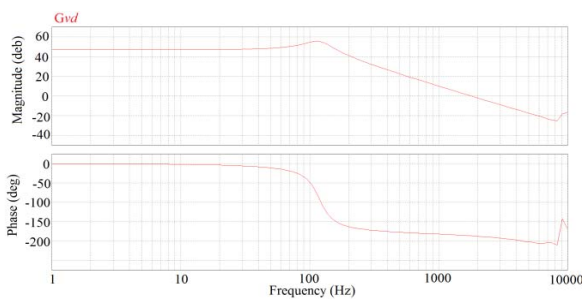


Fig. 9. Step response result in PSIM (a) Inverter output, (b) Load reference and feedback, (c) Inductor current, and (d) Step trigger signal.



(a) MATLAB plot.



(b) PSIM plot.

Fig. 10. Bode plots of G_{vd} (a) Derived transfer function, and (b) Exact PWM-switching model.

bandwidth is sufficient in this paper.

B. Grid-Connection Operation

The control scheme for the proposed PCS under the grid-connected condition is shown in Fig. 11. The PV voltage and current parameters are sensed to implement the MPPT using a perturb-and-observe (P&O) algorithm. Advanced control schemes for tracking the MPP in PV PCS with a line connection have been discussed [33]. The P&O technique assures a relatively high MPPT efficiency if there are no errors in the measurement process. The MPPT algorithm provides a reference for the PI controller of PV voltage loop. The phase lock loop (PLL) also provides phase information from the grid. The reference for the grid current controller is obtained by multiplying the outputs of the voltage loop with the PLL. The proposed controller scheme was tested in simulation for validation. The results are shown in Fig. 12 and Fig. 13. From Fig. 12, it can be seen that the PV voltage successfully tracks the MPP voltage (120V) and that the flyback voltage controller tracks the step responses in the PV voltage, for an excellent voltage balance at all times. Fig. 13 shows a zoom-out view of the response of the controller under a step change in the PV voltage to check the unity power factor between the grid voltage and the inverter current. All of the PV power is effectively transferred to grid.

IV. Loss Calculation

A. Flyback Converter

1) Losses in the Transformer:

An EI 60 core was chosen for the hardware implementation to provide the power handling capacity. From the data sheet, the core loss for the EI 60 core, while taking into account the temperature change from the room temperature (ΔT), was approximated to be 4W for 200W operation. The turns ratio of the transformer is 0.5.

The power loss due to the leakage inductance present in the transformer is given as:

$$P_{leak} = 0.5 \cdot i_{mpeak}^2 \cdot L_{leak} \cdot f_{sw} = 0.5 \cdot 3.6^2 \cdot 12\mu \cdot 50kHz = 3.8W$$

The copper loss in primary and secondary winding are:

$$P_{cu\text{-}pri} = i_{mrms}^2 \cdot R_{pri} = 2^2 \cdot 600m\Omega = 2.4W$$

$$P_{cu\text{-}sec} = i_{secrms}^2 \cdot R_{sec} = 1.5^2 \cdot 300m\Omega = 0.675W$$

The total loss in the transformer = 10.96W.

2) Losses in the Output Diode:

A SiC schottky diode (C4D20120A) was used in the output of the flyback converter to minimize the loss.

The loss due to the forward voltage (V_f) drop = $V_f \cdot I_o$ = 1.5•2 = 3W.

The conduction loss during the switch off-time = $i_{secrms}^2 \cdot r_{D\text{-}on} = n \cdot i_{mpeak} \cdot \sqrt{\frac{\Delta D}{3}} \cdot r_{D\text{-}on} = 1.8^2 \cdot 0.023 = 0.0745W$

The total loss in the diode = 3.0745W.

3) Losses in the Switch:

A SiC MOSFET (SCH2080KE) was used as the switch in the flyback converter for the hardware prototype.

The conduction loss: $i_{mrms}^2 \cdot R_{DS\text{-}on} = 2^2 \cdot 80m\Omega = 0.32W$.

The switching loss: $\frac{V_{dsmax} I_{dmax} (t_f + t_r) f_{sw}}{2} + \frac{1}{2} C_{oss} V_{dsmax}^2 f_{sw} = 3.165W$

The total loss in the flyback converter = 17.52W ≈ (91%

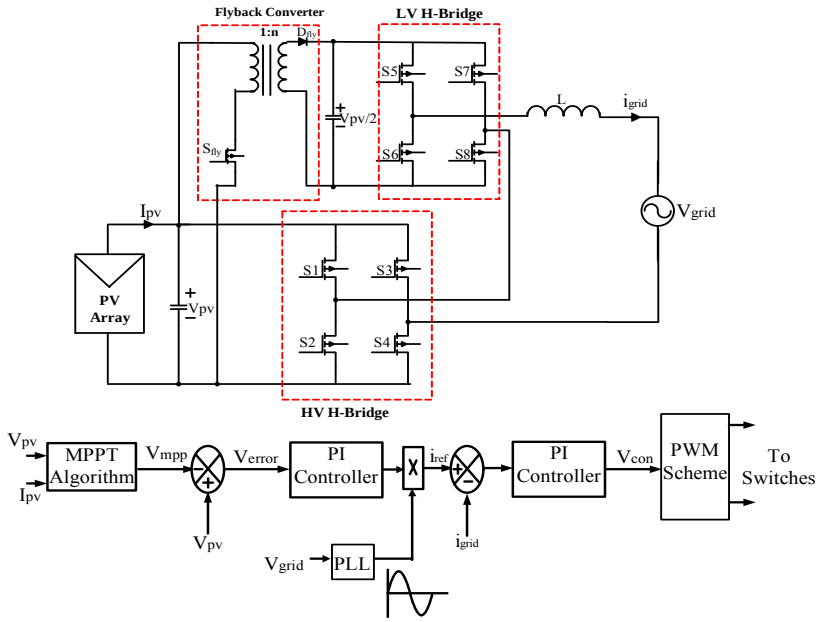


Fig. 11. Control scheme for the proposed PCS in grid connection.

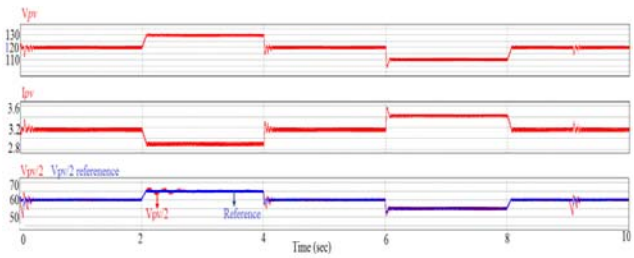


Fig. 12. Grid-connection control scheme with MPPT.

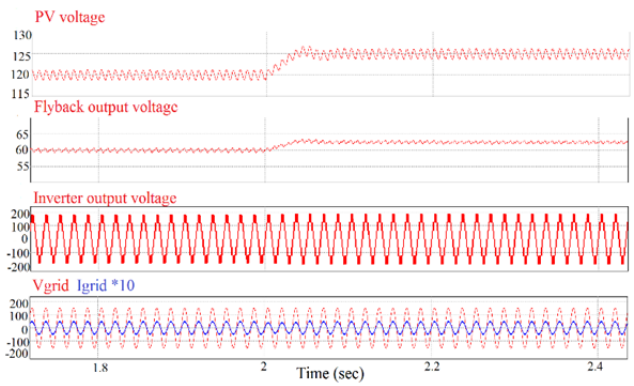


Fig. 13. Simulation results showing the voltage balance of the proposed inverter output during a step change (5V) in PV voltage during MPPT.

efficiency).

B. Asymmetric MLI

Since the HV H-bridge operates under the grid-frequency and the dc-link voltage is considerably lower compared to the single H-bridge topologies, a MOSFET with a low $r_{DS\text{-}on}$ is more suited than the IGBTs used in conventional H-bridge circuits. The switching losses occurring in the HV H-bridge are neglected due to the grid-frequency operation. An IRFP 4868 MOSFET (V_{dss}=300V, I_d=90A, $r_{DS\text{-}on}$=32mΩ) is used in the HV H-bridge circuit.

The conduction loss: $4 \bullet 4.12^2 \bullet 32m = 2.17W$.

Since the LV H-bridge cell operates at a 10kHz switching frequency, a FGP20N60UFD (600V, 20A) IGBT is used. The losses in the LV H-bridge are divided into the conduction loss for the IGBT and diode and the switching loss for the IGBT and diode. Since the fundamental voltage output of asymmetric inverters is varied for each cell, designing the each of the cells in simulations is the ideal way to calculate the losses. From the fundamental voltage block information, the switch and diode current can be determined for calculating the conduction losses.

1) Conduction Losses:

$$P_{cond\text{-}IGBT} = \frac{1}{T}\int_o^T V_{on}\, I(t)dt$$

$$P_{cond\text{-}diode}(t) = i_f(t) \bullet (V_{Fo} + R_f \bullet i_f(t))$$

The conduction loss over one fundamental period of the LV H-bridge is calculated at 7.05W.

2) Switching Losses:

The switching for the IGBT with a free-wheeling diode can be modelled using the switching loss energy in the respective switching device. The switching loss energies can be calculated from the datasheet graphs (Collector current vs Eon and Collector-emittor voltage Eoff graphs). The turn-ON and turn-OFF losses for the IGBT and diode are modelled as below:

$$P_{sw\text{-}ON} = \frac{1}{T}\int_0^T E_{on}(t)dt$$

$$P_{sw\text{-}OFF} = \frac{1}{T}\int_0^T E_{off}(t)dt$$

$$P_{sw\text{-}OFF\text{-}diode} = \frac{1}{T}\int_0^T E_{off-diode}(t)dt$$

The switching loss of the LV H-bridge over one fundamental period is calculated as 2.12W. It should be noted

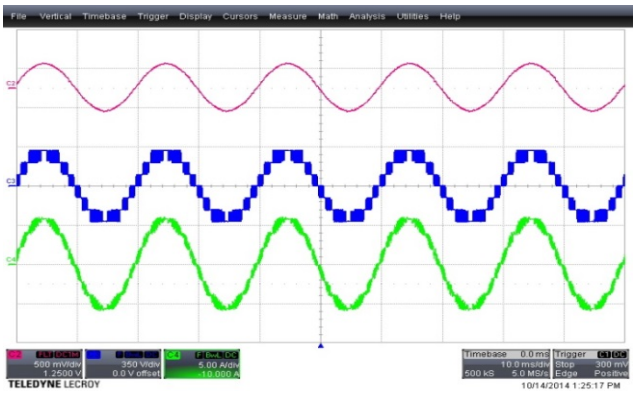


Fig. 14. Inverter output voltage (blue), inductor current waveforms (green) and load voltage (Red) in open-loop operation.

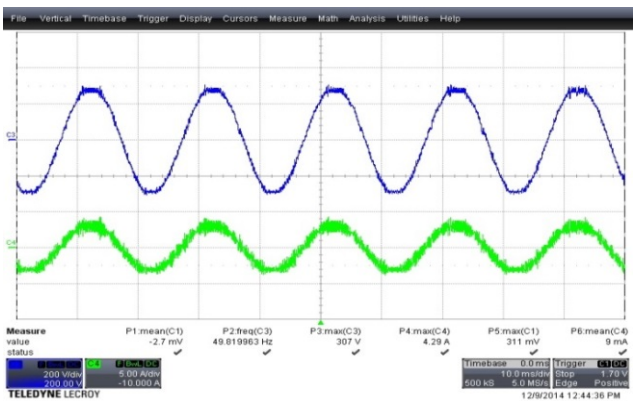


Fig. 15. Load voltage (blue) and inductor current (green) waveforms under a closed-loop stand-alone operation.

that in the asymmetric CHB inverter the conduction loss is relatively higher than the switching loss because during each level, two IGBT and two freewheeling diode are conducting. The total loss from the modelling is 28.86W ≈ 97.12%.

V. Experimental Results

The proposed PV power conditioning system was implemented using a 1-kW hardware prototype for verification. A Texas Instruments (TI) DSC TMS320F28335 was used to produce the gate signals to drive the switching devices in the PCS. The switching frequencies were 50 Hz, 10 kHz and 30 kHz for the main H-bridge, the low-voltage H-bridge and the flyback converter, respectively. A 200W, 2:1 conversion flyback converter was built and operated in the continuous conduction region. Since 80% of the power is processed by the 50-Hz main H-bridge, the efficiency of the system is high, so a small heat sink for the safe operation is enough, compared to that of conventional H-bridge systems. The 7-level output voltage contributes to reductions of the output filter components. The output filter inductor and capacitor were chosen as 1.8mH and 2μF.

Fig. 14 shows a n experimental result of the hardware

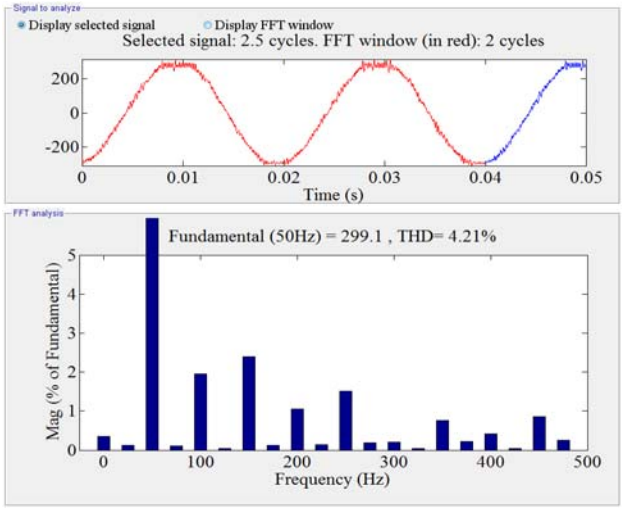


Fig. 16. THD measurement using FFT scope for load voltage (4.21%) under a closed-loop stand-alone operation.

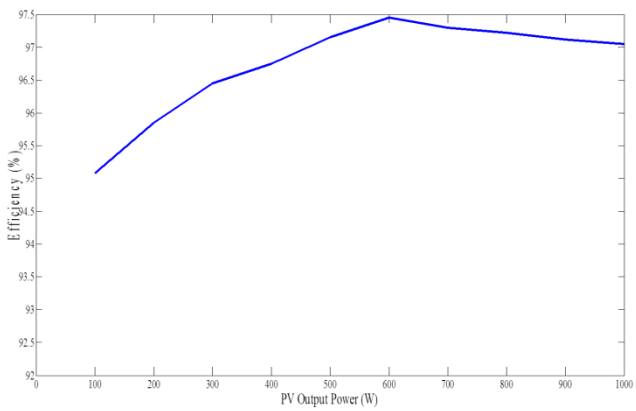


Fig. 17. Efficiency graph for the PV PCS hardware prototype according to the power variation.

prototype operating under the open-loop stand-alone condition. The $220V_{rms}$ result was obtained using a 210 V_{DC} and 50 Ω load. The inverter output voltage shows a 7-level waveform with the voltage levels, ±105 V, ±210 V, and ±315 V, respectively. The efficiency of the entire system was measured as 97.05% from the source to the grid. Previous DER systems using multi-string MLI topologies have been implemented with an efficiency of 96% [4].

Fig. 15 shows a steady-state operation of the designed controllers in closed-loop operation. The hardware was tested under a condition of the $220V_{AC}$ reference and 700W load. The hardware data of the load voltage waveform under the closed-loop operation was used to provide the FFT result by a MATLAB simulation as shown in Fig. 16. The result shows a THD of 4.21%, which satisfies the IEEE regulation standard. The efficiency curve for the PV PCS over a wide operating range is shown in figure 17. It can be seen that a maximum efficiency of 97.45% is achieved at 600W.

In the case of grid-connected operation with the MPPT control scheme, the physical parameters of the PV panel in

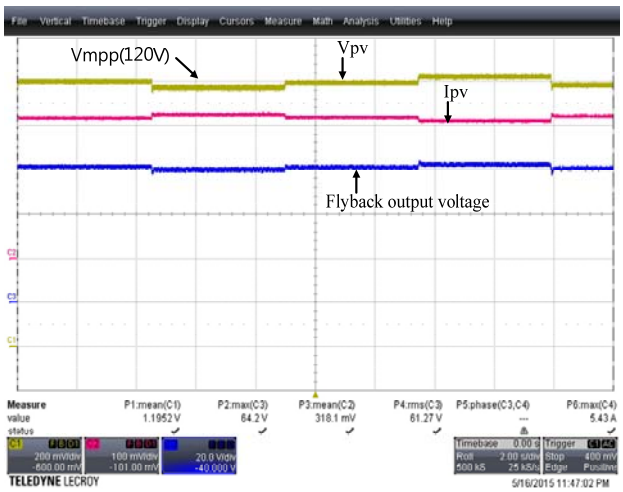


Fig. 18. Experimental result showing the PV voltage tracking the desired MPP voltage (120V) as well as the flyback output regulation.

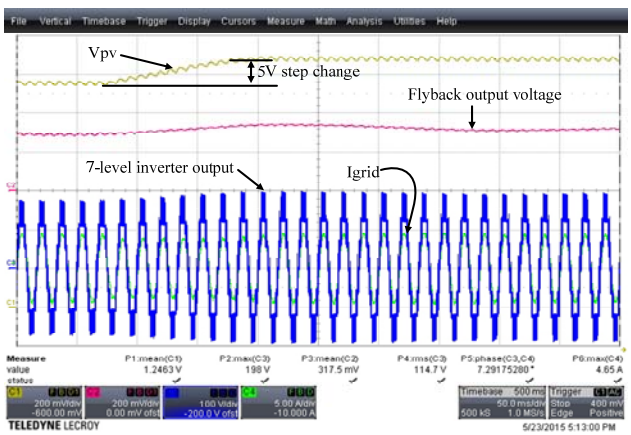


Fig. 19. Experimental results showing the 7-level output voltage balanced during a PV step change.

the simulator were chosen as follows: Open circuit voltage (V_{oc}) as 150V, Maximum power voltage (V_{mpp}) as 120V, Short circuit current (I_{sc}) as 5A, and Maximum power current (I_{mpp}) as 3.16A. The panel was realized by a dual module PV simulator (TerraSAS ELGAR). The time step and voltage step parameters in the MPPT algorithm were chosen as 4 seconds and 3V, respectively. Fig. 18 shows experimental results of successfully tracking the 120V MPP voltage using a P&O algorithm. It can be seen that the flyback output voltage follows exactly half of the PV voltage even when it is perturbed by the MPP tracker. This ensures the voltage balance between the two H-bridge circuits.

For the validation of the balancing capability of this control scheme, the PV voltage step was increased during the MPPT operation. From the results shown in Fig. 19, it can be clearly seen that the flyback voltage loop, which is 4 times faster than the PV voltage dynamics, is able to track the PV voltage quickly, ensuring that the waveform quality is not affected by voltage unbalancing during a step change.

In addition, one of the main criteria that distributed

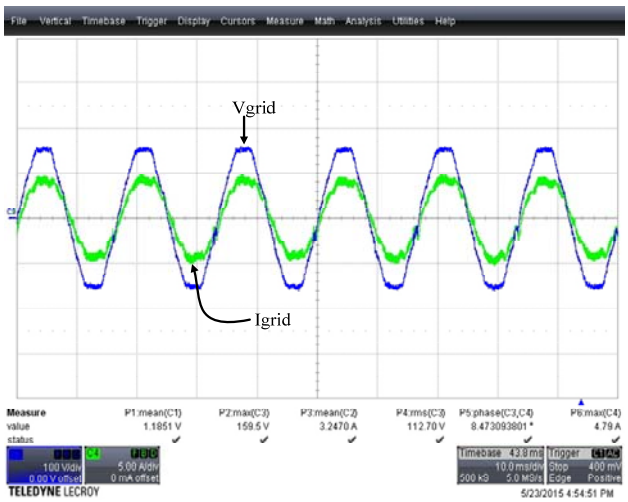


Fig. 20. Grid voltage and the inverter current fed to the grid.

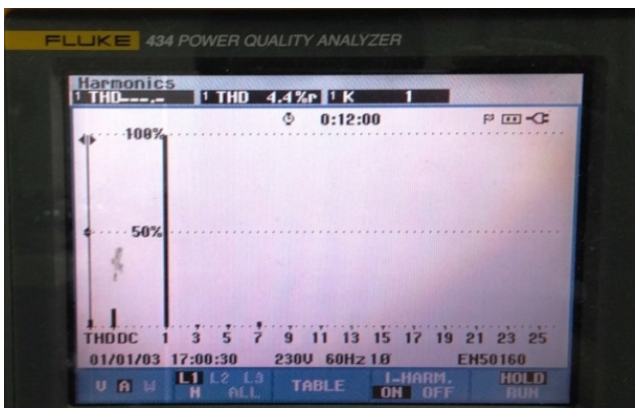


Fig. 21. THD measurement of the grid current (4.4%).

renewable energy systems should satisfy is the THDs of the current injected into the grid, which is a 5% maximum IEEE standard. Fig 20 shows the grid voltage and current fed to the grid by the proposed PCS. It can be seen that even under harsh grid voltage conditions along with a relatively low filter inductance, the current waveform complies with the IEEE standard. The THDs are shown in Fig. 21.

Transitions between the grid-connected and islanding modes are a critical part of grid interfaced PV systems. Especially in distributed generation (DG) systems. When a fault in the grid occurs, the PV inverter should dis-connect from the grid and supply power to critical loads. The IEEE standard for disconnecting a PV inverter from the grid during fault conditions is 2 seconds. Several control schemes have been discussed in the literature to ensure a smooth transition during grid fault conditions. The control scheme with current regulation as the inner-loop and the current reference depending on the fault condition as the outer-loop ensures the elimination of high current spikes during the transition process. The control scheme used for the transition process in the hardware prototype is shown in Fig. 22. The reference for the current loop is flipped between the grid and stand-alone

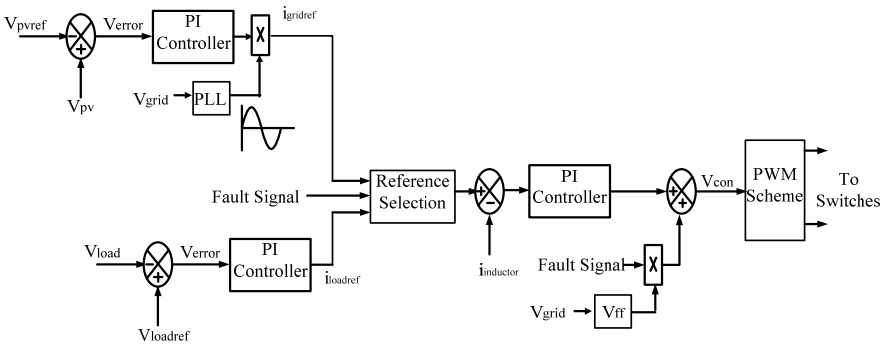


Fig. 22. Control scheme for the PCS for enabling transition operation.

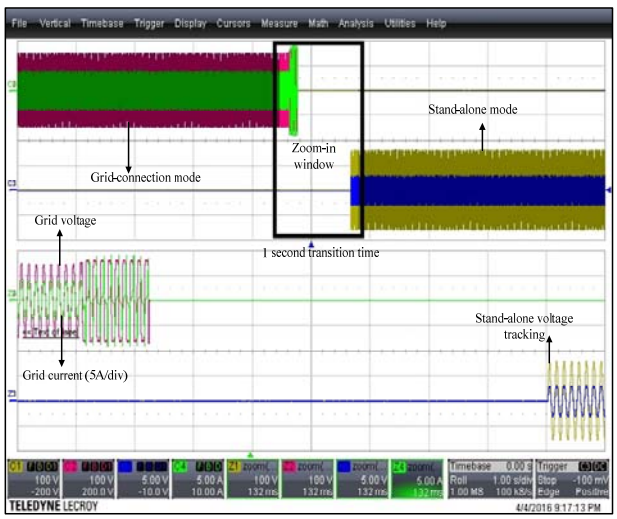
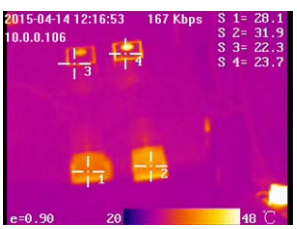
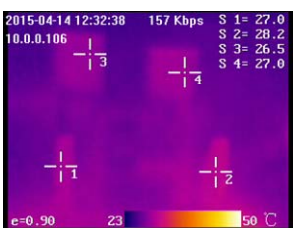


Fig. 23. Hardware result for the transition from grid connection to stand-alone mode showing regulation in both modes.



(a) HV H-bridge.

(b) Flyback converter.



(c) LV H bridge.

Fig. 24. Thermal image showing the surface temperature of the individual inverter/converter in the proposed PCS (no heat sink) (a) and (c) S1,S2,S3,S4=Switches in H-bridge (b) S1= Flyback diode,S2= Flyback transformer,S3= Flyback switch .

loops based on the fault signal (Grid enabled=high, Stand-alone=low). The grid voltage is feed-forwarded to the control voltage during grid-connection to ensure unity power factor operation. Fig. 23 shows the hardware results during the transition process, the one second delay during the transition process is due to the manual switching process in connecting the stand-alone load. The result shows that when a fault in the grid occurs, the PCS is disconnected from the grid and it begins to supply power to the load smoothly without any high current spikes.

Fig. 25. Thermal image showing the surface temperature of the four switches in conventional 3-level H-bridge (no heat sink) S1, S2, S3, S4=Switches in H-bridge.

As previously discussed, another advantage of the asymmetric MLI topology is the transmission of 80% power under the line frequency. This immensely reduces the heat generation caused by the switching losses. DM-60 thermal imaging equipment was used to measure the surface temperatures of all of the switching devices in the proposed PCS under 1kW operation without any heat-sink to verify this feature (see Fig 24). The surface temperature of a conventional unipolar H-bridge under 200W operation was also measured without a heat-sink for a comparison of the switching losses (see Fig 25). From the figures, it can be concluded that the cooling system required for the proposed PCS is drastically reduced compared to the conventional H-bridge PCS. Hence, it helps in reducing the cooling cost and improving the compactness and reliability of the system.

VI. CONCLUSION

An asymmetric multilevel inverter for a single-sourced PV power conditioning system is proposed in this paper, and validated by hardware tests. The asymmetric inverter reduces number of the pre-stage DC sources. A flyback converter provides the input voltage for the low voltage H-bridge. The topology enhances the low PV voltage up to a high DC-link voltage for grid-connection. Since most of the PV power is processed by the grid-frequency high-voltage H-bridge, the power efficiency can be a high value. At 600W generation power condition, the maximum efficiency of 97.05% was achieved in hardware prototype. The small-signal models of the proposed inverter were derived and verified using an exact PWM-switching model in numerical simulation. A digital controller was realized and verified by a hardware prototype for stand-alone operation. In the case of grid-connected operation, the PV voltage was changed according to the P&O algorithm and the voltage balance was maintained during step changes in the PV voltage. A digital PLL loop was used to provide the phase information of the grid, and a conventional PI controller was used to track the reference. The THD of the current fed to grid was measured at 4.4% under harsh grid voltage conditions.

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REFERENCES

[1] E. Dall'Anese, S. V. Dhople, B. B. Johnson, and G. B. Giannakis, "Decentralized optimal dispatch of photovoltaic inverters in residential distribution systems," *IEEE Trans. Energy Convers.*, Vol. 29, No. 4, pp. 957-967, Dec. 2014.

[2] H. Xin, Y. Liu, Z. Qu, and D. Gan, "Distributed control and generation estimation method for integrating high-density photovoltaic systems," *IEEE Trans. Energy Convers.*, Vol. 29, No. 4, pp. 988-996, Dec. 2014.

[3] G.Masson, M. Latour, and D. Biancardi, "Global market outlook for photovoltaics until 2016," in *European Photovoltaic Industry Association*, 2012.

[4] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," *IEEE Trans. Power Electron.*, Vol. 26, No. 9, pp. 2386-2392, Sep. 2011.

[5] M. Boztepe, F, Guinjoan, G. Velasco-Quesada, S. Silvestre, A. Chouder, and E. Karatepe, "Global MPPT scheme for photovoltaic string inverters based on restriceted voltage window search algorith," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 7, pp. 3302-3312, Jul. 2014.

[6] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, Vol. 24, No. 1, pp. 93-101, Mar. 2009.

[7] E. Romero-Cadaval, G. Spagnuolo, L. G. Franquelo, C. A. Ramos-Paja, T. Sunito, and W. M. Xiao, "Grid-connected photovoltaic generation plants: components and operation," *IEEE Ind. Electron. Mag.*, Vol. 7, No. 3, pp. 6-20, Sep. 2013.

[8] H. Patela and V. Agarwal, "MPPT scheme for a PV-fed single-phase single-stage grid-connected inverter operating in CCM with only one current sensor," *IEEE Trans. Energy Convers.*, Vol. 24, No. 1, pp. 256-263, Mar. 2009.

[9] L. An and D. D. C. Lu, "Design of a single-switch DC/DC converter for a PV-battery-powered pump system with PFM+PWM control," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 2, pp. 910-921, Feb. 2015.

[10] M. Amirabadi, A. Balakrishnan, H. A. Toliyat, and W. C. Alexander, "High-frequency AC-link PV inverter," *IEEE Trans. Ind. Electron*., Vol. 61, No. 1, pp. 281-291, Jan. 2014.

[11] N. Sukesh, M. Pahlevaninezhad, and P. K. Jain, "Analysis and implementation of a single-stage flyback PV microinverter with soft switching," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 4, pp. 1819-1833, Apr. 2014.

[12] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 1, pp. 256-269, Jan. 2015.

[13] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron*., Vol. 62, No. 2, pp. 922-929, Feb. 2015.

[14] B. P. McGrath, D. G. Holmes, and W. Y. Kong, "A decentralized controller for a cascaded H-bridge multilevel converter," *IEEE Trans. Ind. Electron*., Vol. 61, No. 3, pp. 1169-1178, Mar. 2014.

[15] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating hybrid power source into an islanded MVMicrogrid using CHB multilevel inverter under unbalanced and nonlinear load conditions," *IEEE Trans. Energy Convers*., Vol. 28, No. 3, pp. 643-651, Sep. 2013.

[16] H. R. Teymour, D. Sutanto, K. M. Muttaqi, and P. Ciufo, "Solar PV and battery storage integration using a new configuration of a three-level NPC inverter with advanced control strategy," *IEEE Trans. Energy Convers.*, Vol. 29, No. 2, pp. 354-365, Jun. 2014.

[17] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[18] D. Balakrishnan and K Indiradevi. "Modified multilevel inverter topology with reduced switch count and a novel PWM control scheme," in *International Conference on Computer Communication and Informatics (ICCCI)*, Jan. 2014.

[19] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl*., Vol. 51, No. 2, pp. 1722-1731, Mar./Apr. 2015.

[20] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, Vol. 56. No. 11, pp. 4399-4406, Nov. 2009.

[21] S. K. Chattopadhay, C. Chandan, A. K. Sinha, and B. C. Pal, "Asymmetric multilevel inverter with quasi-linear power distribution ratio for grid connected photovoltaic converters,"

in *IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 1-6, May 2013.
[22] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one DC supply," *IEEE Trans. Veh. Technol*., Vol. 59. No. 8, pp. 3736-3743, Oct. 2010.
[23] F. S. Kang, S. J. Park, M. H. Lee, and C. U. Kim, "An efficient multi-level synthesis approach and its application to a 27-level inverter," *IEEE Trans. Ind. Electron.*, Vol. 52. No. 6, pp. 1600-1606, Dec. 2005.
[24] A. K. Panda and Y. Suresh, "Research on cascade multi-level inverter with single DC source using three-phase transformers," *International Journal of Electrical Power & Enery Systems*, Vol. 40, No. 1, pp.9-20, Sep. 2010.
[25] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, Vol. 49. No. 4, pp. 724-738, Aug. 2002.
[26] B. P. McGrath, D. G. Holmes, M. Manjrekar, and T. A. Lipo, "An improved modulation strategy for a hybrid multilevel inverter," in *IEEE Industry Applications Conference*, pp. 2086-2093, Oct. 2000.
[27] A. C. Kyritsis, E. C. Tatakis, and N. P. Papanikolaou, "Optimum design of the current-source flyback inverter for decentralized grid-connected photovoltaic systems," *IEEE Trans. Energy Convers.*, Vol. 23, No. 1, pp. 281-293, Mar. 2008.
[28] T. V. Thang, N. M. Thao, J. H. Jang, and J.-H. Park, "Analysis and design of grid-connected photovoltaic systems with multiple- integrated converters and a pseudo-DC-link inverter," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 7, pp. 3377-3386, Jul. 2014.
[29] Y. Li and R. Oruganti, "A low cost flyback CCM inverter for AC module application," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1295-1303, Mar. 2012.
[30] J.-W. Kim and J.-I. Ha, "Cell balancing method in flyback converter without cell selection switch of multi-winding transformer," *Journal of Electrical Engineering & Technology*, Vol. 11, No. 2, pp. 367-376, Mar. 2016.
[31] G.-Y. Jeonga and S.-H. Kwon, "Improved single-stage AC-DC LED-drive flyback converter using the transformer-coupled lossless snubber," *Journal of Electrical Engineering & Technology*, Vol. 11, No. 3, pp. 644-652, May 2016.
[32] M. S. Manoharan, A. Ahmed, H. W. Kim, and J. H. Park, "A single-source photovoltaic power conditioning system using asymmetric cascaded multilevel inverter," in *9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015.
[33] J.-M. Kwon, K.-H. Nam, and B.-H. Kwon, "Photovoltaic power conditioning system with line connection," *IEEE Trans. Ind. Electron.*, Vol. 53 No. 4. pp. 1048-1054, Jun. 2006.

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