JPE 16-6-26

http://dx.doi.org/10.6113/JPE.2016.16.6.2258
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Performance Analysis and Comparison of Post-Fault PWM Rectifiers Using Various Space Vector Modulation Methods

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Abstract

In this paper, some crucial performance characteristics related to the operational reliability of the post-fault Pulse Width Modulated (PWM) rectifiers, such as line current harmonic distortion, Common Mode Voltage (CMV), and current stress on the capacitors, are fully investigated. The aforementioned performance characteristics of post-fault rectifiers are highly dependent on the utilized space vector modulation (SVM) schemes, which are also examined. Detailed analyses of the three most commonly used SVM schemes for post-fault PWM rectifiers are provided, revealing the major differences in terms of the zero vector synthesis approaches. To compare the performances of the three SVM schemes, the operating principles of a post-fault rectifier are presented with various SVM schemes. Using analytical and numerical methods in the time domain, the performances of the line current distortion, common mode voltage and capacitor current are evaluated and compared for each SVM scheme. The proposed analysis demonstrates that the zero vector synthesis approaches of the considered methods have significant impacts on the performance characteristics of rectifiers. In addition, the advantages and disadvantages of the proposed SVM schemes are discussed. The experimental results verify the effectiveness and validity of the proposed analysis.

Key words: Capacitor current stress, Common mode voltage, Current harmonic distortion, Post-fault PWM rectifier, Reliability, Space vector modulation

I. INTRODUCTION

Three-phase six-switch (TPSS) PWM rectifiers are widely used in AC/DC energy conversion systems, such as renewable energy power generation, flexible AC transmission and active power filters. However, one of the major concerns for PWM rectifiers is system reliability. Faults that occur in the power electronic devices endanger the system operation, which leads to undesirable economic losses [1]. Thus, cost-effective fault-tolerant systems with the ability to handle unforeseen failures of semiconductor switches are desired to enable operation to continue after a fault occurs.

Over the past few years, considerably research efforts have focused on fault-tolerant converters with consideration of failures of semiconductor power switches [2]-[18]. Among the various proposed topologies, the three-phase four-switch (TPFS) topology presented in [5]-[18] is a promising option for fault-tolerant PWM rectifiers. In post-fault operation, the faulty phase is replaced with the split of a DC-link capacitor, and the post-fault grid-connected PWM rectifier is equivalent to a TPFS PWM rectifier.

When faults occur to the power switches, the transient performance of the topology changing interval should be guaranteed. This has attracted a lot of research interests. In [16], the transient performance of a fault-tolerant PWM rectifier at the topology changing interval is fully investigated. It is concluded that the transient performance is strongly dependent on the initial DC-link voltage, the response time after fault detection, and the controller parameters.

However, the main concern for a fault-tolerant PWM rectifier is system reliability in post-fault operation. More specifically, this concern should be for the prevention of secondary faults that permanently damage the entire system. Due to the special topology of post-fault PWM rectifiers, the primary issue is to eliminate the imbalanced three-phase current introduced by the capacitor voltage fluctuation.

Manuscript received Apr. 11, 2016; accepted Aug. 8, 2016
Recommended for publication by Associate Editor Trillion Q. Zheng.
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Researchers have proposed several compensated space vector modulation schemes for TPFS PWM rectifiers to reject the imbalanced three-phase current caused by capacitor voltage fluctuations [10]-[18]. Aside from imbalanced line currents, other performance characteristics, which are strongly related to the reliability of post-fault rectifiers, should be comprehensively investigated to ensure stable post-fault operation.

When rectifiers operate in post-fault condition, the phase voltage harmonics are increased due to a reduced number of active vectors. The increased voltage harmonics produce more severe line current distortions, giving rise to more acoustic noises and copper losses. Furthermore, to realize non-stop operation in the post-fault condition, the line current distortions of the rectifiers should meet the standards for grid connection such as IEEE std. 1547 in [19]. If the line current distortions exceed the requirements in the standards, the rectifiers are disconnected from the utility [20]-[23]. Therefore, the reliability of post-fault rectifiers is intensively deteriorated by line current distortions, which should be suppressed.

In addition, when post-fault rectifiers serve as interfaces between a power grid and the PV panels in solar power generation without isolation transformers, the galvanic isolation between the grid and the PV arrays is absent. A parasitic capacitance is formed between the PV module and the frame because of the presence of dielectric between them. When a high-frequency common mode voltage (CMV) is present across the parasitic capacitance, excessive leakage currents are produced. These leakage currents result in many issues related to safety of people in contact with PV modules, and degrades the system reliability [24]-[26]. Therefore, common mode voltage should be suppressed to improve the reliability of post-fault rectifiers and personnel safety.

Furthermore, the lifetime of DC capacitors is a function of the surrounding ambient temperature and the internal heating caused by current flowing through the equivalent series resistance (ESR) of the capacitor, especially in post-fault rectifiers with one phase current flowing directly into the capacitor bank [27]-[30]. Consequently, excessive capacitor current may result in premature failure of the DC capacitors, which endangers the reliability and uninterruptible operation of systems. To improve the reliability of the post-fault rectifiers, the capacitor currents should be alleviated to extend the lifetimes of the DC capacitors.

The SVM schemes discussed in [10]-[18] are classified into three major categories: SVM schemes with the zero vectors synthesized by two short vectors (SVSVM) [11]-[13], [16]-[18], SVM schemes with the zero vectors synthesized by two long vectors (LVSVM) [14], [15] and SVM schemes with the reference vector synthesized by the nearest three vectors (NTSVM) [10]. The essential difference between these three SVM strategies is the zero vector synthesis method. The distributions of the zero-voltage space vectors within a cycle period have a significant effect on the line current harmonics, common mode voltage and capacitor current stress, as already exposed in 6-switch PWM rectifiers under normal operation [25]. However, detailed performance analyses and comparisons of the SVM schemes, in terms of the line current distortion, common voltage and capacitor current stress, are still rare regarding post-fault PWM rectifiers. Thus, a distinct analysis is required to elaborate the different effects of SVM schemes for post-fault rectifiers.

The main purpose of this paper is to evaluate the various SVM strategies of post-fault PWM rectifiers. This paper first presents the different zero vector synthesis methods for the SVM schemes of post-fault PWM rectifiers. Next, the operating principles of post-fault rectifiers under different SVM schemes are investigated. Moreover, the performance characteristics of the modulation strategies are analyzed in detail by computing their RMS values in the time domain. Thus, the line current distortion, common mode voltage and capacitor current stress characteristics of post-fault rectifiers with various SVM schemes are obtained and compared. Finally, the analytical results are verified by laboratory experiments. Thus, the optimized reliability of post-fault rectifiers can be realized with the provided analysis results.

II. Structure and Fundamental of a Post-fault PWM Rectifier

A circuit diagram of fault-tolerant PWM rectifiers is shown in Fig. 1(a). R and L are the resistance and inductance of the filtering inductor, respectively. The output DC voltage, equivalent load and load current are represented by v_o, R_L and i_L, respectively. The two split capacitors are assumed to be identical (i.e., C_1=C_2), and the currents flowing through the two capacitors are defined as i_{c1} and i_{c2}. The capacitor voltages are represented by v_{c1} and v_{c2}. F_1-F_6 denote fast fuses connected with three phase legs in series, which are able to isolate a broken-down leg when a short-circuit faults occur. TR_a, TR_b and TR_c are bidirectional thyristors for connecting the faulty phase with the neutral point of the DC link, providing an additional phase circuit for the faulty phase. For example, if there is an open circuit failure or a short circuit failure (with F_1 and F_2 fusing) of the semiconductor switch S_a, then the broken-down phase a is connected to the neutral point o by the turn on of TR_a. Therefore, a post-fault PWM rectifier topology is rebuilt at the fault operation, with minimum requirements in terms of additional hardware, as shown in Fig. 1(b). Considering unity power operation, vector diagrams of the post-fault rectifier are shown in Fig. 1(c). The switching functions p_b and p_c are presented along with the definition:

$$p_j = \begin{cases} 1, S_j \text{ closed}, \\ -1, \overline{S}_j \text{ closed}, \end{cases} \quad j = b, c \tag{1}$$

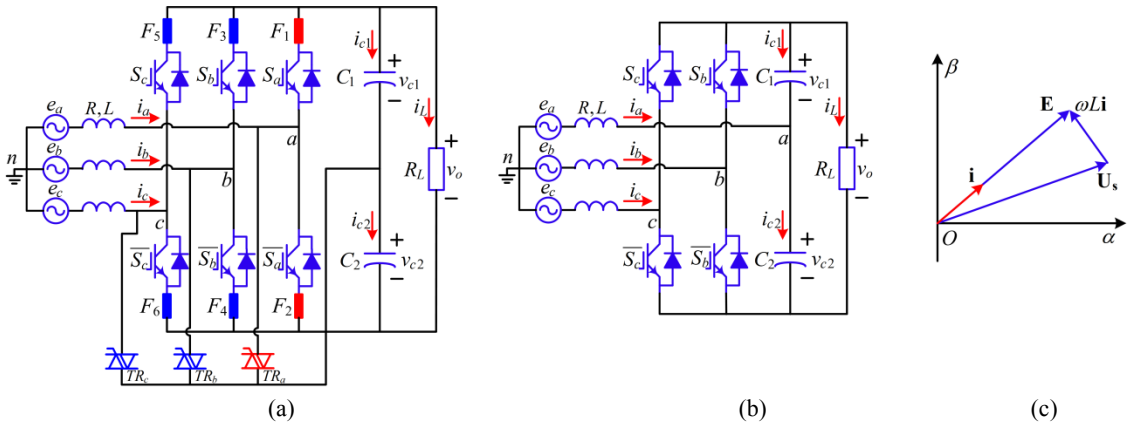


Fig. 1. Basis of a post-fault PWM rectifier. (a) Topology of the proposed fault-tolerant rectifier. (b) Topology of the post-fault rectifier. (c) Vector diagrams of the post-fault rectifier.

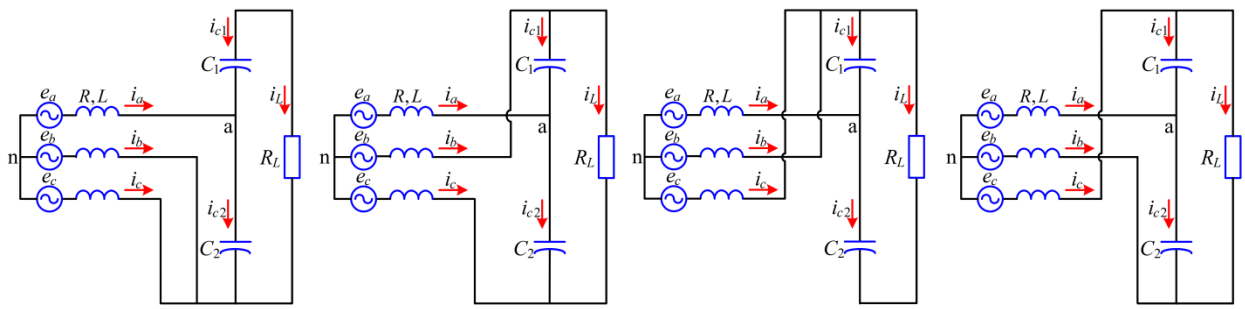


Fig. 2. Equivalent circuits of the post-fault PWM rectifier using the four active vectors: (a) **U1** (p_b=-1, p_c=-1); (b) **U2** (p_b=1, p_c=-1); (c) **U3** (p_b=1, p_c=1). (d) **U4** (p_b=-1, p_c=1).

Fig. 2 shows an equivalent circuits of a post-fault PWM rectifier using four active vectors with all of the possible combinations of p_b and p_c. According to Fig. 2, the output voltage vector $\mathbf{U_s}$ can be represented by the switching states as:

$$\mathbf{U_s}=\begin{bmatrix}u_{an}\\u_{bn}\\u_{cn}\end{bmatrix}=\frac{v_{c1}}{3}\begin{bmatrix}-p_b-p_c\\2p_b-p_c\\2p_c-p_b\end{bmatrix}+\frac{v_{c2}}{3}\begin{bmatrix}2-p_b-p_c\\2p_b-p_c-1\\2p_c-p_b-1\end{bmatrix} \quad (2)$$

Based on Equ. (2), the amplitudes of the three-phase output voltage are listed in Table I, with an assumption of the equality of the capacitor voltages (v_{c1}=v_{c2}=v_o/2). According to Table I, the amplitudes of the three-phase output voltages depend on the vectors applied, and the harmonics of the output voltage are determined by the choice of vectors per sampling period. Consequently, the choice of vectors per sampling period affects the line current harmonics of the post-fault PWM rectifier.

Furthermore, common mode voltage is defined as the potential of the neutral point of the DC link with respect to the power line ground. For post-fault PWM rectifiers, the common mode voltage is simply the faulty phase voltage u_{an}, which is highly dependent on the applied vectors, as shown in Fig. 2.

In addition, the DC-link capacitor current is the difference between the load current i_L and segments of the rectifier phase currents, which are dependent on the rectifier switching state. For example, when the vector $\mathbf{U_2}$ is applied, the post-fault PWM rectifier is equivalent to Fig. 2 (b), where phase *b* and phase *c* are connected to the positive DC bus and the negative DC-link rail, respectively. Due to the complementary operation of DC-side capacitors, an analysis of capacitor current can be focused on capacitor C_1. According to Fig. 2 (b), the capacitor current i_{c1} under vector $\mathbf{U_2}$ is the difference between the load current i_L and the phase currents i_b. The expressions of the capacitor currents i_{c1} corresponding to the four vectors are also listed in Table I. The different vectors result in varied capacitor currents.

The above analysis reveals that the choice of the vectors within a cycle period has a significant effect on the AC current ripple, the common voltage and the capacitor current.

III. Various Space Vector Modulation Strategies of Post-Fault PWM Rectifiers

The main concept of space vector modulation in a post-fault rectifier is similar to that of a six-switch converter, where the reference vector should be synthesized by two active basic vectors according to the principle of the voltage-second values being equal. In 6-switch rectifiers, the rest time portions are filled with zero vectors 000 or 111. However, due to the absence of zero vectors in post-fault

TABLE I
CRUCIAL PERFORMANCES OF THE POST-FAULT RECTIFIER WITH DIFFERENT VOLTAGE VECTORS

Switching state (p_b, p_c)	Common mode voltage u_{an}	Phase voltage u_{bn}	Phase voltage u_{cn}	Capacitor current i_{c1}
$\mathbf{U_1}$ (-1, -1)	$v_o/3$	$-v_o/6$	$-v_o/6$	$-i_L$
$\mathbf{U_2}$ (1, -1)	0	$v_o/2$	$-v_o/2$	i_b-i_L
$\mathbf{U_3}$ (1, 1)	$-v_o/3$	$v_o/6$	$v_o/6$	$-i_a$-i_L
$\mathbf{U_4}$ (-1, 1)	0	$-v_o/2$	$v_o/2$	i_c-i_L

Table II
UTILIZED VECTORS IN THREE SVM SCHEMES

	Sector I	Sector II	Sector III	Sector IV
SVSVM	$\mathbf{U_1}$, $\mathbf{U_2}$, and $\mathbf{U_3}$	$\mathbf{U_1}$, $\mathbf{U_2}$, and $\mathbf{U_3}$	$\mathbf{U_1}$, $\mathbf{U_3}$, and $\mathbf{U_4}$	$\mathbf{U_1}$, $\mathbf{U_3}$, and $\mathbf{U_4}$
LVSVM	$\mathbf{U_1}$, $\mathbf{U_2}$, and $\mathbf{U_4}$	$\mathbf{U_2}$, $\mathbf{U_3}$, and $\mathbf{U_4}$	$\mathbf{U_2}$, $\mathbf{U_3}$, and $\mathbf{U_4}$	$\mathbf{U_1}$, $\mathbf{U_2}$,and $\mathbf{U_4}$
NTSVM	$\mathbf{U_1}$, $\mathbf{U_2}$, and $\mathbf{U_4}$	$\mathbf{U_1}$, $\mathbf{U_2}$, and $\mathbf{U_3}$	$\mathbf{U_2}$, $\mathbf{U_3}$, and $\mathbf{U_4}$	$\mathbf{U_1}$, $\mathbf{U_3}$, and $\mathbf{U_4}$

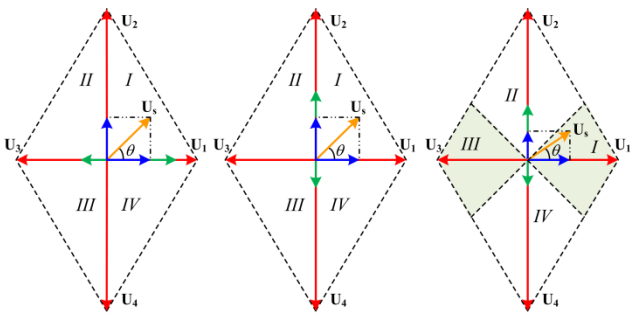


Fig. 3. Voltage vector synthesis of the three SVM schemes in Sector I: (a) SVSVM; (b) LVSVM; and (c) NTSVM.

rectifiers, the remaining time cannot be allocated by the conventional approach of six-switch converters. Therefore, it is impossible to use only two active vectors to synthesize the reference voltage $\mathbf{U_s}$ in one switching period. For post-fault rectifiers, two opposite active vectors ($\mathbf{U_1}$-$\mathbf{U_3}$ or $\mathbf{U_2}$-$\mathbf{U_4}$), whose volt-second integral is equal to zero, are used to achieve the equivalent zero vectors. For example, when the reference voltage vector lies in Sector I, the effective part is always synthesized by $\mathbf{U_1}$ and $\mathbf{U_2}$, whereas the remaining part is synthesized by either $\mathbf{U_1}$-$\mathbf{U_3}$ (SVSVM) or $\mathbf{U_2}$-$\mathbf{U_4}$ (LVSVM), as shown in Fig. 3. It should be noted that only one pair of equivalent zero vectors can be utilized during one switching period, because each power switch only switches 2 times per period due to the switching losses limitations. Based on the distinct equivalent zero vector synthesis approaches, three commonly used SVM schemes (SVSVM, LVSVM, and NTSVM) are developed, and their utilized voltage vectors per switching period are listed in Table II. The sector division of the NTSVM is different from those of the other two SVM strategies.

Table II illustrates that the equivalent zero vectors in the SVSVM strategy are always synthesized by $\mathbf{U_1}$ and $\mathbf{U_3}$, and that $\mathbf{U_2}$ and $\mathbf{U_4}$ are always selected in the LVSVM strategy. The NTSVM can be regarded as a composition of the SVSVM and LVSVM strategies, where the reference vectors are always synthesized by the three basic vectors nearest to the reference vector. Thus, if the reference vector $\mathbf{U_s}$ lies in Sector I ($\theta \in [-\pi/4, \pi/4]$) and Sector III ($\theta \in [3\pi/4, 5\pi/4]$), the zero vector is synthesized by $\mathbf{U_2}$ and $\mathbf{U_4}$ like in the LVSVM method. Meanwhile, if the reference vector lies in Sector II ($\theta \in [\pi/4, 3\pi/4]$) and Sector IV ($\theta \in [5\pi/4, 7\pi/4]$), the zero vectors is synthesized by $\mathbf{U_1}$ and $\mathbf{U_3}$, as in the SVSVM method.

According to the different utilizations of vectors, various SVM strategies introduce varied PWM sequences, as shown in Fig. 4. As noted above, the choice of the vectors and its corresponding PWM sequence within a cycle period have significant effects on the AC current ripple, common voltage and capacitor current.

Regarding the AC current harmonics, various SVM strategies select different amplitudes and have various timings of the output voltage of the post-fault rectifier, resulting in different grid current harmonics. In addition, the faulty phase voltage u_{an} has a vastly different amplitude compared to other two phase voltages, leading to a unique harmonic content of the faulty phase current in post-fault PWM rectifiers. In the normal 6-switch rectifiers' case, the total harmonic distortion (THD) of one arbitrary phase current is usually utilized to evaluate the current distortions injected into the grid. However, in the proposed post-fault rectifiers' case, the THD of only one phase current is not appropriate for evaluating the overall current distortions, because the harmonic contents of the faulty phase current are different from other two phase currents. Therefore, an alternative approach for the evaluation of the current harmonic characteristic of post-fault PWM rectifiers is required.

Moreover, the common mode voltage, namely the faulty phase voltage u_{an}, is also affected by the different SVM strategies. For example, the common mode voltage u_{an} has bipolar values of $v_o/3$ and $-v_o/3$ when the SVSVM is utilized, because both $\mathbf{U_1}$ and $\mathbf{U_3}$ are used as ineffective vectors. On the other hand, when the LVSVM is implemented, only u_{an}

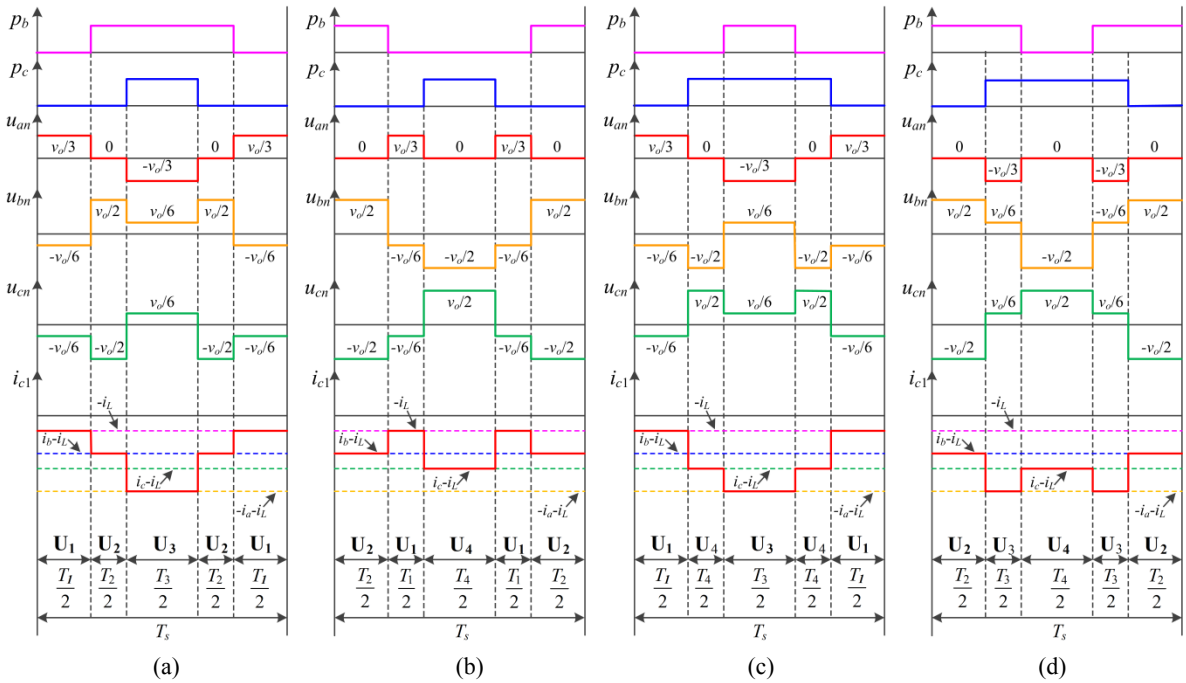


Fig. 4. Switching sequences and crucial performances of the post-fault rectifier using: (a) SVSVM in Sectors I and II, and LVSVM in Sector II; (b) LVSVM in Sectors I and IV, and NTSVM in Sector I; (c) SVSVM in Sectors III and IV, and NTSVM in Sector IV; (d) LVSVM in Sectors II and III, and LVSVM in Sector III.

has a unipolar value and a zero value, because only one vector among $\mathbf{U_1}$ and $\mathbf{U_3}$ is used as an effective vector during a switching period. Moreover, grid interface applications have a major difference compared to motor drive applications in terms of common-mode behavior. In motor drive applications, the common mode current (CMC) i_{cm} is strongly dependent on dv/dt of the converter, and is partially dependent on the CMV magnitude and waveform. On the other hand, in grid-connected applications, the magnitude and RMS value of the CMV play an important role in determining the peak value and RMS of the CMC.

Different SVM strategies also result in different amplitudes and timings of the capacitor current, which results in them generating different harmonic spectrums. The total harmonic distortion (THD) in the frequency domain is often used to evaluate the harmonic spectral of the capacitor current. However, compared with the harmonic spectral analysis, the capacitor current RMS is a meaningful indicator for assessing the current stress on DC-link capacitors, which is related to the power dissipation in the capacitors.

Therefore, detailed and accurate analyses of the effects of various SVM strategies on the line current harmonic distortion, CMV and current stress to the capacitors are essential for stable post-fault operation. The results of such analyses are presented in the following sections.

IV. Performance of the Line Current Harmonic Distortion

As analyzed above, the THD of only one phase current in

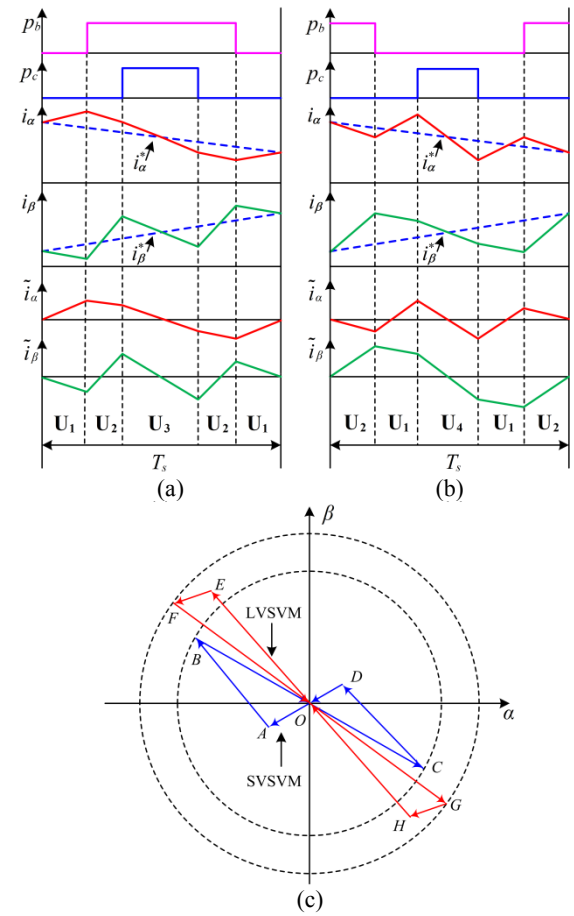


Fig. 5. Switching sequences and related α-β axis current ripples of: (a) SVSVM; (b) LVSVM; (c) current ripple trajectories for both methods.

the frequency domain is not appropriate to evaluate the overall current harmonic performance of a post-fault rectifier. Therefore, the current ripple root mean square (RMS) value, which is a comprehensive index for evaluating all of the three-phase current distortions, is selected as the criterion to evaluate the total current harmonic distortion characteristic of the three SVM approaches from the perspective of the time domain.

The current ripple is defined as follows, ignoring the filter resistance [20]-[22]:

$$\tilde{\mathbf{i}} = \int \frac{\mathbf{U_s} - \mathbf{U_s^*}}{L} dt \tag{3}$$

where $\mathbf{U_s}$ and $\mathbf{U_s^*}$ denote the real output voltage and reference voltage, respectively. As shown in Fig. 3, a difference is found between the reference vector and the output voltage vector of the post-fault PWM rectifier over a switching period. Consequently, undesirable current ripples are produced around the pure sinusoidal reference line currents. Considering the symmetrical allocation of the vectors, the current ripple per switching period is considered only in the first half. According to Equ. (3), the current ripple for both the SVSVM and LVSVM are provided by:

$$\tilde{\mathbf{i}}_{\mathbf{SV}} = \begin{cases} \dfrac{\left(\mathbf{U_1} - \mathbf{U_s^*}\right)\cdot t}{L}, & 0 < t < \dfrac{T_1}{2} \\ \dfrac{\left(\mathbf{U_2} - \mathbf{U_s^*}\right)\cdot t}{L} + \dfrac{\left(\mathbf{U_1} - \mathbf{U_s^*}\right)\cdot T_1}{2L}, & \dfrac{T_1}{2} < t < \dfrac{T_1+T_2}{2} \\ \dfrac{\left(\mathbf{U_3} - \mathbf{U_s^*}\right)}{L}\cdot\left(t - \dfrac{T_s}{2}\right), & \dfrac{T_1+T_2}{2} < t < \dfrac{T_s}{2} \end{cases} \tag{4}$$

$$\tilde{\mathbf{i}}_{\mathbf{LV}} = \begin{cases} \dfrac{\left(\mathbf{U_2} - \mathbf{U_s^*}\right)\cdot t}{L}, & 0 < t < \dfrac{T_2}{2} \\ \dfrac{\left(\mathbf{U_1} - \mathbf{U_s^*}\right)\cdot t}{L} + \dfrac{\left(\mathbf{U_2} - \mathbf{U_s^*}\right)\cdot T_2}{2L}, & \dfrac{T_2}{2} < t < \dfrac{T_2+T_1}{2} \\ \dfrac{\left(\mathbf{U_4} - \mathbf{U_s^*}\right)}{L}\cdot\left(t - \dfrac{T_s}{2}\right), & \dfrac{T_2+T_1}{2} < t < \dfrac{T_s}{2} \end{cases} \tag{5}$$

Based on Eqns (4) and (5), the current ripples in the α-β plane for both the SVSVM and LVSVM are shown in Figs. 5 (a) and (b), respectively, considering that $\mathbf{U_s^*}$ lies in the first quadrant. Moreover, the current ripple trajectories with different SVM schemes in the α-β plane are also provided in Fig. 5(c), where *OA-AB-BC-CD-DO* represents the current ripple trajectory of the SVSVM, and *OE-EF-FG-GI-IO* represents the current ripple trajectory of the LVSVM. Although the current ripple vectors produced by $\mathbf{U_1}$ and $\mathbf{U_2}$ exist with both the SVSVM and LVSVM schemes, their magnitudes differ due to different duration times. For example, *AB* and *OE* are both created using $\mathbf{U_2}$, but with different lengths, which primarily determines the different amplitudes of the current ripple trajectories. Furthermore, the current ripple trajectory of the SVSVM contains *BC* created by $\mathbf{U_3}$, whereas the current ripple trajectory of the LVSVM contains an entirely different current ripple vector *FG* in both the direction and length created by $\mathbf{U_4}$. Consequently, the current ripple vectors have different shapes and amplitudes with different zero vector synthesis methods. This reveals the different overall harmonic distortions of the three-phase line currents caused by the distinct SVM approaches. In terms of the NTSVM, the situation becomes more complex because the NTSVM uses both switching sequences in different sectors and can be considered as a hybrid PWM scheme.

In this study, the current RMS value, which is the RMS value of the current ripple vector's magnitude, is derived to evaluate the total current harmonic distortion performance. Considering the symmetry of the system, the current ripple RMS over a PWM period is defined as:

$$\begin{aligned} \tilde{i}_{RMS} &= \sqrt{\frac{2}{3}\left(\tilde{i}_{\alpha RMS}^{\ 2} + \tilde{i}_{\beta RMS}^{\ 2}\right)} \\ &= \sqrt{\frac{2}{3}\left[\frac{2}{T_s}\int_0^{T_s/2}\tilde{i}_{\alpha}^{\ 2}dt + \frac{2}{T_s}\int_0^{T_s/2}\tilde{i}_{\beta}^{\ 2}dt\right]} \end{aligned} \tag{6}$$

Equ. (6) demonstrates that the three phase current ripples are all considered by the defined current ripple RMS index. This enables an evaluation of the total current harmonic distortion characteristics of the SVM schemes. Substituting the duration time of each vector into Eqns. (3) and (6), the RMS current ripple of the three SVM schemes over a PWM period are described by:

$$\begin{aligned} \tilde{i}_{RMSSV} = \frac{\sqrt{2}U_m^{*2}T_s}{24v_oL}(&-216U_m^{*4}\cos^4\theta + 270U_m^{*4}\cos^2\theta - \\ &12\sqrt{3}v_0U_m^{*3}\left|\sin^3\theta\right| - 18v_o^2U_m^{*2}\cos^2\theta + \\ &27U_m^{*4} + v_o^2)^{\frac{1}{2}} \end{aligned} \tag{7}$$

$$\begin{aligned} \tilde{i}_{RMSSV} = \frac{\sqrt{6}U_m^{*2}T_s}{24v_0L}(&-72U_m^{*4}\cos^4\theta + 90U_m^{*4}\cos^2\theta - \\ &36v_oU_m^{*3}\left|\cos^3\theta\right| - 18v_o^2U_m^{*2}\cos^2\theta + \\ &v_o^4 - 6v_o^2U_m^{*2} + 9U_m^{*4})^{\frac{1}{2}} \end{aligned} \tag{8}$$

$$\tilde{i}_{RMSNT} = \begin{cases} \tilde{i}_{RMSLV}, \mathbf{U_s^*} \text{ in Sector I and III} \\ \tilde{i}_{RMSSV}, \mathbf{U_s^*} \text{ in Sector II and IV} \end{cases} \tag{9}$$

where U_m^* and θ are the magnitude and angle of the reference voltage vector, respectively. Based on Eqns. (7)-(9), the RMS current ripple of the three SVM schemes is shown in Fig. 6 with variations in the reference vector angle θ, where the related parameters are listed in the Appendix. Fig. 6 illustrates that the RMS current ripple per switching period of the SVSVM is less than that of the LVSVM in the entire range, i.e., the line current harmonic contents are reduced when selecting the SVSVM regardless of the voltage vector angle. The RMS current ripple of the NTSVM presents discontinuity with voltage angles θ ranging from 0 to 2π, due to the alternative use of the switching sequences of the SVSVM and LVSVM in a fundamental period. As a result,

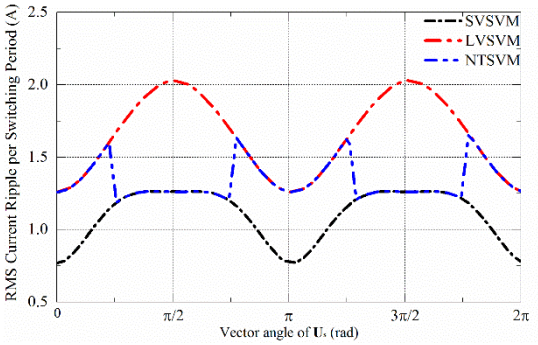


Fig. 6. RMS current ripple over a switching period with v_o=700 V.

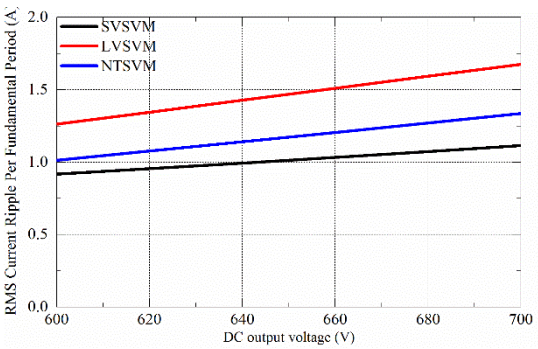


Fig. 7. RMS current ripple during a fundamental period.

the line current harmonic contents of the NTSVM fall in-between those of the SVSVM and the LVSVM.

To assess the current ripple characteristic from a macro perspective, the current ripple RMS over a fundamental period, which can also be considered as the overall line current harmonic losses, are given by:

$$\tilde{I}_{RMS}=\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\tilde{i}_{RMS}^{\,2}\,d\theta} \tag{10}$$

Considering Eqns. (7)-(10), during a fundamental period, the RMS current ripple of the three SVM strategies are expressed as:

$$\tilde{I}_{RMSSV}=\frac{\sqrt{2}U_m^{*2}T_s}{24v_oL}\sqrt{81-\frac{16\sqrt{3}v_o}{\pi U_m^*}-\frac{9v_o^2}{U_m^{*2}}+\frac{v_o^4}{U_m^{*4}}} \tag{11}$$

$$\tilde{I}_{RMSLV}=\frac{\sqrt{6}U_m^{*2}T_s}{24v_oL}\sqrt{27+\frac{48v_o}{\pi U_m^*}-\frac{15v_o^2}{U_m^{*2}}+\frac{v_o^4}{U_m^{*4}}} \tag{12}$$

$$\tilde{I}_{RMSNT}=\frac{\sqrt{2}U_m^{*2}T_s}{24v_oL}\sqrt{81+\frac{10\sqrt{2}(9-\sqrt{3})v_o}{\pi U_m^*}-(27+\frac{18}{\pi})\frac{v_o^2}{U_m^{*2}}+\frac{2v_o^4}{U_m^{*4}}} \tag{13}$$

As shown in Fig. 7, the current ripple RMS is reduced with decreases in the DC output voltage v_o. However, this feature is restricted by the linear modulation range. Thus, a more effective method for line current harmonic reduction is to choose a proper modulation strategy that produces less current ripple. The SVSVM produces the least current ripple with variations of the DC voltage v_o, which is favorable for reducing the line current harmonic distortion. On the other hand, the LVSVM produces the largest line current distortion among the three SVM schemes, and the performance of the NTSVM falls between the SVSVM and the LVSVM.

V. Performance of the Common Mode Voltage

As noted above, for grid-connected applications, the magnitude and RMS value of the CMV play an important role in determining the peak value and RMS of the CMC. Therefore, the RMS values of the CMVs are adopted as the indicator of evaluating the effect of SVM strategies on common mode voltage. A basic principle of the CMV reduction in normal 6-switch PWM rectifiers is to eliminate the zero vectors 000 and 111 in the modulation so that the values of $\pm v_o/2$ can be avoided. Thus, the RMS value of the common mode voltage in a 6-switch rectifier is also reduced by avoiding the zero vectors 000 and 111 [24]-[26]. Meanwhile, in post-fault PWM rectifiers, the CMV reduction methods should be reconsidered due to the different topologies.

Table I illustrates that the long pair vectors $\mathbf{U_2}$ and $\mathbf{U_4}$ produce null common mode voltages, which are effective for CMV reduction. Because the CMV is also the phase voltage u_{an} of the faulty phase, its fundamental component is completely unaffected by different equivalent zero vectors. On the other hand, because the two active vectors selected in the three SVM schemes and their duration times are the same, the major difference in the RMS value of the CMV is generated by the zero vector synthesis methods. For example, the SVSVM applies $\mathbf{U_1}$ and $\mathbf{U_3}$ to synthesize zero vectors. Thus, the CMV values of $v_o/3$ and $-v_o/3$ both appeared in each switching period. In terms of the LVSVM, the bipolar CMV over each switching period can be avoided because only one vector among $\mathbf{U_1}$ and $\mathbf{U_3}$ is selected per switching period. The RMS value of the CMV per switching period can be derived as:

$$u_{anRMS}=\sqrt{\frac{2}{T_s}\int_0^{T_s/2}u_{an}^2dt} \tag{14}$$

The common mode voltages along with the basic voltage vectors are listed in Table V. The RMS values of the CMV for the three SVM schemes can be calculated by substituting these values into Equ. (14):

$$u_{anRMSSV}=\frac{\sqrt{6}}{6}\Big[v_o^2-U_m^*v_o(\sqrt{3}|\sin\theta|-\cos\theta)-U_m^{*2}\cos\theta(2\sqrt{3}|\sin\theta|+9\cos\theta)-3U_m^{*3}\cos^2\theta(\sqrt{3}|\sin\theta|+3\cos\theta)/v_o\Big]^{1/2} \tag{15}$$

$$u_{anRMSLV}=\sqrt{\frac{U_m^*v_o|\cos\theta|}{3}-U_m^{*2}\cos^2\theta} \tag{16}$$

$$u_{anRMSNT}=\begin{cases}u_{anRMSLV},\ \mathbf{U_s^*}\text{ in Sector I and III}\\ u_{anRMSSV},\ \mathbf{U_s^*}\text{ in Sector II and IV}\end{cases} \tag{17}$$

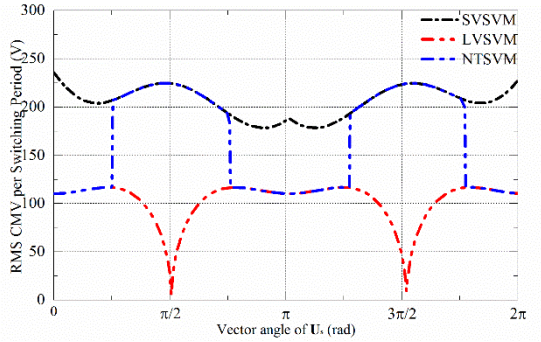


Fig. 8. RMS value of the CMV over one switching period.

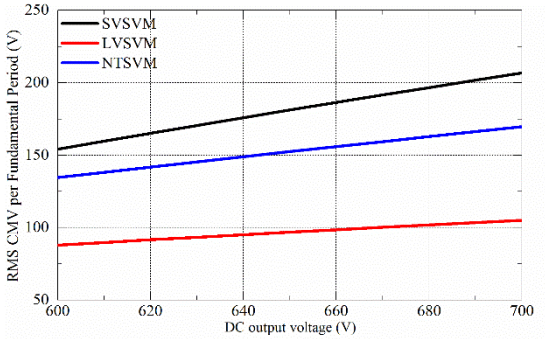


Fig. 9. RMS value of the CMV over a fundamental period.

According to Eqns. (15)-(17), the RMS values of the CMV over a switching period using the three SVM methods are shown in Fig. 8. In contrast to the current ripple characteristic, the CMV is reduced when the LVSVM is selected regardless of the vector angle. Because the voltage vectors $\mathbf{U_2}$ and $\mathbf{U_4}$ produce null common mode voltages, the LVSVM, which usually employs $\mathbf{U_2}$ and $\mathbf{U_4}$, is favorable for CMV reduction. Meanwhile, the SVSVM produces the largest CMV RMS, since the zero vectors are synthesized by $\mathbf{U_1}$ and $\mathbf{U_3}$, while restricting the use of $\mathbf{U_2}$ and $\mathbf{U_4}$. The CMV RMS of the NTSVM also presents discontinuity for the alternative use of switching sequences during a fundamental period, just as in the current ripple characteristic.

The CMV RMS over a fundamental period is a more macroscopic and convincing index for evaluating the CMV characteristic of SVM schemes, and is given by:

$$U_{anRMS}=\sqrt{\frac{1}{2\pi}\int_0^{2\pi} u_{anRMS}{}^2 d\theta} \tag{18}$$

Substituting Eqns. (15)-(17) into Equ. (18), the CMV RMS over a fundamental period is obtained as:

$$U_{anRMSSV}=\frac{\sqrt{3}}{6}\sqrt{2v_o^2-9U_m^{*2}-\frac{4\sqrt{3}U_m^*}{\pi}\left(v_o-\frac{U_m^{*2}}{v_o}\right)} \tag{19}$$

$$U_{anRMSLV}=\sqrt{\frac{2v_oU_m^*}{3\pi}-\frac{U_m^{*2}}{2}} \tag{20}$$

$$U_{anRMSNT}=\frac{\sqrt{3}}{12}\left[v_o^2+\frac{(6\sqrt{2}-4)v_oU_m^*}{\pi}+\left(\frac{3-2\sqrt{6}+2\sqrt{3}}{\pi}-\frac{15}{2}\right)U_m^{*2}+\frac{(24-\sqrt{6}-15\sqrt{2})U_m^{*3}}{\pi v_o}\right]^{1/2} \tag{21}$$

According to Eqns. (19)-(21), the CMV characteristics of the three SVM schemes over a fundamental period are shown in Fig. 9. The LVSVM produces the minimum CMV, whereas the SVSVM produces the maximum CMV, which is 1.5 to 2 times larger than that of the LVSVM. The CMV performance of the NTSVM falls between the LVSVM and the SVSVM, which is similar to the current harmonic distortion characteristic. In addition, the lower DC link voltage also benefits the CMV reduction. However, the CMV values can only be suppressed by decreasing the DC voltage limitedly, due to restrictions on the linear modulation range. Thus, when the performance characteristic of the CMV is taken as a priority in post-fault PWM rectifiers, the most effective approach is to choose the LVSVM as the modulation strategy.

VI. Performance of the Capacitor Current Stress

Field experiences have demonstrated that DC-link capacitors are vulnerable components, and that current stress is the primary provocation for failure of DC-link capacitors. As noted above, various SVM strategies result in a variety of capacitor currents. Thus, it is essential to investigate the capacitor current characteristics of the SVM schemes of post-fault PWM rectifiers. As described in [27], the temperature T_c of the capacitor, which is important for the working life of the capacitor, is determined from the power dissipation on the capacitor, as caused by the capacitor RMS current i_{cRMS}:

$$T_c=T_a+i_{cRMS}^2R_{ESR}R_{th} \tag{22}$$

where T_a is the ambient temperature, R_{ESR} denotes the equivalent series resistance, and R_{th} denotes the thermal resistance between the capacitor and the ambient temperature. Therefore, the RMS capacitor current of each SVM scheme is of paramount importance for extending the lifetime of a capacitor.

In normal 6-switch rectifiers, the capacitor voltages are almost constant. Thus, only high-frequency harmonic currents flow through the capacitors. High-frequency capacitor currents can be alleviated by proper distributions of the zero vectors 000 and 111 [27]-[30]. However, in the proposed post-fault rectifier, faulty phase currents flow directly into the midpoint of the capacitor, leading to periodically fluctuated capacitor voltages. Therefore, the capacitor currents in post-fault rectifiers have fundamental component that cannot be eliminated by modulation schemes, while the high-frequency components are affected by the equivalent zero vectors. According to Table I, the capacitor currents are varied under various basic voltage vectors. With different combinations of the voltage vectors, the three SVM

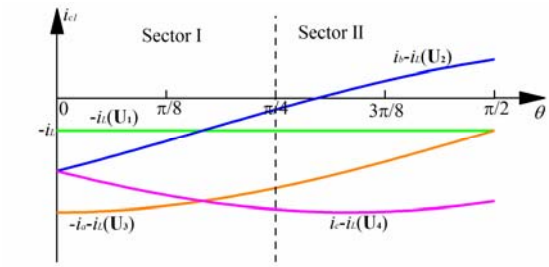


Fig. 10. Components of capacitor current when $\theta \in [0,\pi/2]$.

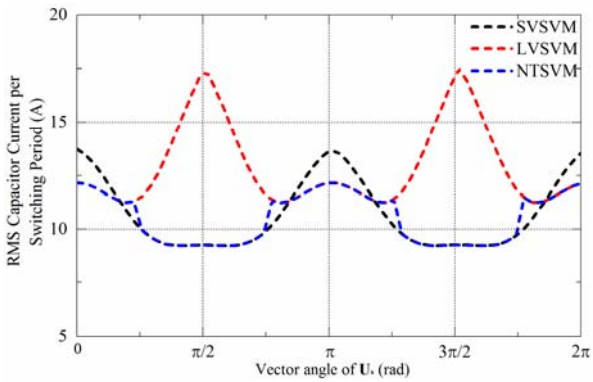


Fig. 11. RMS value of capacitor current over one switching period.

schemes provide different capacitor current performances for post-fault PWM rectifiers, as shown in Fig. 4. Compared with the common mode voltage characteristic, the influence of voltage vectors on the capacitor current is more sophisticated, since the three-phase line currents are time-variant and lead to a polytopical wave shape of the capacitor current, as shown in Fig. 10. For example, the reference vector $\mathbf{U_s}^*$ should be synthesized by two effective vectors $\mathbf{U_1}$ and $\mathbf{U_2}$ at $\theta \in [0,\pi/2]$, which implies that the capacitor current components $-i_L$ and i_b-i_L produced by $\mathbf{U_1}$ and $\mathbf{U_2}$ always exist. Meanwhile, the remaining parts of the capacitor current produced by the equivalent zero vectors ultimately determine the total performance of the capacitor current stress due to the different approaches of zero vector synthesis. As shown in Fig. 10, the amplitude of (i_c-i_L) is smaller than that of (-i_a-i_L) at the beginning of Sector I, i.e., the voltage vector $\mathbf{U_4}$ is better than $\mathbf{U_3}$ for capacitor current stress reduction in this region. In other words, the LVSVM implementing $\mathbf{U_4}$ is preferable to the SVSVM implementing $\mathbf{U_3}$ in this area. Nevertheless, with an increasing θ, the amplitude of (i_c-i_L) reaches and exceeds that of (-i_a-i_L). Thus, the SVSVM becomes favorable.

Due to the symmetry of the capacitor current, an analysis of the capacitor current during the first half of a switching period can be the focus of the study. Thus, the capacitor current RMS over a subcycle can be calculated using:

$$i_{cRMS} = \sqrt{\frac{2}{T_S}\int_0^{T_s/2} {i_{c1}}^2 dt} \tag{23}$$

Substitute the capacitor current listed in Table I into Equ. (23) so that the capacitor current RMS of the three SVM

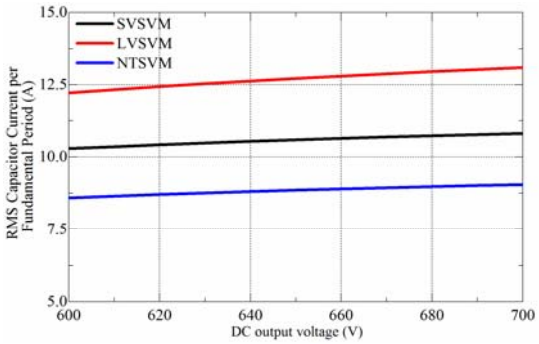


Fig. 12. RMS value of capacitor current during a fundamental period.

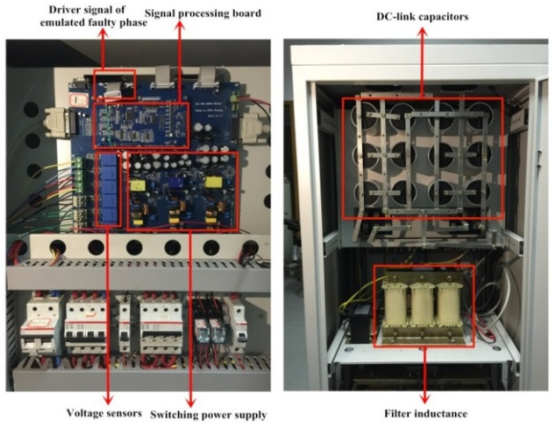


Fig. 13. Experimental prototype.

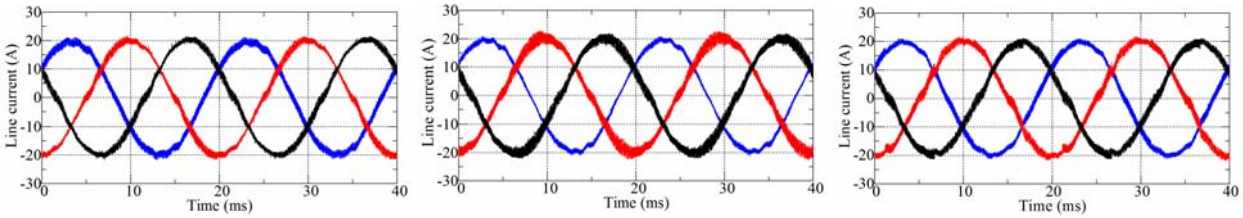
schemes in each switching period can be obtained as:

$$i_{cRMSSV} = \frac{I_m}{2v_o}\sqrt{2v_o^2\cos^2\theta + \sqrt{3}U_m v_o\left|\sin\theta\right|(3-4\cos^2\theta) - 9U_m^2} \tag{24}$$

$$i_{cRMSLV} = \frac{I_m}{2v_o}\sqrt{3v_o^2 + 3U_m v_o\left|\cos\theta\right|(3-4\cos^2\theta) - 2\cos^2\theta - 9U_m^2} \tag{25}$$

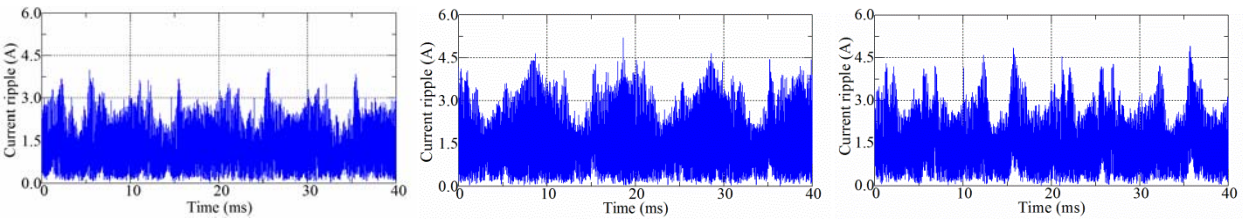
$$i_{cRMSNT} = \begin{cases} i_{cRMSLV}, \mathbf{U_s}^* \text{ in Sector I and III} \\ i_{cRMSSV}, \mathbf{U_s}^* \text{ in Sector II and IV} \end{cases} \tag{26}$$

In connection with Eqns. (24)-(26), there is an initial approximation (calculated by only considering the line current fundamentals) during the deduction. Moreover, the fundamentals of the line currents are assumed to be constant within a switching period. According to Eqns. (24)-(26), Fig. 11 shows the capacitor current RMS over a switching period with θ ranging from 0 to 2π. Unlike the current ripple and CMV characteristics, the capacitor current RMS of the SVSVM is either larger or smaller than that of the LVSVM when the reference voltage vector $\mathbf{U_s}^*$ rotates in the α-β plane, which agrees with the above analysis. The NTSVM possesses two types of zero vector synthesis methods in alternative sectors. This avoids the peak values of the capacitor current RMS in both the SVSVM and LVSVM. For a more in-depth investigation, the capacitor current RMS over a fundamental



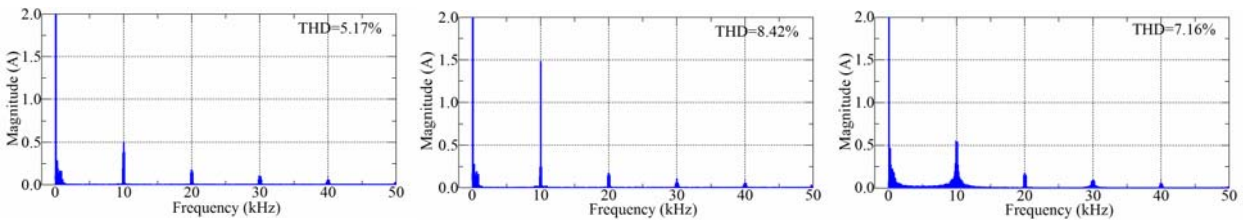
(a) (b) (c)

Fig. 14. Experimental results of line currents: (a) SVSVM; (b) LVSVM; (c) NTSVM.



(a) (b) (c)

Fig. 15. Experimental results of three-phase current ripple: (a) SVSVM; (b) LVSVM; (c) NTSVM.



(a) (b) (c)

Fig. 16. FFT analysis results of line current phase B: (a) SVSVM; (b) LVSVM; (c) NTSVM.

period is deduced by:

$$I_{cRMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{cRMS}^2 d\theta} \tag{27}$$

Thus, the analytical expressions of the three SVM schemes are given as follows:

$$I_{cRMSSV} = \frac{\sqrt{3}I_m}{6v_o}\sqrt{3v_o^2 + \frac{10\sqrt{3}v_o U_m^*}{\pi} - 27U_m^{*2}} \tag{28}$$

$$I_{cRMSLV} = \frac{I_m}{2v_o}\sqrt{2v_o^2 - \frac{2v_o U_m^*}{\pi} - 9U_m^{*2}} \tag{29}$$

The relationship between the capacitor current stress and the DC voltage for the three SVM schemes is clearly shown in Fig. 12. Evidently, a lower DC link voltage can suppress the RMS value of the capacitor current to a limited degree in the linear modulation range. Moreover, this figure also shows that the most effective approach for capacitor current reduction is to select the NTSVM, since it uses two switching sequences in different regions alternatively. When implementing the NTSVM in a post-fault PWM rectifier, the current stress of the capacitor can be reduced, so that the lifetime of the capacitor can be extended. In other words, the reliability of a post-fault rectifier is improved by the NTSVM when the capacitor current stress is considered to be a major concern.

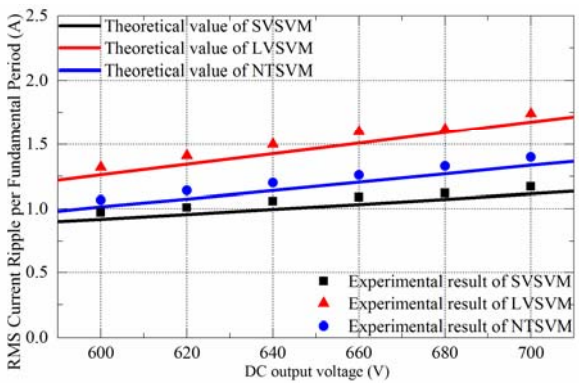
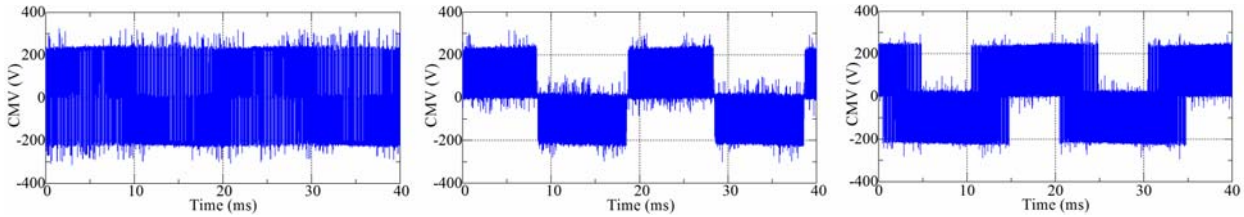


Fig. 17. Experimental results of RMS current ripple over a fundamental period.

VII. Experimental Results

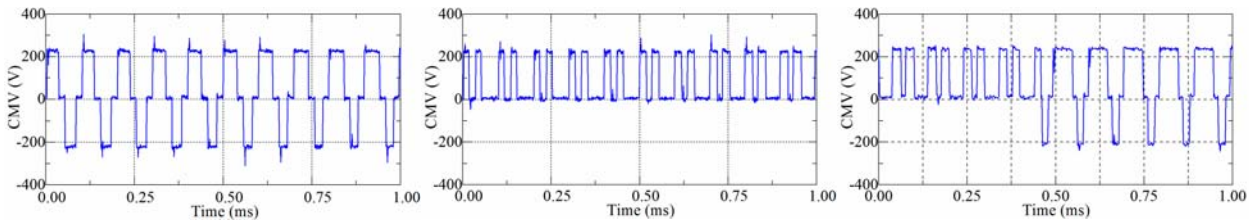
To verify the performances of the three SVM schemes for the post-fault rectifiers, an experimental prototype based on a digital signal processor TMS320F2808 is established, as shown in Fig. 13. The IGBT driver signal of phase A is removed to emulate an open-circuit fault. The experimental parameters are listed in the Appendix.

$$I_{cRMSNT} = \frac{\sqrt{3}I_m}{12}\sqrt{3(2\pi - 1 - \frac{2}{\pi})v_o^2 + (6\sqrt{2} - \frac{14\sqrt{6}}{\pi})v_o U_m^* - 27(\pi + 1)U_m^{*2}} \tag{30}$$



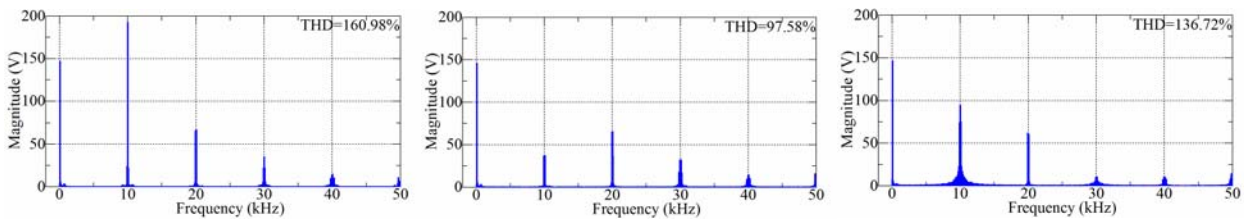
(a) (b) (c)

Fig. 18. Experimental results of common mode voltage during 2 fundamental periods: (a) SVSVM; (b) LVSVM; (c) NTSVM.



(a) (b) (c)

Fig. 19. Experimental results of common mode voltage during 5 switching periods: (a) SVSVM; (b) LVSVM; (c) NTSVM.



(a) (b) (c)

Fig. 20. FFT analysis results of common mode voltage: (a) SVSVM; (b) LVSVM; (c) NTSVM.

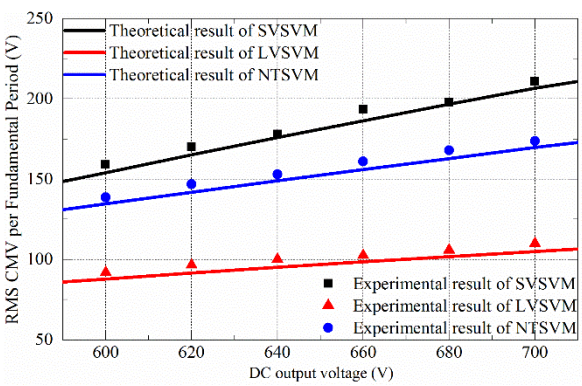


Fig. 21. Experimental results of RMS CMV over a fundamental period.

The experiment was first performed at a DC voltage of 700 V. Figs. 14 and 15 display experimental results for the line currents and current ripples of the three SVM schemes. It is clear that faulty phase currents have unique harmonic distortions compared to the other two phase currents. The current ripple when using the LVSVM is found to be the largest, whereas the current ripple is the smallest when the SVSVM is used. The experimental result of the current ripple corresponds well with the analytical result, verifying the effectiveness of the proposed analysis method. FFT analysis results for the phase current i_b of the three SVM schemes are also provided in Fig. 16 to further validate the relationship between the current ripple and the current harmonic distortion. The SVSVM possesses the least current harmonics around the switching frequency, whereas the high frequency current harmonics of the LVSVM are the largest. The THD of the line currents using the SVSVM, LVSVM and NTSVM are 5.17%, 8.42%, and 7.16%, respectively. This shows that the current ripple can accurately describe the content of the current harmonics. Moreover, with an identical output power, the test is also conducted under DC voltages of 600, 620, 640 and 680 V. The current ripple RMS over a fundamental period with different DC voltages are calculated and presented in Fig. 17. As shown in this figure, decreasing the DC voltage can suppress current ripple. In addition, the SVSVM produces the least current ripple regardless of the DC voltage, which is favorable for line current harmonic reduction.

Figs. 18-20 display experimental results for the common mode voltages of post-fault rectifiers using the three SVM schemes. As noted above, the common mode voltage of the LVSVM over one switching period only has the unipolar nonzero state along with the zero state, as shown in Fig. 19(a). Meanwhile, the common mode voltage of the SVSVM during one switching period has bipolar nonzero states as shown in Fig. 19(b). This restricts the duration time of the zero states. The NTSVM uses two sequences alternatively during a fundamental period, as shown in Fig. 19(c). Thus, the

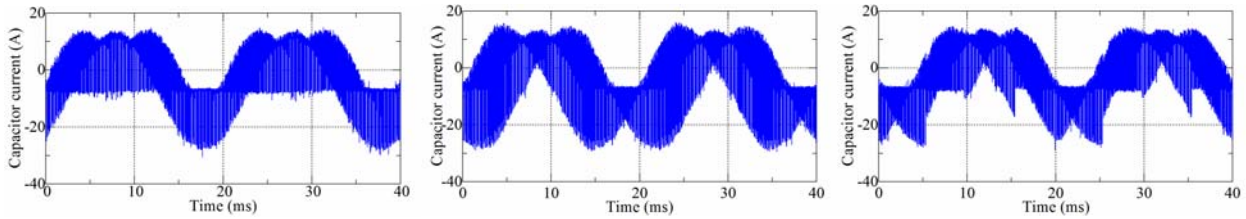


Fig. 22. Experimental results of the capacitor current during 2 fundamental periods: (a) SVSVM; (b) LVSVM; (c) NTSVM.

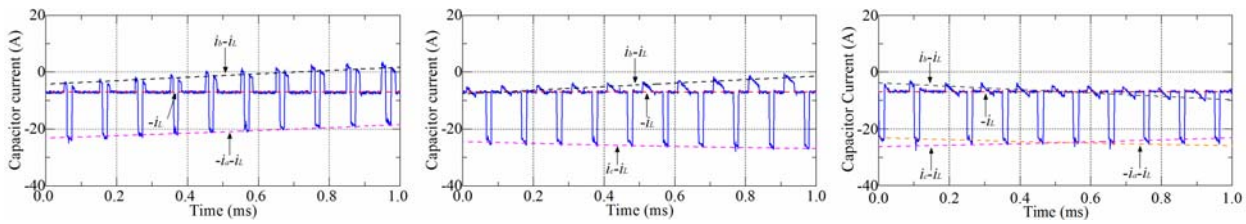


Fig. 23. Experimental results of the capacitor current during 5 switching periods: (a) SVSVM; (b) LVSVM; (c) NTSVM.

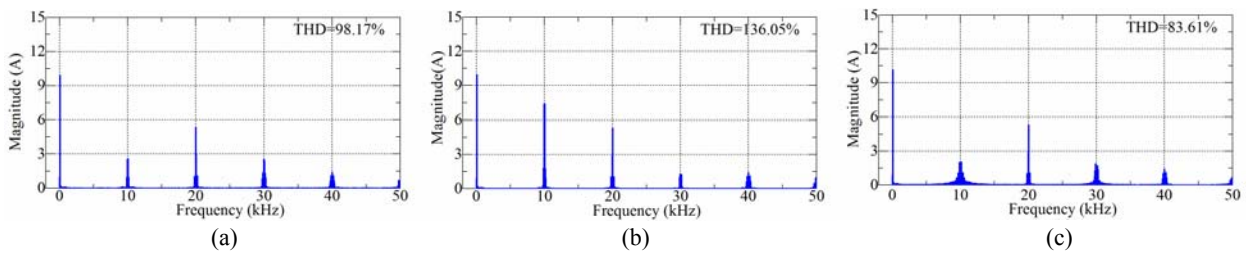


Fig. 24. FFT analysis results of the capacitor current: (a) SVSVM; (b) LVSVM; (c) NTSVM.

common mode voltage of the LVSVM has more zero states than the SVSVM and NTSVM, enabling more implementations of the vectors $\mathbf{U_2}$ and $\mathbf{U_4}$. Consequently, the CMV RMS of the LVSVM over a fundamental period is the minimum among the three SVM schemes. This is also supported by the FFT analysis results in Fig. 20. Similarly, the fundamental component of the common mode voltage is 150 V when each of the SVM schemes is implemented. This shows that different equivalent zero vectors have no influences on the fundamental components of the CMV. However, the switching harmonic contents of the common mode voltage are significantly different when the three SVM schemes are implemented. The SVSVM produces the most switching harmonics of the CMV, whereas the LVSVM produces the least switching harmonics of the CMV. As a result, the THD of the CMV for the SVSVM, LVSVM and NTSVM are 160.98%, 97.58% and 136.72%, respectively. The experimental results verify that the LVSVM produces the least RMS value of the CMV, when considering the positive relations between the THD and RMS values [22]. The RMS values of the CMV during a fundamental period are calculated to further validate the analysis, as show in Fig. 21. The figure clearly demonstrates that the minimum CMV is achieved by using the LVSVM schemes, regardless of the DC voltage value. In contrast, the SVSVM produces the largest CMV, for the zero vectors are synthesized by $\mathbf{U_1}$ and $\mathbf{U_3}$ in

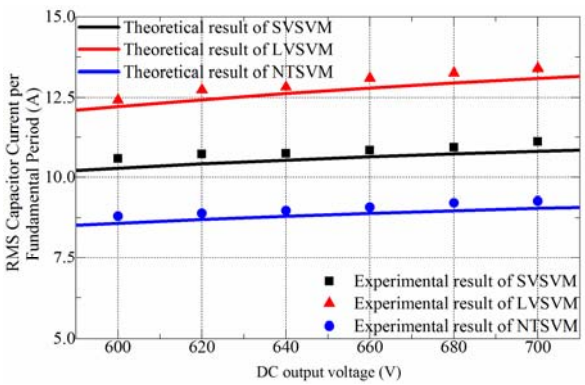


Fig. 25. Experimental results of RMS capacitor current over a fundamental period

SVSVM, which limits the use of $\mathbf{U_2}$ and $\mathbf{U_4}$. The CMV performance of NTSVM falls between those of LVSVM and SVSVM, as in the case of the current ripple performance.

The capacitor currents of post-fault rectifiers using the three SVM schemes are shown in Fig. 22-24. The shapes of the capacitor currents using the different SVM schemes are varied, producing different current stresses to the DC capacitors. In Fig. 23(a), the capacitor current is clearly composed of the components of $-i_L$, $(i_b\text{-}i_L)$, and $(-i_a\text{-}i_L)$. This indicates that $\mathbf{U_1}$, $\mathbf{U_2}$ and $\mathbf{U_3}$ are implemented in the SVSVM. In contrast, in Fig. 23(b), the capacitor current consists of the components of $-i_L$, $(i_b\text{-}i_L)$, and $(i_c\text{-}i_L)$. This indicates that $\mathbf{U_1}$,

TABLE III
PERFORMANCE COMPARISON OF VARIOUS SVM SCHEMES

	SVSVM	LVSVM	NTSVM
Line current harmonic distortion	low	high	medium
Common mode voltage	high	low	medium
Capacitor current stress	medium	high	low

$\mathbf{U_2}$ and $\mathbf{U_4}$ are implemented in the LVSVM.

As shown in Fig. 23(c), the capacitor current of the NTSVM presents two types of shapes due to the alternative use of the switching sequences. FFT analysis results are also provided in Fig. 24. The fundamental components of the capacitor currents using the three different SVM schemes are always 9.88A. This shows that the equivalent zero vectors have no influences on the fundamental components of the capacitor currents. However, the switching frequency harmonic contents are quite different. The THDs of the capacitor current when using the SVSVM, LVSVM and NTSVM are 98.17%, 136.05% and 83.61%, respectively. This demonstrates that the NTSVM produces the least current stress to the capacitors due to the positive correlation between the THD and RMS values of the capacitor current. The RMS values of the capacitor current with various DC voltage values are presented in Fig. 25. In this figure, the NTSVM shows superior performance in capacitor current reduction, whereas the other two methods are not comparable. The experimental result supports the theoretical analysis in Section V, which indicates that the NTSVM can effectively reduce the current stress of the capacitor.

VIII. CONCLUSION

This paper investigated the performance characteristics of the three most commonly used SVM schemes for post-fault PWM rectifiers, aiming to provide a modulation strategy selection criterion for improving system reliability in post-fault operation. An analytical method is utilized to obtain the line current harmonic distortion, common mode voltage and capacitor current stress characteristics for the three SVM schemes. The theoretical results are supported by experimental results, indicating that the analytical method proposed in this paper is an effective approach for SVM scheme evaluation.

The results of this study illustrate the performance characteristics of the three SVM schemes, as listed in Table III. The SVSVM produces the least line current harmonic distortion, whereas the LVSVM produces the most line current harmonic distortion. Regarding the common mode voltage characteristic, the LVSVM becomes favorable for the most frequently used vectors that generate zero states in the common mode voltage: $\mathbf{U_2}$ and $\mathbf{U_4}$. On the other hand, the SVSVM produces the largest RMS value of the common mode voltage due to its restricted use of the vectors $\mathbf{U_2}$ and $\mathbf{U_4}$. The NTSVM produces the minimum capacitor current stress, which is beneficial to the lifetime of DC link capacitors. According to the proposed research results, improved reliability of post-fault PWM rectifiers can be achieved when each of the aforementioned performance characteristics is taken as a priority.

APPENDIX

TABLE IV
PARAMETERS OF THE PROPOSED POST-FAULT RECTIFIER

Grid voltage magnitude E_m	150 V
Grid current magnitude I_m	20 A
Fundamental frequency f	50 Hz
Filter inductance L	3 mH
DC capacitance C_1/C_2	3600 μF
Switching period T_s	1e-4 s

REFERENCES

[1] Y. Shaoyong, A. Bryant, P. Mawby, X. Dawei, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 3, pp. 1441-1451, May/Jun. 2011.

[2] C. B. Jacobina, R. L. de Araujo Ribeiro, A. M. N. Lima, and E. R. C. Da Silva, "Fault-tolerant reversible AC motor drive system," *IEEE Trans. Ind. Appl.*, Vol. 39, No. 4, pp. 1077-1084, Jul./Aug. 2003.

[3] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations," *IEEE Trans. Power Electron.*, Vol. 19, No. 4, pp. 1108-1116, Jul. 2004.

[4] Z. Wenping, X. Dehong, P. N. Enjeti, L. Haijin, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6319-6331, Dec. 2014.

[5] H. W. Van der Broeck and J. D. Van Wyk, "A comparative investigation of a three-phase induction machine drive with a component minimized voltage-fed inverter under different control options," *IEEE Trans. Ind. Appl.*, Vol. IA-20, No. 2, pp. 309-320, Mar. 1984.

[6] K. Gi-Taek and T. A. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," *IEEE Trans. Ind. Appl.* Vol. 32, No. 6, pp. 1331-1337, Nov./Dec. 1996.

[7] C. Zhang, J. Zheng, J. Mei, K. Deng, and F. Zhou, "Control method for fault-tolerant active power filters," *Journal of Power Electronics*, Vol. 15, No. 3, pp. 796-805, May 2015.

[8] L. Pan, H. Sun, B. Wang, G. Su, X. Wang, and G. Peng, "Torque ripple suppression method for BLDCM drive based on four-switch three-phase inverter," Vol. 15, No. 4, pp. 974-986, Jul. 2015.

[9] D. Zhou, J. Zhao, and Y. Liu, "Predictive torque control scheme for three-phase four-switch inverter-fed induction motor drives with DC-link voltage offset suppression," IEEE Trans. Power Electron., Vol. 30, No. 6, pp. 3309-3318, Jun. 2015.

[10] F. Blaabjerg, S. Freysson, H. H. Hansen, and S. Hansen, "A new optimized space-vector modulation strategy for a component-minimized voltage source inverter," *IEEE Trans. Power Electron.*, Vol. 12, No. 4, pp. 704-714, Jul. 1997.

[11] M. Beltrao De Rossiter Correa, C. B. Jacobina, E. R. Cabral Da Silva, and A. M. N. Lima, "A general PWM

strategy for four-switch three-phase inverters," *IEEE Trans. Power Electron.*, Vol. 21, No. 6, pp. 1618-1627, Nov. 2006.
[12] Q. T. An, L. Sun, K. Zhao, and T. M. Jahns, "Scalar PWM algorithms for four-switch three-phase inverters," *Electronics Letters,* Vol. 46, No. 13, pp. 900-902, Jun. 2010.
[13] L. Tzann-Shin and L. Jia-Hong, "Modeling and control of a three-phase four-switch PWM voltage-source rectifier in d-q synchronous frame," *IEEE Trans. Power Electron.*, Vol. 26, No. 9, pp. 2476-2489, Sep. 2011.
[14] W. Rui, Z. Jin and L. Yang, "A comprehensive investigation of four-switch three-phase voltage source inverter based on double fourier integral analysis," *IEEE Trans. Power Electron.*, Vol. 26, No. 10, pp. 2774-2787, Oct. 2011.
[15] W. Wen, L. An, X. Xianyong, F. Lu, M. C. Thuyen, and L. Zhou, "Space vector pulse-width modulation algorithm and DC-side voltage control strategy of three-phase four-switch active power filters," *IET Power Electronics*, Vol. 6, No. 1, pp. 125-135, Jan. 2013.
[16] N. M. A. Freire and A. J. Marques Cardoso, "A fault-tolerant direct controlled PMSG drive for wind energy conversion systems," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 2, pp. 821-834, Feb. 2014.
[17] K. Jaehong, H. Jinseok and N. Kwanghee, "A current distortion compensation scheme for four-switch inverters," *IEEE Trans. Power Electron.*, Vol. 24, No. 4, pp. 1032-1040, Apr. 2009.
[18] W. Zhou, and D. Sun, "Adaptive PWM for four-switch three-phase inverter", *Electronics Letters*, Vol. 51, No. 21, pp. 1690-1692, Oct. 2015.
[19] "IEEE standard for interconnecting distributed resources with electric power systems," in *IEEE Std 1547-2003*, 2003, pp. 1-28.
[20] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Theoretical and experimental analysis for the RMS current ripple minimization in induction motor drives controlled by SVM technique," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 5, pp. 1056-1065, Oct. 2004.
[21] D. Dujic, M. Jones and E. Levi, "Analysis of output current-ripple RMS in multiphase drives using polygon approach," *IEEE Trans. Power Electron.*, Vol. 25, No. 7, pp. 1838-1849, Jul. 2010.
[22] O. Dordevic, M. Jones and E. Levi, "Analytical formulas for phase voltage RMS squared and THD in PWM multiphase systems," *IEEE Trans. Power Electron.,* Vol. 30, No. 3, pp. 1645-1656, Mar. 2015.
[23] F. Wu, B. Sun, K, Zhao, and L. Sun, "Analysis and solution of current zero-crossing distortion with unipolar hysteresis current control in grid-connected inverter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 10, pp. 4450-4457, Oct. 2012.
[24] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1971-1979, Apr. 2013.
[25] A. M. Hava and E. Un, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 241-252, Jan. 2009.
[26] D. Barater, G. Buticchi, E. Lorenzani, and C. Concari, "Active common-mode filter for ground leakage current reduction in grid-connected PV converters operating with arbitrary power factor," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 8, pp. 3940-3950, Aug. 2014.
[27] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *Electric Power Applications, IEE Pro.,* Vol. 153, No. 4, pp. 535-543, Jul. 2006.
[28] J. Hobraiche, J. P. Vilain, P. Macret, and N. Patin, "A new PWM strategy to reduce the inverter input current ripples," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 172-180, Jan. 2009.
[29] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 5, pp. 1851-1859, Sep./Oct. 2009.
[30] W. Huai and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters——an overview," *IEEE Trans. Ind. Appl.*, Vol. 50, No. 5, pp. 3569-3578, Sep./Oct. 2014.

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