JPE 16-6-15

http://dx.doi.org/10.6113/JPE.2016.16.6.2139
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Cascaded Modular Multilevel Inverter Topology Using Novel Series Basic Units with a Reduced Number of Power Electronic Elements

Reza Barzegarkhoo[†], Naser Vosoughi[*], Elyas Zamiri[*], Hossein Madadi Kojabadi[**], and Liuchen Chang[***]

[†,**]Faculty of Electrical Engineering, Sahand University of Technology (SUT), Tabriz, Iran
[*]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran
[***]Department of Electrical and Computer Engineering, University of New Brunswick, Fredericton, Canada

Abstract

In this study, a new type of cascaded modular multilevel inverters (CMMLIs) is presented which is able to produce a considerable number of output voltage levels with a reasonable number of components. Accordingly, each series stage of the proposed CMMLI is comprised of two same basic units that are connected with each other through two unidirectional power switches without aiming any of the full H-bridge cells. In addition, since the potentiality for generating a higher number of output voltage levels in CMMLIs hinges on the magnitude of the dc voltage sources used in each series unit, in the rest of this paper, four different algorithms for determining an appropriate value for the dc sources' magnitude are also presented. In the following, a comprehensive topological analysis between some CMMLI structures reported in the literature and proposed structure along with several simulation and experimental results will be also given to validate the lucrative benefits and viability of the proposed topology.

Key words: Cascade multilevel inverter, Determination of dc voltage sources, Modular multilevel inverter topologies, Reduced number of components.

I. INTRODUCTION

In the field of industrial power electronic utilities, multilevel voltage source inverters (MLVSIs) offer the promising potential for use in medium and high power applications due to their various salient features such as low voltage stresses on switches, low total harmonic distortion (THD) of the output waveforms, no need for large output filters or transformers, and low cost [1]-[10].

In general there are three types of MLVSIs. These are the diode clamp MLVSIs [5], flying capacitor MLVSIs [6]-[8] and cascaded H-bridge MLVSIs [9], [10]. However, these conventional types always suffer from requiring a large number of power electronic components, isolated dc voltage sources and charge balancing control procedures which can increase the overall operating and maintenance costs. Nowadays, in order to alleviate the above-mentioned limitations, many structures have been presented in the literature. They have addressed the elevation of the output voltage levels through the minimization of the overall costs by regarding the basic concept of MLVSIs. Hence, several new basic units were suggested which can work as a level creator sub-unit. These proposed basic units are connected to a full H-bridge unit for changing the voltage polarity of the output waveform and then these modules are cascaded with each other in series form to generate multiple output voltage levels [11]-[19]. In addition, cascaded connection of series basic units offers the modularity property which can reinforce the reliability and flexibility of system.

Since cascaded modular multilevel inverters (CMMLI) can typically generate any desired number of higher output voltage levels, the value of the dc voltage sources which can be provided from several renewable energy resources (REs)

Manuscript received Sep. 7, 2015; accepted Sep. 2, 2016
Recommended for publication by Associate Editor Rae-Young Kim.
[†]Corresponding Author: barzegar_sina@yahoo.com.au
Tel: +98 41 2344 3801, Sahand University of Technology (SUT)
[*]Faculty of Electrical and Computer Eng., University of Tabriz, Iran
[**]Faculty of Electrical Eng., Sahand Univ. of Technology (SUT), Iran
[***]Dept. of Electrical & Computer Eng., Univ. of New Brunswick, Canada

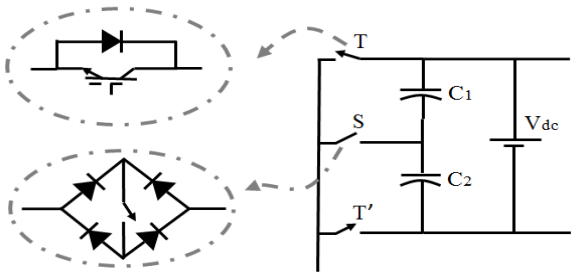


Fig. 1. Proposed basic unit.

can be chosen to be either symmetric or asymmetric. In the symmetric structures, the magnitudes of the dc voltage sources are same. Therefore, the variety of isolated dc voltage sources is low which makes them more suitable for cost effective power electronic applications [12], [20], [21].

On the other hand, these dc voltage values can be selected to be different in the asymmetric configurations. In this case, although the variety of isolated dc voltage sources is high, the number of generated output voltage levels is a lot more than the symmetric structures which attempts to achieve a better power quality through a lower value of the THD and a reduced number of power electronic elements [22]-[26]. Nevertheless, using an additional full H-bridge unit in the new developed MLVSIs usually leads to an increase in the number of power switches and in the maximum number of current path components which can enhance the total conduction loss and degrade the overall efficiency thereby.

The aim of this paper is to reduce the overall component count of CMMLIs through presenting a novel topology which does not need a conventional full H-bridge cell for changing the output voltage polarity and can improve the flexibility of the system by the contribution of the capacitive divider technique applied on the dc-links.

Therefore, the rest of this study is organized as follows. At first, a new basic modular MLVSI topology is presented which is comprised of six unidirectional and two bi-directional power switches, two isolated dc voltage sources and four capacitors as the dc link energy sharing elements in the power circuit. In this case, the four utilized capacitors are charged and discharged frequently during the positive and negative half cycles of the output waveform by power supply self-voltage balancing. Meanwhile, the suggested topology does not contain any full H-bridge cells.

After that, to increase the number of output voltage levels with the smallest number of switches and other accompanying components, the proposed CMMLI is presented. It offers a modular structure and a lower component count than many of the recently presented topologies. Section III also presents four different algorithms in order to determine the proper magnitude for the dc voltage sources used in each series unit of the proposed CMMLI. Moreover, to corroborate the advantages of the proposed CMMLI in contrast to other recently presented structures, a comprehensive comparison from different aspects under fair conditions has been conducted in section IV. To confirm the effectiveness of proposed topology, several results obtained from experimental tests and a computer simulation platform done by PSCAD/EMTDC software are presented in section V. Finally, some conclusions are presented in section IV.

II. PROPOSED MLVSI TOPOLOGY

The main component of the proposed modular MLVSI topology named as the proposed basic unit is shown in Fig. 1. As can be seen, the proposed basic unit consists of one dc voltage source, two capacitors as dc link energy sharing elements, and one bi-directional and two unidirectional power switches which should be triggered by complementary operations to avoid short circuit problems. In this case, the bi-directional power switch can be substituted by one ordinary power switch and four power diodes to undertake the conduction of the reverse current in both directions.

In order to demonstrate the operating modes of the proposed basic unit, the current flow path of four passible output voltage states are illustrated in Fig. 2(a)-(d). According to Fig. 2(a) and (b), when either the switch of T or T' is turned ON and S becomes OFF, the voltage of the dc source ($+V_{dc}$ or $-V_{dc}$) is transferred to the output. At this stage, none of the dc link capacitors enter into the current path and as a result both of them are directly charged by power supply.

In addition, according to Fig. 2(c) and (d), when S becomes ON and switches T or T' become OFF, the across voltage of C_1 or C_2 is pumped to the output. Here, when the across voltage of one supposed capacitor (C_1 or C_2) is being pumped to the output, another capacitor is directly charged by the power supply.

The proposed MLVSI topology shown in Fig. 3(a) is made by the contribution of the introduced basic unit. Here, to create an optimum structure of a MLVSI in terms of having the lowest number of switching devices with greatest number of generated output voltage levels, two same basic units with opposite polarities are used in the proposed overall structure instead of using a full H-bridge unit in the front of the proposed basic unit. Table I indicates the seventeen different ON switching states of the proposed topology in which C and D stand for the charging and discharging modes of the capacitors, respectively. In addition, $V_{C1,L}$, $V_{C2,L}$, $V_{C1,R}$ and $V_{C2,R}$ are the across voltages of the capacitors $C_{1,L}$, $C_{2,L}$, $C_{1,R}$ and $C_{2,R}$, respectively.

Meanwhile, $V_{dc,L}$ and $V_{dc,R}$ denote the required dc voltage sources located at the left and right side of the circuit, respectively. In this case, to avoid short circuit problems, the

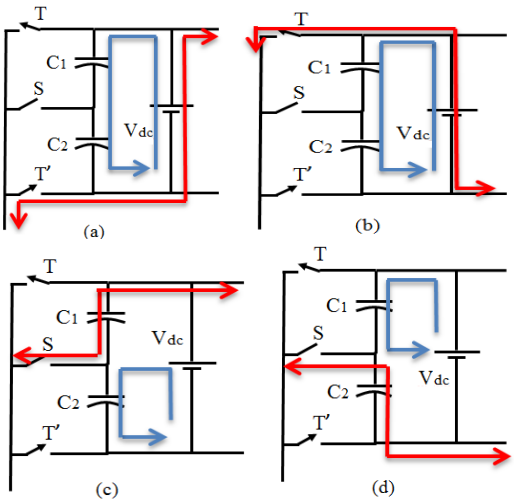


Fig. 2. Different current flow path of operating modes for proposed basic unit when (a) $-V_{dc}$ (b) $+V_{dc}$ (c) across voltage of C_1 (d) across voltage of C_2 is transferred to the output.

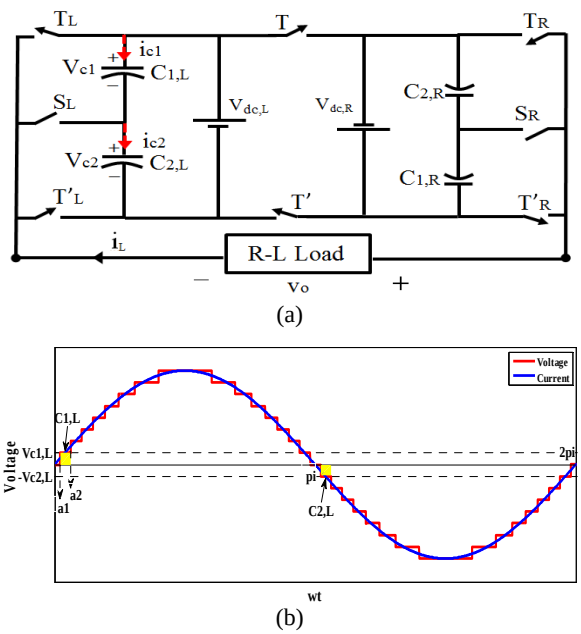


Fig. 3. (a) Proposed MLVSI topology (b) Typical output voltage and current waveforms of proposed topology.

paired switches (T,T'), (T_R,T_R') and (T_L,T_L') should not be turned ON, simultaneously.

Fig. 3(b) shows typical output voltage and current waveforms of the proposed topology based on a 50Hz switching frequency. In this case, two utilized dc voltage sources are assumed to be non-equal and a resistive-inductive load has been connected at the output of the proposed topology.

At this stage, to demonstrate the accurate self-charge balancing operation of capacitors in the proposed topology, the capacitance for all of the capacitors are assumed to be the same and equal to C. Therefore, by considering the time

TABLE I

DIFFERENT SWITCHING AND CAPACITORS' STATES FOR PROPOSED MLVSI

States	ON-STATE SWITCHES	Cap States				v_o
		$C_{1,L}$	$C_{2,L}$	$C_{1,R}$	$C_{2,R}$	
1	(T_L,T,T_R) (T_L',T',T_R')	C	C	C	C	0
2	(S_L,T,T_R)	D	C	C	C	$V_{C1,L}$
3	(T_L',T,T_R)	C	C	C	C	$V_{dc,L}$
4	(T_L,T,S_R)	C	C	C	D	$V_{C2,R}$
5	(S_L,T,S_R)	D	C	C	D	$V_{C1,L}+V_{C2,R}$
6	(T_L',T,S_R)	C	C	C	D	$V_{dc,L}+V_{C2,R}$
7	(T_L,T,T_R')	C	C	C	C	$V_{dc,R}$
8	(S_L,T,T_R')	D	C	C	C	$V_{C1,L}+V_{dc,R}$
9	(T_L',T,T_R')	C	C	C	C	$V_{dc,L}+V_{dc,R}$
10	(S_L,T',T_R')	C	D	C	C	$-V_{C2,L}$
11	(T_L,T',T_R')	C	C	C	C	$-V_{dc,L}$
12	(T_L',T',S_R)	C	C	D	C	$-V_{C1,R}$
13	(S_L,T',S_R)	C	D	D	C	$-V_{C2,L}-V_{C1,R}$
14	(T_L,T',S_R)	C	C	C	D	$-V_{dc,L}-V_{C1,R}$
15	(T_L',T',T_R)	C	C	C	C	$-V_{dc,R}$
16	(S_L,T',T_R)	C	D	C	C	$-V_{C2,L}-V_{dc,R}$
17	(T_L,T',T_R)	C	C	C	C	$-V_{dc,L}-V_{dc,R}$

interval of (α_1,α_2) in Fig. 3(b) and with respect to Table I, the voltage variations of the capacitor $C_{1,L}$ for the first positive step of the output voltage can be expressed as:

$$\underset{<\alpha_1,\alpha_2>}{\Delta V_{C1,L}} = \frac{1}{C}\int_{\alpha_1}^{\alpha_2} i_{C,1L}(t)\,dt = -\frac{1}{C}\int_{\alpha_1}^{\alpha_2} i_L(t)\,dt \qquad (1)$$

where, $i_{C,1L}(t)$ is the passing current of $C_{1,L}$ and $i_L(t)$ is supposed to be a sinusoidal load current which can be expressed as:

$$i_L(t) = I_m \sin(\omega t - \varphi) \qquad (2)$$

where I_m, ω and φ are the amplitude of load current, the angular frequency of the output voltage and the phase difference between the load voltage and the current waveforms, respectively. On the other hand, by applying the Kirchhoff voltage law (KVL) in the left loop of the converter, it is obvious that:

$$V_{C1,L}+V_{C2,L}=V_{dc,L} \qquad (3)$$

Therefore, the voltage variation of the capacitor $C_{2,L}$ is always equal to the opposite value of the voltage variation of the capacitor $C_{1,L}$ or in other words:

$$\Delta V_{C1,L} = -\Delta V_{C2,L} \qquad (4)$$

In addition, by using (4) and according to Fig. 3(b), the

voltage variations of the capacitors for the time interval of $(\alpha_1+\pi,\alpha_2+\pi)$ in the first negative step of the output voltage can be taken by:

$$\underset{<\alpha_1+\pi,\alpha_2+\pi>}{\Delta V_{C1,L}} = -\Delta V_{C2,L} = -\frac{1}{C}\int_{\alpha_1+\pi}^{\alpha_2+\pi} i_{C,2L}(t)\,dt = -\frac{1}{C}\int_{\alpha_1+\pi}^{\alpha_2+\pi} i_L(t)\,dt \quad (5)$$

where, $i_{C,2L}(t)$ is the passing current of $C_{2,L}$. From the sinusoidal assumption of the load current according to (2) and having considered (1) and (5), the voltage variations of $C_{1,L}$ during the generation of the first output voltage level in both the positive and negative half cycles is equal to zero, according to (6):

$$\underset{<\alpha_1,\alpha_2>}{\Delta V_{C1,L}} + \underset{<\alpha_1+\pi,\alpha_2+\pi>}{\Delta V_{C1,L}} = 0 \quad (6)$$

Meanwhile in the first output voltage level in both half cycles, two other capacitors from the right side of the circuit are being charged separately by another dc power supply.

With respect to this analysis, the across voltage of each capacitor is balanced at the initial voltage value in the zero output voltage level which is equal to $\frac{V_{dc}}{2}$.

A similar analysis can be accomplished for each of the output voltage levels and for each of the capacitors. The result of this behavior is that the proposed circuit is able to fix the voltage of the capacitors at the half value of the dc voltage sources since the capacitive divider technique and this operation do not depend on the value or type of loads.

Now, in order to increase the number of output voltage levels and to define the general modular structure, the proposed CMMLI is made according to Fig. 4. In this regard, if n is assumed to be the number of the proposed MLVSI units connected with each other by series connection, the output voltage of the proposed CMMLI can be obtained by:

$$V_O(t) = v_{o,1}(t) + v_{o,2}(t) + \ldots + v_{o,n}(t) \quad (7)$$

In addition, the number of required power switches or required gate drivers and the number of required dc voltage sources, dc-link capacitors and the maximum number of switches in the current path for proposed CMMLI are calculated by the following equations, respectively:

$$N_{Switch} = N_{Driver} = 8n \quad (8)$$

$$N_{Source} = 2n \quad (9)$$

$$N_{Cap} = 4n \quad (10)$$

$$N_{C,\max} = 3n \quad (11)$$

III. Proposed Algorithms to Determine the Magnitude of DC Voltage Sources

In this section, to determine a suitable magnitude for the dc voltage sources of the proposed CMMLI topology, four different passible algorithms are presented. In addition, the number of generated output voltage levels, the maximum value of the output voltage, the variety of the isolated dc voltage sources and the total value of the blocked voltage are calculated for each of them.

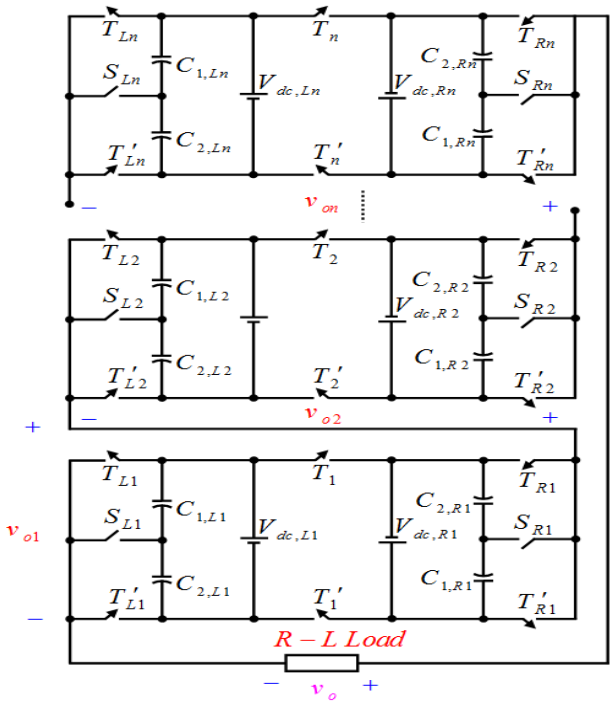


Fig. 4. Proposed CMMLI topology.

A. First Proposed Algorithm

In the first algorithm, the magnitude for all of the dc voltage sources is assumed to be the same (symmetric algorithm) and equal to:

$$V_{dc,Li} = V_{dc,Ri} = 2V_{dc} \quad for(i = 1,2,\ldots,n) \quad (12)$$

It is clear that the variety of isolated dc voltage sources based on the proposed symmetric algorithm is one. Therefore, the number of output voltage levels and the maximum value of the output voltage are expressed as (13) and (14), respectively.

$$N_{level} = 8n + 1 \quad (13)$$

$$V_{o,\max} = 4nV_{dc} \quad (14)$$

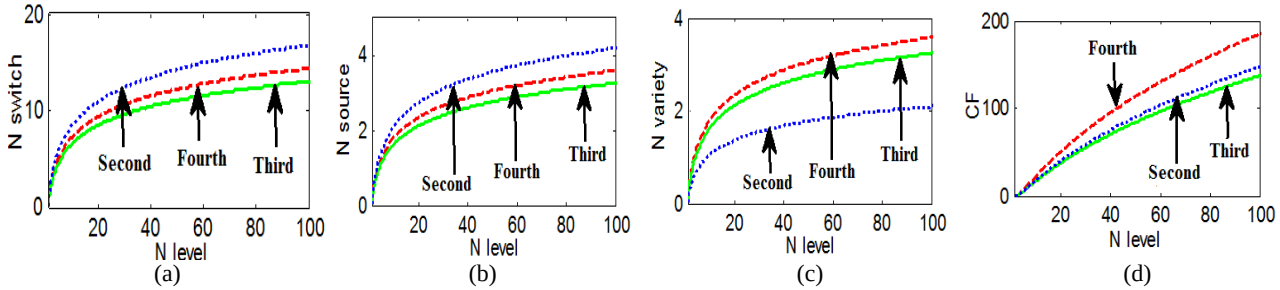
Another critical parameter which usually influences the overall cost function of an inverter is the total value of the maximum blocked voltage across the switches in their OFF state condition. Therefore, this value is calculated by the following equations for all of the involved switches in the proposed CMMLI based on the first proposed method.

$$V_{Block,T_i'} = V_{Block,T_i} = 4V_{dc} \quad (15)$$

$$V_{Block,T'_{Li}} = V_{Block,T_{Li}} = V_{Block,T'_{Ri}} = V_{Block,T_{Ri}} = 2V_{dc} \quad (16)$$

$$V_{Block,S_{Li}} = V_{Block,S_{Ri}} = \pm V_{dc} \quad (17)$$

$$V_{Block} = 2\sum_{i=1}^{n}(V_{Block,T_i} + V_{Block,T_{Li}} + V_{Block,S_{Li}}) = 18nV_{dc} \quad (18)$$



(a) (b) (c) (d)

Fig. 5. Comparisons between three supposed asymmetric algorithms (a) variations of N_{Switch} versus N_{level} (b) variations of N_{Source} versus N_{level} (c) variations of $N_{Variaty}$ versus N_{level} (d) variations of CF versus N_{level}.

B. Second Proposed Algorithm

The second proposed algorithm is dedicated to the binary pattern for the magnitude of the dc voltage sources in each series unit, which can be written according to (19):

$$V_{\mathrm{dc,Ri}} = 2V_{\mathrm{dc},Li} = 2\times 13^{n-1}V_{dc} \quad for(i=1,2,...,n) \tag{19}$$

Hence, the number of output voltage levels, the maximum value of the output voltage, the maximum value of the blocked voltage and the variety of the isolated dc voltage sources are calculated by the following equations:

$$N_{level} = 13^{n} \tag{20}$$

$$V_{o,\max} = \frac{(13^{n}-1)}{2}V_{dc} \tag{21}$$

$$V_{Block} = 9\times(\frac{13^{n}-1}{4})\,\mathrm{V}_{dc} \tag{22}$$

$$N_{Variaty} = 2n \tag{23}$$

C. Third Proposed Algorithm

The magnitude of the dc voltage sources in each series unit of the proposed CMMLI can be adjusted as a trinary pattern in third proposed algorithm, according to (24):

$$V_{\mathrm{dc,Ri}} = 3V_{\mathrm{dc},Li} = 2\times 17^{n-1}V_{dc} \quad for(i=1,2,...,n) \tag{24}$$

The related equations of N_{level}, $V_{o,\max}$, V_{Block} and $N_{Variaty}$ are obtained by the following:

$$N_{level} = 17^{n} \tag{25}$$

$$V_{o,\max} = \frac{(17^{n}-1)}{2}V_{dc} \tag{26}$$

$$V_{Block} = 9\times(\frac{17^{n}-1}{4})\,\mathrm{V}_{dc} \tag{27}$$

$$N_{Variaty} = 2n \tag{28}$$

D. Fourth Proposed Algorithm

In the fourth proposed algorithm, the magnitude of the dc voltage sources used in each unit is adjusted in the symmetric form. These values are different in comparison to the other units in the proposed CMMLI and can be set based on (29):

$$V_{\mathrm{dc,Ri}} = V_{\mathrm{dc},Li} = 2\times 9^{n-1}V_{dc} \quad for(i=1,2,...,n) \tag{29}$$

In this case, the related equations, like those of the other proposed algorithms, are calculated and can be expressed as:

TABLE II

SYMMETRIC COMPARISON BETWEEN PROPOSED CMMLI AND OTHER TOPOLOGIES FOR $N_{level}=25$

	Paramaters				
No. Refs	N_{Switch} & N_{Driver}	N_{Source}	$N_{C,\max}$	V_{Block}	CF
[12]	30	12	12	$54V_{dc}$	1620
[14]	36	6	24	$60V_{dc}$	1080
[20]	26	12	13	$48V_{dc}$	1248
[21]&[25]	36	12	12	$60V_{dc}$	2160
[22]	36	12	24	$48V_{dc}$	1728
First top [26]	28	6	14	$72V_{dc}$	1008
Second top [26]	48	6	24	$72V_{dc}$	1728
Proposed CMMLI	24	6	9	$54V_{dc}$	648

$$N_{level} = 9^{n} \tag{30}$$

$$V_{o,\max} = \frac{(9^{n}-1)}{2}V_{dc} \tag{31}$$

$$V_{Block} = 9\times(\frac{9^{n}-1}{4})\,\mathrm{V}_{dc} \tag{32}$$

$$N_{Variaty} = n \tag{33}$$

At this stage, in order to evaluate the three supposed asymmetric algorithms for the proposed CMMLI topology, variations of the number of required power switches, the number of required dc voltage sources and the variety of isolated dc voltage sources versus different numbers of output voltage levels have been shown on the basis of Fig. 5(a)-(c).

In addition, the consequent above-mentioned parameters which can estimate the overall operating cost of the system are functionalized according to (34). This equation is derived from the defined cost function (CF) presented in [14].

Then its respective variations are shown by Fig. 5(d). Here, the per unit value of the total blocked voltage ($V_{Block}{}^{pu}$) can be denoted by (35).

$$CF = (\mathrm{N}_{Switch})\times(\mathrm{N}_{Source})\times(\mathrm{N}_{Variaty})\times(V_{Block}{}^{pu}) \tag{34}$$

$$V_{Block}{}^{pu} = \frac{V_{Block}}{V_{o,\max}} \tag{35}$$

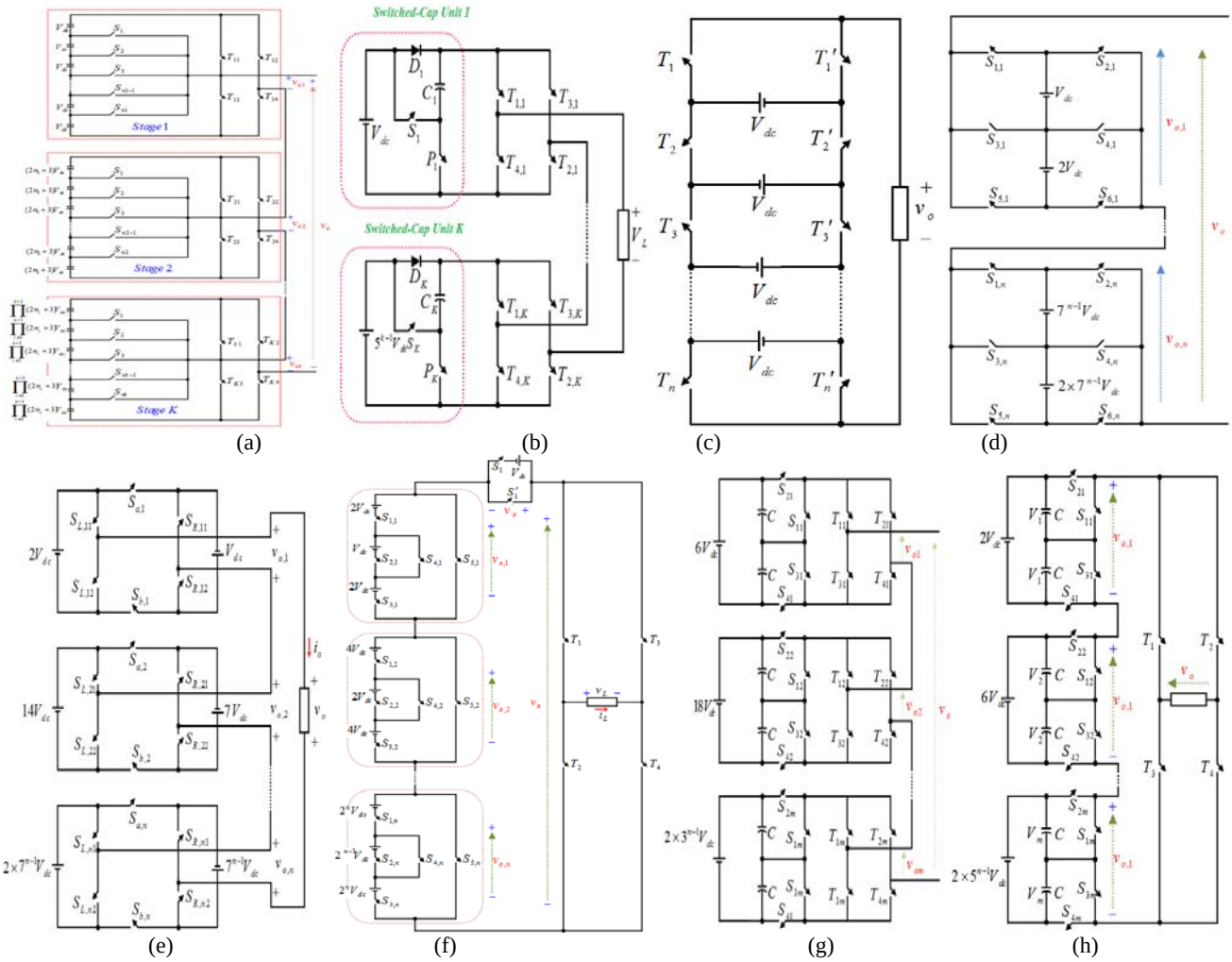


Fig. 6. Suggested CMMLI topologies in (a) Ref [12] (b) Ref [14] (c) Ref [20] (d) Ref [21]&[25] (e) Ref [22] (f) Ref [24] (g) First Top of Ref [26] (h) Second Top of Ref [26].

It should be noted that, the values of the blocked voltages for each of the proposed algorithms, in terms of number of output voltage levels, are always equal to each other and can be written as:

$$V_{Block} = \frac{9\times(N_{level}-1)}{4} \tag{36}$$

By taking these figures into account, it is clear that the third proposed algorithm offers the better condition in contrast to others and since it can minimize the cost, this algorithm would be selected as the main proposed asymmetric structure for the comparison done in the next section.

IV. Comparison Discussion

In this section, the proposed CMMLI is compared with several recently presented MLVSI topologies from the view point of both symmetric and asymmetric conditions. The details of each cited structure in terms of its topological platform, have been depicted in Fig. 6(a)-(h).

A. Symmetric Comparison

In the symmetric comparison, the proposed topology based on the first recommended algorithm is compared with the MLVSIs proposed in [12],[14], [20]-[22], [25] and the two suggested structures in [26] in terms of the number of required power switches or gate drivers, the total value of the blocked voltage, the maximum number of current path components and the number of required dc link voltages for the specific number of output voltage levels ($N_{level}=25$) that can be generated by all of the structures. These comparisons are summarized by Table II which can corroborate the salient advantages of the proposed topology compared to the existing structures in terms of most of the key parameters.

B. Asymmetric Comparison

In this case study, to have fair surveys in comparisons, among the various suggested algorithms to determine the magnitude of dc voltage sources, the best option of each structure is chosen in such a way that the maximum number

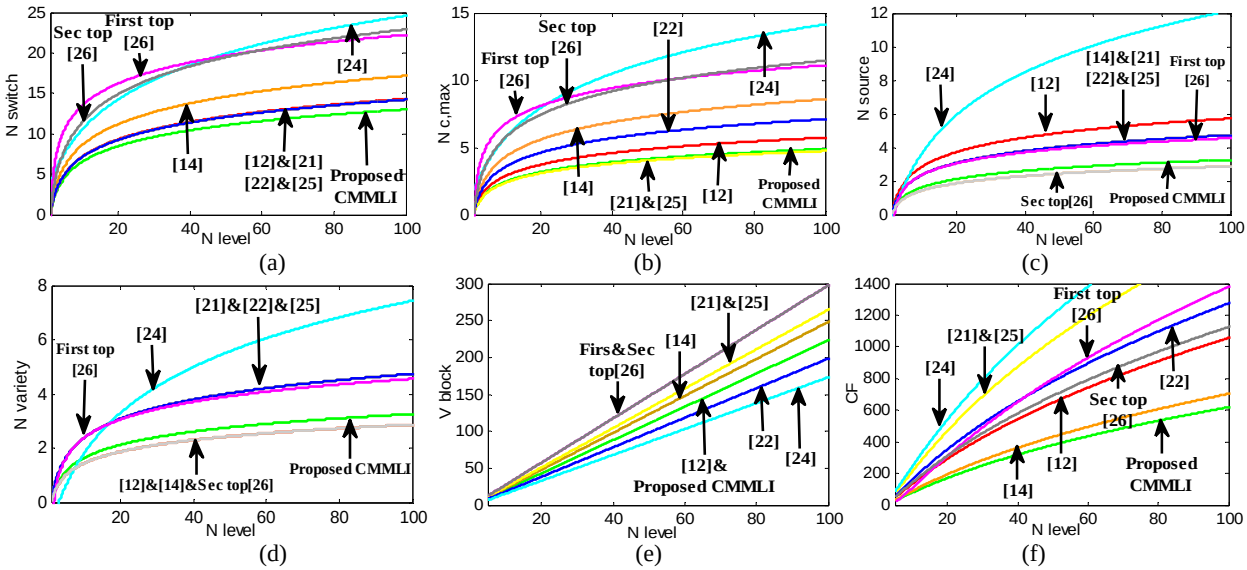


Fig. 7. Asymmetric comparisons (a) variations of N_{Switch} & N_{Driver} versus N_{level} (b) variations of $N_{C,\max}$ versus N_{level} (c) variations of N_{Source} versus N_{level} (d) variations of $N_{Variaty}$ versus N_{level} (e) variations of V_{Block} versus N_{level} (f) variations of CF versus N_{level}.

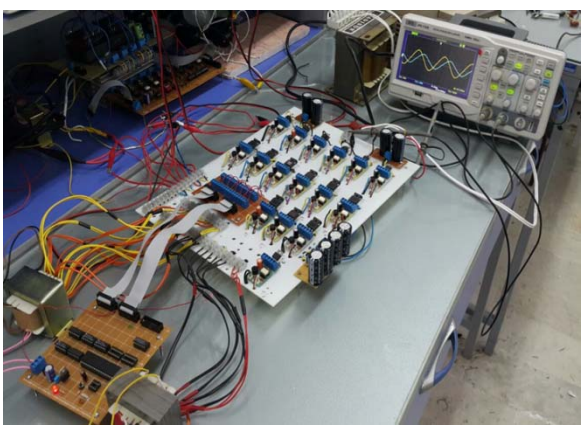


Fig. 8. Laboratory prototype.

of output voltage levels is able to be generated with the least of component counts. For this reason, the fourth proposed algorithm of [24] and ninth proposed algorithm of [22] are selected in this comparison.

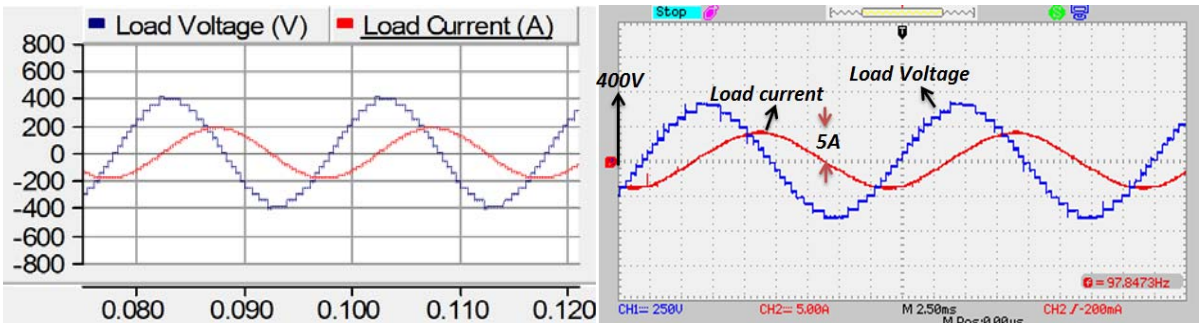
On the basis of the above specifications, Fig. 7(a)-(f) show the variations of the required power switches or gate drivers, the maximum number of load current path components, the number of required dc voltage sources, the variety of isolated dc voltage sources, the maximum value of the total blocked voltage and the overall cost function based on (42) versus the different number of output voltage levels for the proposed asymmetric CMMLI working on the basis of the third presented algorithm and some other existing structures depicted in Fig. 6(a)-(f). From Fig. 7(a) and (b), it is clear that the proposed topology requires the smallest number of power switches and current path components for generating the same number of output voltage levels. In addition, with respect to Fig. 7(c), and (d), it can be understood that the proposed topology possesses acceptable conditions in terms of the number of required dc voltage sources and the variety of isolated dc voltage sources, as well. Furthermore, Fig. 7(e) corroborates the desired situation of the proposed topology as the total blocking voltage view point in comparison to the others. Meanwhile, in terms of the overall estimated cost function aspect, the proposed topology has the most desirable conditions in comparison with all of the discussed structures based on their variations in Fig. 7(f).

IV. Verification Results

In this section, obtained simulation and experiment results based on the proposed MLVSI topology shown in Fig. 3(a) and the proposed CMMLI depicted in Fig. 4 are presented. In the computer simulation process, PSCAD/EMTDC software is used and all of the semiconductor devices are assumed to be ideal.

In all processes of simulation and experimental tests, a resistive-inductive load with values of $R = 25\Omega$ and $L = 250mH$ is considered. The experimental setup of the proposed topology is shown in Fig 8. The power MOSFETs used in the prototype are SPW47N60C3s (with antiparallel diode) that can tolerate 650V as the maximum value of the peak inverse or blocked voltage value. Meanwhile, a 89C52 microcontroller made by ATMEL Company has been utilized in the experimental tests to generate the respective gate switching pulses at the fundamental switching frequency with respect to Table I.

In addition, among the four proposed algorithms to meet



(a) (b)

Fig. 9. Output voltage and current waveforms (a) in simulation (b) in experiment.

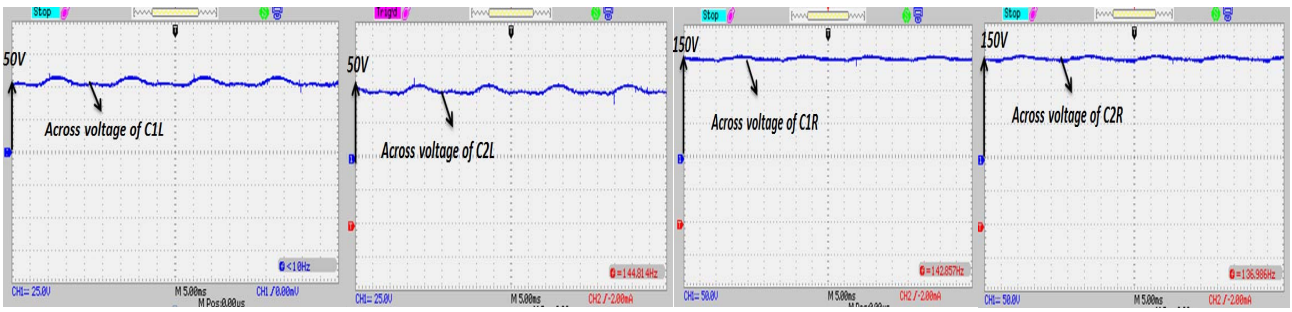


Fig. 10. Across voltage waveforms of capacitors in the experiment (50V/div).

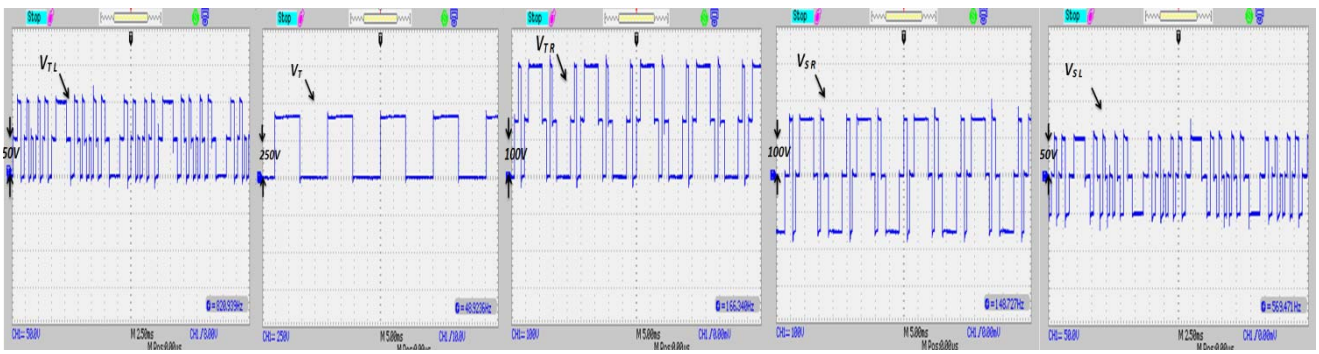


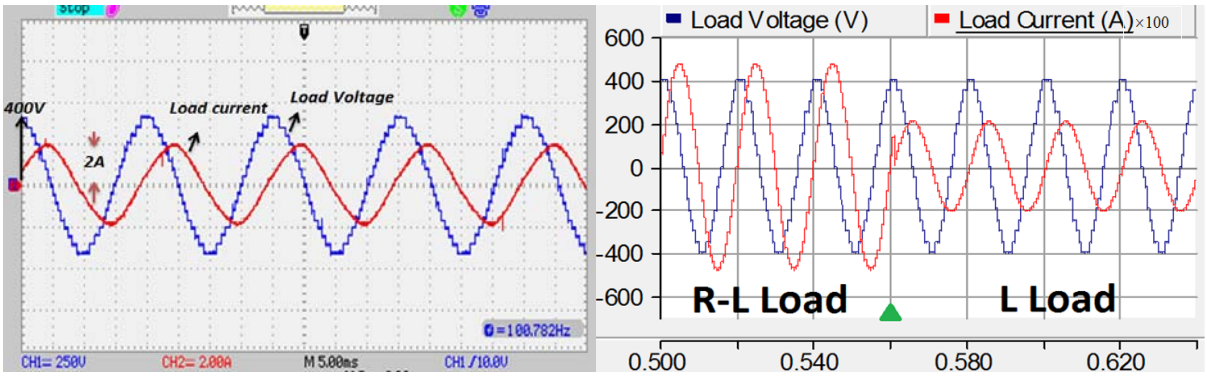
Fig. 11. Observed blocking voltage waveforms from left to right for switches T_L (50V/div), T (50V/div), T_R (100V/div), S_R (100V/div)and S_L (50V/div) based on the experimental results.

the precise magnitudeof dc voltage sources, the third asymmetric pattern which could attain the best cost-effective capability of generating the largest number of output voltage levels with the minimum devices count, is considered in the performance evaluation. Therefore, the values of two utilized dc voltage sources are set on 100V and 300V based on the third presented algorithm. In addition the capacitance of all dc link capacitors are assumed same and equal to $2200\mu F$.

Fig. 9 (a) and (b) show the output 17-level voltage and nearly sinusoidal load current in the simulation and in experiment, respectively. As can be seen, the obtained results have good agreement with each other. Here, the maximum amplitude of the load voltage and current are 400V and 5A, respectively.

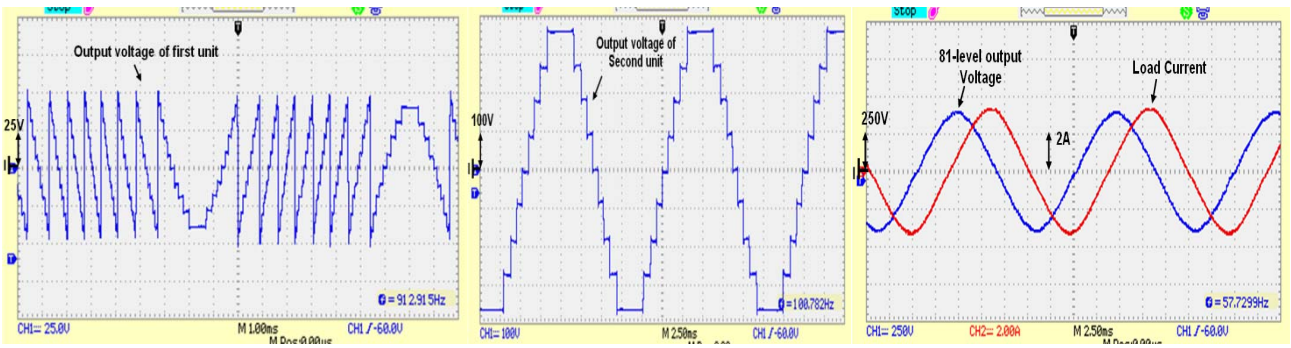
Furthermore, the balanced voltage waveforms of the dc link capacitors on the basis of experimental results are shown in Fig. 10. As can be seen, the dc link voltages are quite smooth and have acceptable ripple values, which can attest to the precise capacitive divider feature of the proposed topology during the loading condition. The peak inverse voltage (PIV) or blocked voltage waveforms across the switches T_L , T , T_R , S_R and S_L in the experimental process have also been illustrated in Fig. 11. In this case, the maximum value of blocked voltage is about 400V which can be tolerated by two interconnected switches.

Likewise, to confirm the correct performance of the proposed circuit during different types of loading conditions when a 2A inductive load has been connected at the output, the experimental effectiveness of output voltage and current waveforms are shown in Fig. 12(a). Also, based on the simulation platform, the overall performance of system under a step change in the type of load from 5A (resistive-inductive loading condition) to 2A (inductive loading condition) is



(a) (b)

Fig. 12. Output voltage and current waveforms (a) Under an inductive load condition in the experiment (b) Sudden dynamic behavior in simulation.



(a) (b) (c)

Fig. 13. Observed waveforms of proposed 81-level inverter from the experimental test (a) output voltage of first unit (25V/div) (b) output voltage of second unit (100V/div)(c) load voltage and current (250V/div&2A/div).

shown in Fig. 12(b). In this case, as expected, all of the output voltage levels can be properly made without any distortions in the output voltage levels which can demonstrate the robust performance of the proposed system in terms of dynamic view.

Finally, in order to assert the capability of the proposed structure in a higher number of output voltage levels and to authenticate the performance of the other recommended algorithms for the dc voltage sources' magnitude, the connection of two series units of the proposed MLVSI based on Fig. 4 is considered at this stage, when an inductive load has been connected at the output. In this case, by utilizing only 16 switching devices, two dc sources in each unit and the fourth presented pattern for the magnitude of the dc voltage sources, an 81-level output voltage is made with respect to (30).

Fig. 13 (a)-(c) show the corresponding output voltages of the first unit, second unit and 81-level load voltage and current waveforms of this structure in the experiment, while a 3A inductive load is connected at the output. Here, the magnitude of the used dc-sources are set at $V_{dc,L1} = V_{dc,R1} = 20V$ and $V_{dc,L2} = V_{dc,R2} = 180V$.

Therefore, both of the units of the proposed MLVSIs produce four positive levels, four negative levels and one zero level at their output with amplitudes of $\pm 10V, \pm 20V, \pm 30V, \pm 40V$ and $\pm 90V, \pm 180V, \pm 270V, \pm 360V$, for the first and second proposed series units, respectively.

V. CONCLUSIONS

In this paper, to generate a higher number of output voltage levels with reductions in the components count and in the other important power electronic parameters of the cascaded modular multilevel inverters (CMMLIs), a new topology was presented in which does not require any H-bridge cells in each series unit to turn the output voltage polarity. Hence, each series unit of the proposed CMMLI is composed of two isolated dc voltage sources, four capacitors and eight gate drivers. In this case, all of the dc link capacitors are directly charged by power supplies without utilizing any complicated control strategies. In addition, in order to achieve a different number of output voltage levels, four different algorithms for determining the magnitude of the dc voltage sources were suggested. A comprehensive comparison from different aspects confirms the advantages of the proposed structure in comparison to several recently presented CMMLIs. Finally,

the effectiveness and correct performance of proposed 17-level and 81-level derived topologies have been verified by simulation and experimental results.

REFERENCES

[1] J. Rodriguez, L. J.Sheng, and P. Fang Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE* Trans. Ind Electron., Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[2] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., Vol. 57, No. 7, pp. 2197-2206, Jul. 2010.

[3] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on natural point clamped inverters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.

[4] M. Ebadi, M. Joorabian, and J. S. Moghani, "Multilevel cascade transformerless inverter for connecting distributed-generation sources to network," *IET Power Electron,* Vol. 7, No. 7, pp. 1691-1703, Dec. 2014.

[5] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.,* Vol. 23, No. 4, pp. 1598-1607, Jul. 2008.

[6] M. Khazraei, H. Sepahvand, M. Ferdowsi, and K. A. Corzine, "Hysteresis based control of a single-phase multilevel flying capacitor active rectifier," *IEEE Trans. Power Electron*., Vol. 28, No. 1, pp. 154-164, Jan. 2013.

[7] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp. 140-147, Jan. 2006.

[8] P. Roshankumar, R. S. Kaarthic, K. Gupakumar, J. I. Leon and L. G. Franquelo, " A seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridge, " *IEEE Trans. Power Electron.,* Vol. 30, No. 7, pp. 3471-3478. Jan. 2015

[9] M. FarhadiKangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of sub multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 625-636, Feb. 2013.

[10] A. Ajami, M. R. J. Oskuee, A. Mokhberdoran, and A. Van den Bossche, "Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches," *IET Power Electron.*, Vol. 7, No. 2, pp. 459-466, Feb. 2014.

[11] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.,* Vol. 57, No. 8, pp. 2643-2650, Aug. 2010.

[12] R. S. Alishah, D. Nazarpour, S. H. Hosseini and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.* Vol. 62, No. 1, pp. 256-269, Jan. 2015.

[13] M. F. Kangarlu, E. Babaei, M. Sabahi, and M. R. AlizadehPahlavani, "Cascaded multilevel inverter using sub-multilevel cells," *J. Elect. Power Syst. Res,* Vol. 96, pp. 101-110, Mar. 2013.

[14] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched-capacitor units," *IEEE Trans. Ind. Electron*., Vol. 61, No. 9, pp 4614-4621, Sep. 2014.

[15] A. K. Sadigh,. V. Dargahi, M. Abarzadeh, and S. Dargahi, "Reduced DC voltage source flying capacitor multicell multilevel inverter: analysis and implementation," *IET Power Electron*., Vol. 7, No. 2, pp. 439-450, Feb. 2014.

[16] R. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi, and L.Chang "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple dc link producer with reduced number of switches," *IEEE Trans. Power Electron.,* Vol. 31, No. 8, pp 5604-5617, Aug. 2016.

[17] R. ShalchiAlishah, D. Nazarpour, S. H Hosseini, and M. Sabahi, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electron*., Vol. 7, No. 1, pp. 96-104, Jan. 2014.

[18] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Trans. Power Electron.*, Vol. 26, No. 11,pp. 3109-3118, Nov. 2011.

[19] E. Babaei and S.H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Elsevier Journal of Energy Conversion and Management*, Vol. 50, No. 11, pp. 2761- 2767, Nov. 2009.

[20] K. K. Gupta and Sh. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 7, pp. 3269-3278, Jul. 2014.

[21] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power Electron*. Vol. 29, No. 12, pp. 6712-6724, Dec. 2014.

[22] E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with Series Connection of novel H-bridge basic units," *IEEE Trans. Ind. Electron*, Vol. 61, No. 12, pp. 6664-6671, Dec. 2014.

[23] M. FarhadiKangarlu, E. Babaei, and S. Laali, "Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources," *IET Power Electron.*, Vol. 5, No. 5, pp. 571-581, May 2012.

[24] E. Babaei, S. Laali, and Z. Bayat "A single phase cascade multilevel inverter based on a new basic unit with reduced number of power switches,"*IEEE Trans. Ind. Electron*, Vol. 62, No. 2, pp. 922-929. Jan. 2015.

[25] S. Laali, E. Babaei, and M. B. Sharifian, "A new basic unit for cascade multilevel inverters with the capability of reducing the number of switches," *Journal of Power Electronics*, Vol. 14, No. 4, pp. 671-677, Nov. 2014.

[26] E. Babaei, M. F. Kangarlu and M. Sabahi, "Extended multilevel converters: an attempt to reduce the number of independent dc voltage sources in cascade multilevel converters," *IET Power Electron.* Vol. 7, No. 1, pp. 157-166. Jan. 2014.

Reza Barzegarkhoo received his B.S. degree in Electrical Power Engineering from the University of Guilan, Rasht, Iran, in 2010; and his M.S. degree from the Sahand University of Technology (SUT), Tabriz, Iran, in 2012. He is presently working at the Guilan Electrical Energy Distribution Company, Rasht, Iran, as an Operating Electrical Power Engineer. His current research interests include the design and control of power electronic converters, multilevel voltage source inverters, charge balancing control, switched-capacitor converters and photovoltaic and distributed generation systems.

Naser Vosoughi received his B.S. degree from the Islamic Azad University, South Tehran Branch, Tehran, Iran, in 2011; and his M.S. degree in Electrical Engineering from the University of Tabriz, Tabriz, Iran, in 2014, where he is presently working towards his Ph.D. degree in the Department of Electrical and Computer Engineering. His current research interests include multilevel inverters, grid tied inverters, dc-dc switched capacitors, switched inductor converters, switching power supplies, induction motor drives and MPC controllers.

Elyas Zamiri received his B.S. degree in Electrical Engineering from the University of Guilan, Rasht, Iran, in 2012; and his M.S. degree from the University of Tabriz, Tabriz, Iran, in 2014. His current research interests include new topologies for multilevel voltage source inverters, switched-capacitor dc-dc converters and renewable energy systems.

Hossein Madadi Kojabadi received his Ph.D. degree in Electrical Engineering from the University of New Brunswick, Fredericton, NB, Canada, in 2003. Since 1993, he has been a faculty member at the Sahand University of Technology, Tabriz, Iran. From 2003 to 2004 he was Post-doctoral Fellow at the University of New Brunswick. He has published over 100 papers in technical journals and conference proceedings. He has also published two books. He is currently the Managing Director of the Renewable Energy Research Center. His current research interests include renewable energy conversion, power electronic converters and variable-speed drives.

Liuchen Chang received his B.S. degree in Electrical Engineering from Northern Jiaotong University, Beijing, China, in 1982; his M.S. degree from the China Academy of Railway Sciences, Beijing, China, in 1984; and his Ph.D. degree from Queen's University, Kingston, ON, Canada, in 1991. He is presently working as a Professor at the University of New Brunswick, Fredericton, NB, Canada. His current research interests include distributed generation, renewable energy conversion, direct load controls, and power electronic converters. Dr. Chang is a Fellow of the Canadian Academy of Engineering.