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Optimized Hybrid Modulation Strategy for AC Bypass Transformerless Single-Phase Photovoltaic Inverters

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Abstract

The full-bridge inverter, widely used for single-phase photovoltaic grid-connected applications, presents a leakage current issue. Therefore, an AC bypass branch is introduced to overcome this challenge. Nevertheless, existing modulation strategies entail drawbacks that should be addressed. One is the zero-crossing distortion (ZCD) of the AC current caused by neglecting the AC filter inductor voltage. Another is that the system cannot deliver reactive power because the AC bypass branch switches at the power frequency. To address these problems, this work proposes an optimized hybrid modulation strategy. To reduce ZCD, the phase angle of the inverter output voltage reference is shifted, thereby compensating for the neglected leading angle. To generate the reactive power, the interval of the negative power output is calculated using the power factor. In addition, the freewheeling switch is kept on when power is flowing into the grid and commutates at a high frequency when power is fed back to the DC side. In this manner, the dead-time insertion in the high-frequency switching area is minimized. Finally, the performances of the proposed modulation strategy and traditional strategies are compared on a universal prototype inverter. Experimental results validate the theoretical analysis.

Key words: Dead time, Leakage current, Modulation strategy, Transformerless inverter, Zero-crossing distortion (ZCD)

I. INTRODUCTION

The transformer-less, grid-connected, full-bridge inverters have advantages over the transformer-based inverters in their efficiency, size, weight, and cost [1]-[4]. Compared with bipolar sinusoidal pulse-width modulation (SPWM), unipolar SPWM has received more attention due to its smaller current ripple in the filter inductor and higher operation efficiency [5]. However, common-mode voltage (CMV) changes at the switching frequency as a result of zero vectors. Without galvanic separation, high-frequency CMV causes adverse leakage current. The current flows from the photovoltaic (PV) module to the system through the grid to ground parasitic capacitance [6]. The flow paths of the differential-mode and common-mode current are shown in Fig. 1. The leakage current increases the grid current harmonics and system losses, generating a strong conducted and radiated electromagnetic interference and threatening personal safety [5]-[7]. Therefore, the leakage current must be suppressed under a certain value. The German DIN VDE 0126-1-1 standard states that the grid must be disconnected within 0.3 s if the leakage current is over 300 mA [8].

To suppress the leakage current, new freewheeling paths are constructed to separate the PV array from the grid [2], [9]-[19]. According to the position of freewheeling switches, the topologies can be divided into the DC bypass ones [9]-[12] and the AC bypass ones [2], [13]-[19]. In H5 topology, an active switch is introduced to the DC bus to decouple the PV module [10]. However, this method does not clamp CMV to half of the DC-link voltage during zero vector generation [2]. For this purpose, an active switch is inserted between the midpoint of the split DC-link capacitors and the upper terminal of the full-bridge module, which is called the DC-based H6 inverter [11]. If two passive diodes are inserted into the H6 inverter to achieve passive clamping performance, then the DC-based neutral point clamp (NPC) H6 inverter is obtained [9]. Compared with DC bypass topologies, AC bypass topologies

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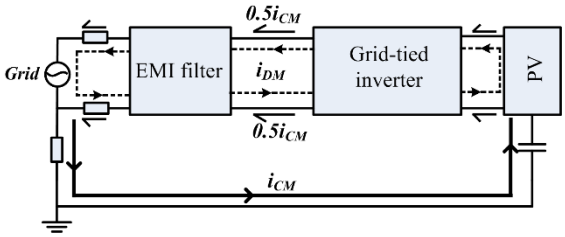


Fig. 1. Flow paths of the differential-mode (i_{DM}) and common-mode (i_{CM}) currents.

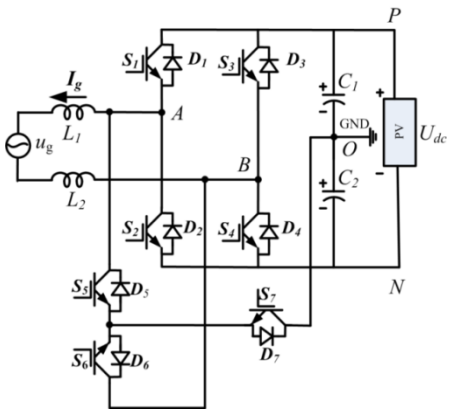


Fig. 2. HERIC-based clamping topology.

have lower power losses due to the current flowing through lower power switches. AC bypass topologies realize new freewheeling paths by adding a bidirectional switch between the midpoints of two legs. In accordance with the aforementioned principle, a highly efficient and reliable inverter concept (HERIC) topology [15], an H-bridge zero voltage rectifier (HB-ZVR) topology [13], a full-bridge inverter topology with a constant common-mode voltage (FB-CCV) [14], and a HERIC-based clamping topology [2] are proposed. The clamping methods are similar to the DC topologies. In addition, the HERIC-based clamping topology is typical because it only has one active clamping switch. Fig. 2 illustrates this topology. Although existing modulation strategies achieve adequate leakage current suppression, they present several drawbacks.

The first problem is zero-crossing distortion (ZCD). ZCD results from neglecting inductor voltage, which is an inherent problem of single-phase inverters. In general, inverter output voltage and grid voltage are considered equal. In addition, drive signals operate in accordance with the grid voltage phase. The ideal inverter output voltage leads the grid voltage when inductor voltage is considered. However, in the modulation design process, the inverter output and grid voltages are generally considered equal, which causes ZCD of the grid-in current. Beyond the aforementioned reason, ZCD is caused by switching delay [20] and inadequate inductor excitation [21]. The ZCD issue resulting from neglecting the inductor voltage has been explored in [22], [23]. The analysis of ZCD is strictly under the unity power factor operation and focuses on the transient process. Moreover, while the AC bypass switches is working in power frequency, the AC bypass single-phase inverter is unable to generate reactive power. In accordance with the requirement of the standard VDE-AR-N 4105 [8], grid-tied PV inverters should be able to compensate for the reactive power [23], [24]. To adjust the reactive power, the bypass switches should commutate at a high frequency. However, dead-time insertion is required to avoid a short circuit on the DC side. During dead time, reverse charging occurs in the DC capacitors, which causes a series of problems. First, dead time offsets the effective duty, and dead-time compensation is required. Second, differential-mode characteristics deteriorate, which causes the inverter to lose unipolar properties [14]. Third, dead time produces charge and discharge currents at switch frequency, thereby introducing an additional loss. Fourth, the induced CMV change excites the leakage current. To solve the aforementioned problems, this work presents an optimized hybrid modulation strategy. First, to reduce ZCD, the phase angle of the inverter output voltage is shifted to compensate for the neglected leading angle caused by the inductor. Then, the interval of the negative power output is calculated using the power factor. The freewheeling switch is kept on while power is flowing into the grid and commutates at a high frequency when power is fed back to the DC side. Therefore, the dead time insertion area is minimized. Overall, two modulation strategies are based on system states. Hence, the common-mode and differential-mode characteristics of the AC bypass inverter system are promoted.

The rest of this paper is organized as follows. Section II analyzes the ZCD and dead time issues in the existing modulation strategy. The optimized hybrid modulation strategy is then proposed in Section III. Section IV presents the comparative experiments. Section V summarizes the conclusions.

II. Analysis of the Existing Modulation Strategy

A. Zero-Crossing Distortion

The ordinary full-bridge, single-phase inverter topology is shown in Fig. 3(a). The drive signals of the general unipolar modulation strategy are illustrated in Fig. 3(b). The inductor voltage is neglected, and the inverter output voltage is considered equal to the grid voltage [9]-[19].

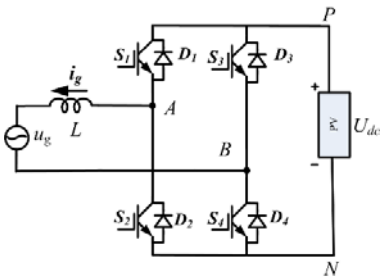
The voltage equation of the single-phase inverter is

$$u_L(t) = L\frac{di_g(t)}{dt} = u_{AB}(t) - u_g(t) \tag{1}$$

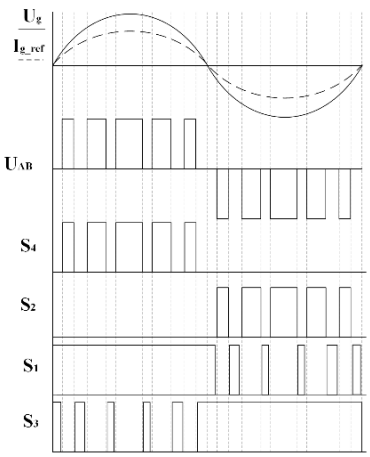
where $u_L(t)$ is the voltage drop across the inductor L. Considering the steady state,

$$u_g(t) = E_m \sin(wt),\ \ i_g(t) = i_g^*(t) = I_m^* \sin(wt+\alpha) \tag{2}$$

where ω, α, and E_m are the grid angular frequency, power factor angle, and grid voltage amplitude, respectively.

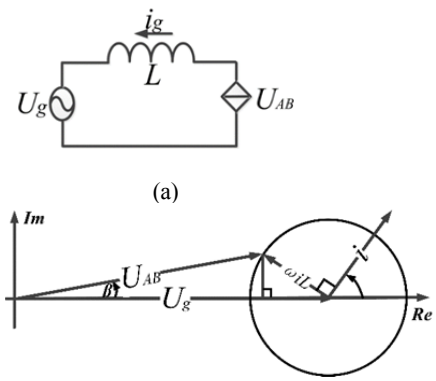


(a)



(b)

Fig. 3. (a) Ordinary single-phase inverter topology, (b) drive signals.



(a)

(b)

Fig. 4. (a) Inverter equivalent circuit, (b) inverter vector diagram at an arbitrary power factor.

Substituting (2) into (1) results in

$$u_L(t) = \omega L I_m^* \cos(\omega t+\alpha) = u_{AB}(t) - E_m \sin(\omega t) \tag{3}$$

$$\begin{aligned} u_{AB}(t) &= \omega L I_m^* \cos(\omega t+\alpha)+E_m \sin(\omega t) \\ &= (E_m - \omega L I_m^* \sin\alpha)\sin(\omega t)+\omega L I_m^* \cos\alpha \cos(\omega t) \\ &= U_m \sin(\omega t+\beta) \end{aligned} \tag{4}$$

$$U_m = \sqrt{(E_m - \omega L I_m^* \sin\alpha)^2 + (\omega L I_m^* \cos\alpha)^2} \tag{5}$$

$$\beta = \arctan\frac{w L I_m^* \cos\alpha}{E_m - w L I_m^* \sin\alpha} \tag{6}$$

Fig. 4(a) presents the equivalent circuit diagram of the AC side. Fig. 4(b) shows the vector diagram at an arbitrary power factor. The power factor angle is considered from $-\pi/2$ to $\pi/2$.The lead angle β can also be directly calculated using voltage vector relationships.

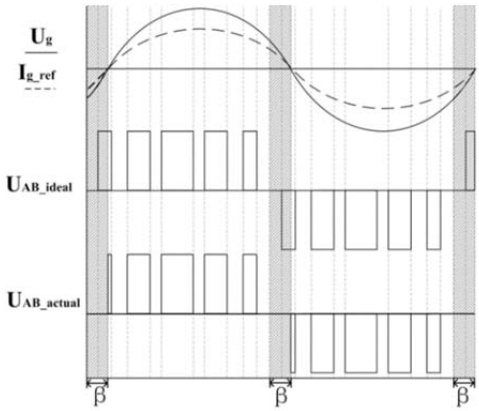


Fig. 5. Comparison between the ideal and the actual inverter output voltages under the unity power factor operation.

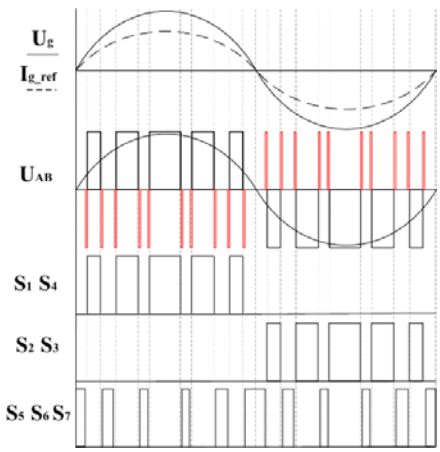


Fig. 6. Gate drive signal of the HERIC-based clamping topology with dead-time insertion (the red area is caused by the dead-time insertion).

The leading angle reaches a maximum value under the unity power factor operation. The comparison between the ideal and the actual inverter output voltages is illustrated in Fig. 5. Disregarding the leading angle results in ZCD because the actual inverter output voltage is incomplete. The shaded area denotes the missing interval.

B. Dead-Time Insertion

The HERIC-based clamping topology cannot adjust the reactive power when the bypass switches work at a power frequency. In modified clamping topologies, such as HB-ZVR [13] and FB-CCV [14], the AC bypass switches commutate at a high frequency. Consequently, the power factor adjustment is simple. The modulation strategy is universal for different AC bypass topologies. Fig. 6 illustrates the typical dead-time insertion gate drive signals of the HERIC-based clamping topology without considering voltage drop on the inductor. The HB-ZVR and FB-CCV topologies have similar modulation strategies.

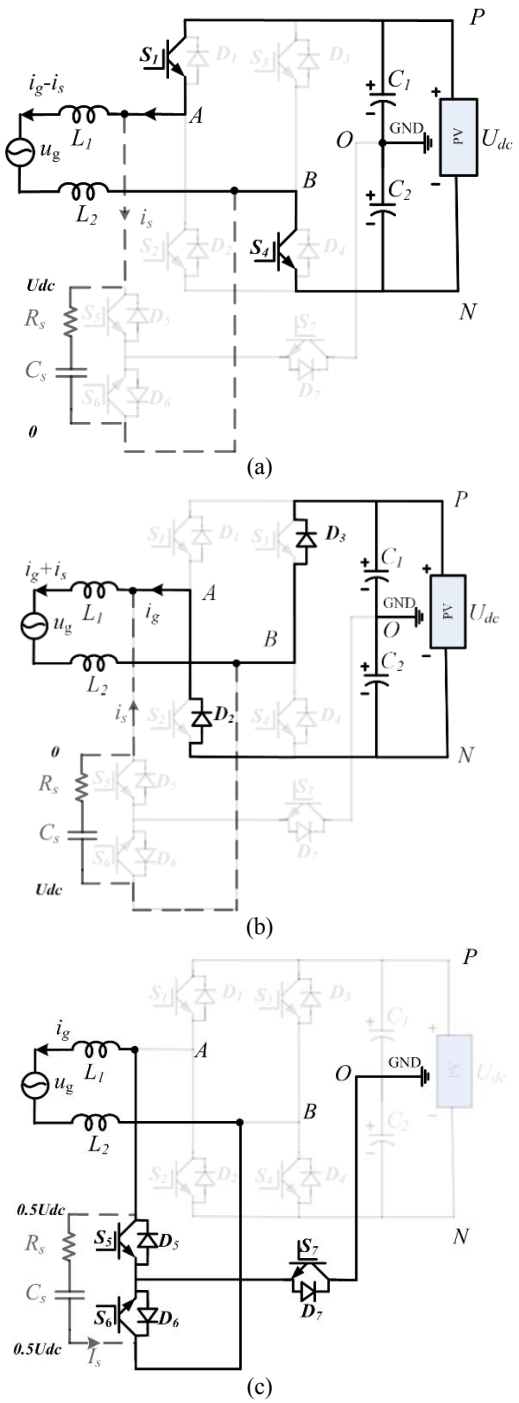


Fig. 7. Operation modes of HERIC-based clamping topology in the positive voltage half cycle: (a) mode 1, power transmission, (b) mode 2, reverse charging, (c) mode 3, freewheeling.

During dead time, all the switches are turned off, and reverse charging occurs in the DC capacitors. The grid-in current flows into the DC bus capacitors through the antiparallel diodes, D_2 and D_3, during the positive half cycle, and D_1 and D_4, during the negative half cycle, respectively. Fig. 7 shows the operation modes of the HERIC-based clamping topology in the positive voltage half cycle. Figs. 7(a), 7(b), and 7(c) illustrate modes 1, 2, and 3, which are the power transmission, reverse charging, and freewheeling modes, respectively. The dead-time insertion causes a series of problems. First, the effective time is cancelled out by the dead time as a consequence of reverse charging. In addition, dead-time compensation is required. Second, the differential-mode characteristics deteriorate, and the unipolar properties are affected. Mode 2 is consistent with the freewheeling mode of bipolar SPWM. However, modes 1 and 3 belong to unipolar SPWM. As a result of the combined operation modes, the modulation is a quasi-unipolar SPWM (qSPWM) instead of a real unipolar SPWM [14]. From modes 1 to 2 and then mode 3, the voltage of the parasitic capacitance and resistance (or snubber capacitance and resistance) changes from U_{dc} to $-U_{dc}$ and then to 0. A charge and discharge current I_s is found at the switch frequency, which results in an additional loss. Although the steady-state CMV is constant in the three modes, the transient charge and discharge process simultaneously changes the CMV and induce an increased leakage current.

III. Proposed Optimized Hybrid Modulation Strategy

A. Interval Division of the Hybrid Modulation Strategy

The ZCD problem resulting from disregarding the inductor voltage is analyzed in Section II.A. In the actual inverter system, the grid voltage U_g, inductance L, and grid electrical frequency ω are constant. The power factor angle α is artificially set. Specific to the solar system, the real-time grid-in current I^*_m can be determined using the maximum power point tracking (MPPT) algorithm. Therefore, the real-time lead angle β can be obtained.

The phase-shift angle of the inverter voltage is calculated according to the real-time leading angle β and the grid voltage phase ωt obtained by a phase-locked loop (PLL). The inverter voltage phase changes from ωt to $\omega t+\beta$. Thus, the actual inverter voltage is equal to the ideal one, and ZCD is avoided.

The AC bypass switches do not work at a power frequency under the non-unity power factor operation because of the short-circuit phenomenon of the DC capacitors via S_1, S_5, D_6, and S_4 or S_3, S_6, D_5, and S_2 during power transmission interval. This condition occurs when the power is fed back to the DC side. To avoid a short circuit, the bypass switches should commutate at a high frequency with dead-time insertion. The inverter output power is expressed as follows:

$$P_{inv} = u_{AB}(t) i_g(t) = U_M I^*_m \sin(\omega t + \alpha) \sin(\omega t + \beta) \tag{7}$$

When the power flow is negative,

$$P_{inv} < 0 \tag{8}$$

$$\sin(\omega t + \alpha) \sin(\omega t + \beta) < 0 \tag{9}$$

By solving Formula (9), the dead-time insertion interval can be determined. On the basis of the sizes of α and β, the interval division of the hybrid modulation strategy is presented in Table I.

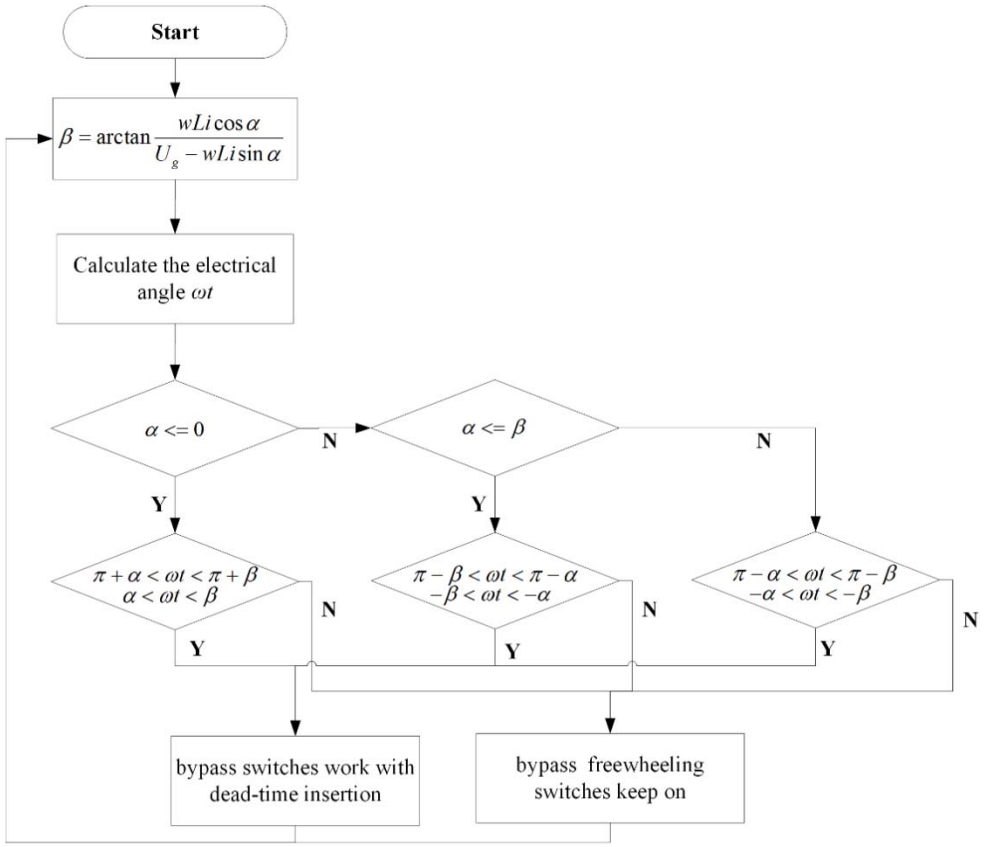
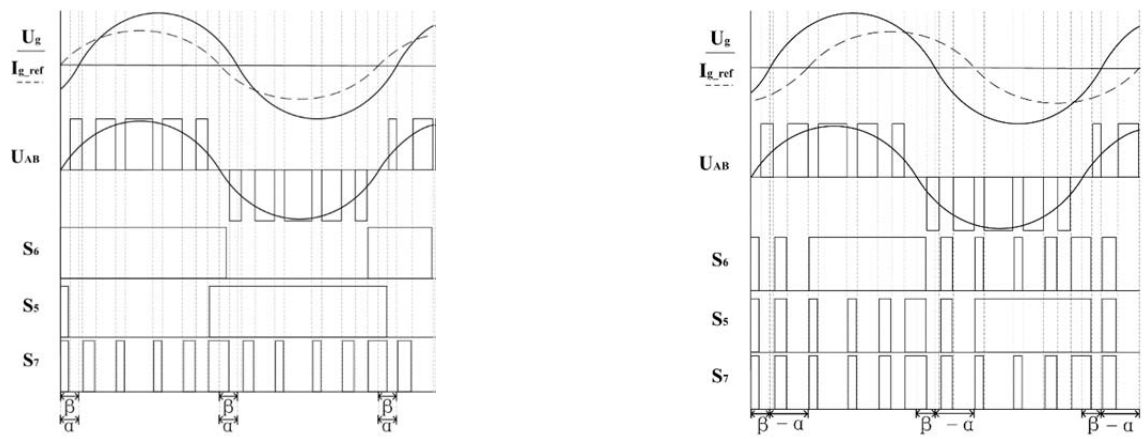


Fig. 8. Flowchart of the optimized hybrid modulation strategy.



(a) (b)

Fig. 9. (a) Driver signals and waveforms when $\alpha = \beta$, (b) driver signals and waveforms for a lagging power factor with a phase shift.

(a) (b)

Fig. 10. Waveforms of the hybrid modulation strategy for a leading power factor: (a) $\alpha < \beta$, (b) $\alpha > \beta$.

TABLE I
INTERVAL DIVISION OF THE HYBRID MODULATION STRATEGY

Power factor angle α	Dead-time insertion interval	Freewheeling interval
$-\pi/2<\alpha<0$	$[2\pi+\alpha\ 2\pi]\cup[0\ \beta]\cup[\pi+\alpha\ \pi+\beta]$	$[\alpha,\ 2\pi]\cup[\beta\ \pi+\alpha]\cup[\pi+\beta\ 2\pi+\alpha]$
$0<\alpha<\beta<\pi/2$	$[\pi-\beta\ \pi-\alpha]\cup[2\pi-\beta\ 2\pi-\alpha]$	$[2\pi-\alpha\ 2\pi]\cup[0\ \pi-\beta\cup[\pi-\alpha\ 2\pi-\beta]$
$0<\beta<\alpha<\pi/2$	$[\pi-\alpha\ \pi-\beta]\cup[2\pi-\alpha\ 2\pi-\beta]$	$[2\pi-\beta\ 2\pi]\cup[0\ \pi-\alpha\cup[\pi-\beta\ 2\pi-\alpha]$

The flowchart of the proposed optimized modulation strategy is shown in Fig. 8. The specific procedures are described as follows:

1) Calculate the phase shifting angle using (6).
2) Calculate the angle *wt* using PLL.
3) Evaluate the interval as indicated in Table I.

In addition, the dead-time insertion is analyzed under different power factors. When $\alpha = \beta$, the inverter voltage presents the same phase as the inductor current. The inverter-out power flow is positive for the entire cycle, and the AC bypass switches work at a power frequency. Fig. 9(a) shows the driver signals and waveforms for these conditions. Fig. 9(b) shows the driver signals and waveforms with a lagging power factor. The intervals of phase shifting between U_{AB} and U_g and phase lagging between U_g and I_{g_ref} demonstrate dead-time insertion. The condition under the leading power factor is presented in Fig. 10. Fig. 10(a) corresponds to $\alpha < \beta$, and Fig. 10(b) corresponds to $\alpha > \beta$. In addition, during the negative power flow interval, the inverter works in reverse charging mode, which is the same as the dead-time interval. Thus, the differential-mode characteristics and unipolar properties are unaffected.

B. Reliability Analysis

Without full-period dead-time-insertion, the reliability of the hybrid modulation strategy requires special attention. When power flow changes from positive to negative, the bypass switches should be transformed into a high-frequency commutation state. Otherwise, a DC source short circuit will occur. To prevent this problem, the interval division of the hybrid modulation strategy should be precise, which is based on the grid electrical phase that can be obtained using the PLL. A successful phase lock state is also the foundation for normal operation. In the event of phase lock failure, the system enters a self-protection status. Thus, the proposed modulation strategy is secure.

IV. EXPERIMENTAL RESULTS

A prototype of the HERIC-based clamping topology was built to conduct a comparative experiment between the proposed hybrid modulation strategy and the traditional modulation strategies. The prototype schematic is shown in Fig. 11(a), and the system parameters are listed in Table II.

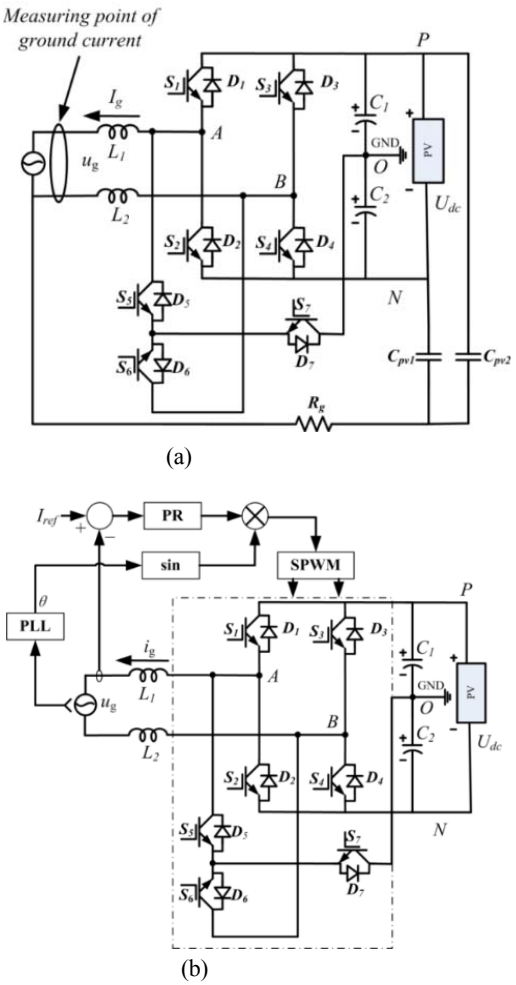


Fig. 11. (a) Schematic of the prototype of the HERIC-based clamping topology, (b) control block diagram for the prototype.

TABLE II
PROTOTYPE PARAMETERS

Parameters	Values
U_{dc}	350 V
Grid voltage/frequency	220 V/50 Hz
Switching frequency	20 kHz
DC-bus capacitor C_1, C_2	2820 μF
Filer inductor L_1, L_2	0.75 mH
PV parasitic capacitor C_{pv1}, C_{pv2}	0.047 μF

The control block diagram for the prototype is presented in Fig. 11(b). The grid voltage is measured and fed to the PLL to obtain ωt. A quasi-proportional resonant (PR) current controller is used to control the grid-in current, thereby

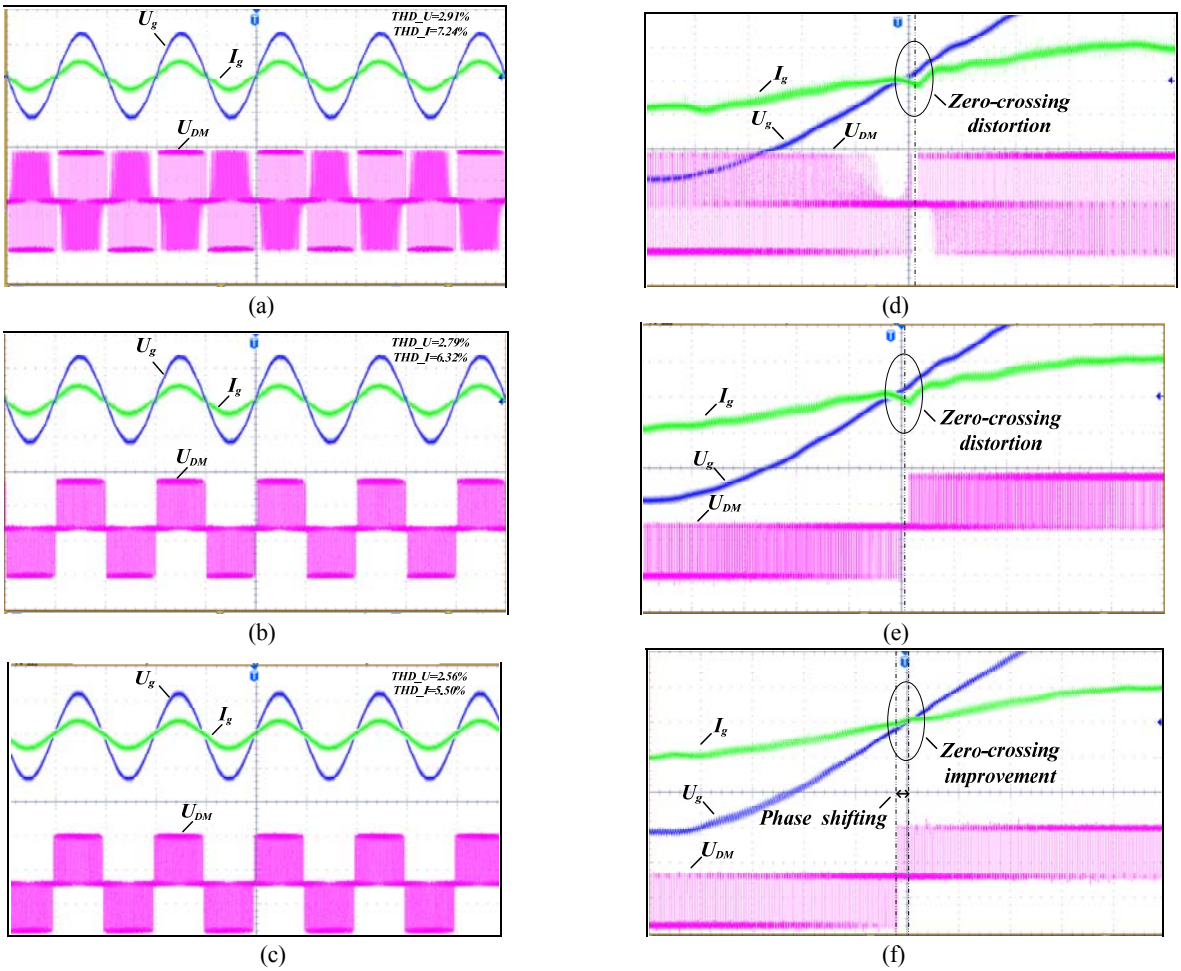


Fig. 12. Experimental waveforms of grid voltage U_g (250 V/div), grid-in current I_g (25A/div), and differential-mode voltage U_{DM} (250 V/div) under a unity power factor: (a) (d) modulation strategy I, (b) (e) modulation strategy II, (c) (f) proposed modulation strategy.

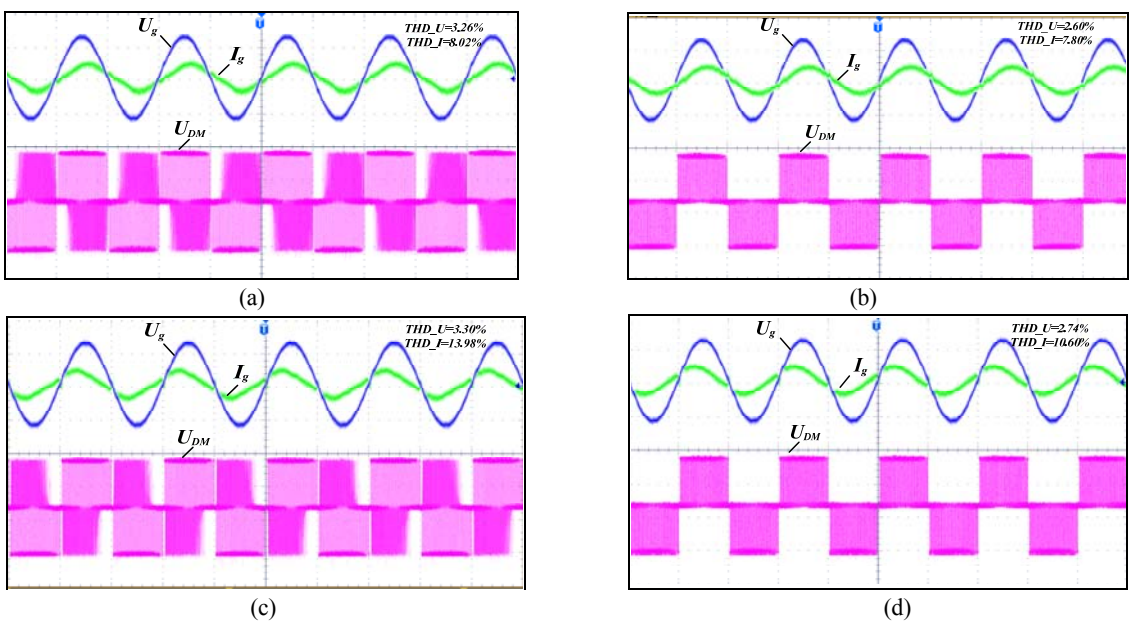


Fig. 13. Experimental waveforms of grid voltage U_g (250 V/div), grid-in current I_g (25 A/div), and differential-mode voltage U_{DM} (250 V/div) (t = 1 ms/div): (a) modulation strategy I under power factor 0.9 lagging, (b) proposed modulation strategy under power factor 0.9 lagging, (c) modulation strategy I under power factor 0.9 leading, (d) proposed modulation strategy under power factor 0.9 leading.

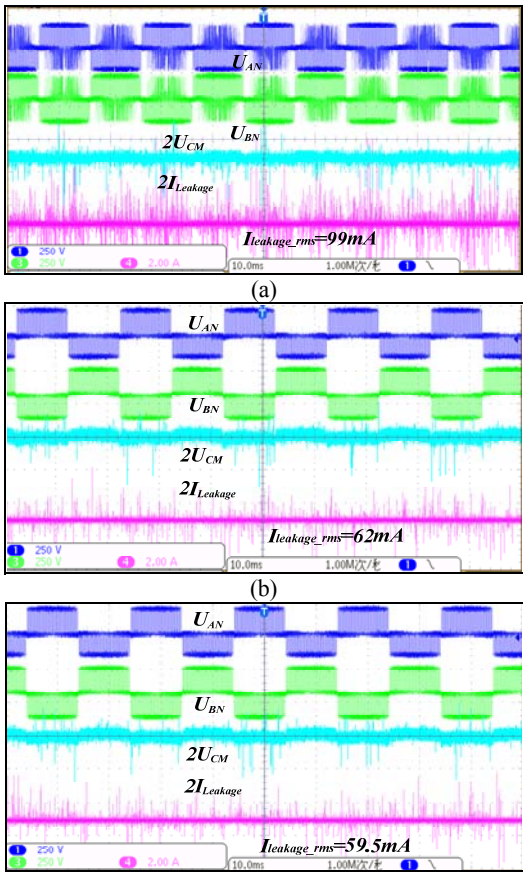


Fig. 14. Experimental waveforms of leakage current $I_{leakage}$ (2 A/div), voltage U_{AN} (250 V/div), U_{BN} (250 V/div), and common-mode voltage U_{CM}(200 V/div) under unity power factor (t = 1 ms/div): (a) modulation strategy I, (b) modulation strategy II, and (c) proposed modulation strategy.

ascertaining that the inductor current precisely tracks the current reference. The output of the quasi-PR current controller is multiplied by the unity sinusoidal signal. The product is then sent to a comparator to generate the switching signals.

A. Validation of the Differential-Mode Characteristics

Fig. 12 shows the experimental waveforms of the grid voltage U_g, grid-in current I_g, and differential-mode voltage U_{DM} under a unity power factor operation. Figs. 12(a), 12(b), and 12(c) illustrate the bypass branch's modulation strategy for complementing the main switches (modulation strategy I), modulation strategy for switching power frequency (modulation strategy II), and hybrid modulation strategy with phase shifting (proposed modulation strategy), respectively. The comparison of the three figures shows that the proposed modulation strategy exhibits the same differential-mode voltage quality as that of modulation strategy II, which is better than modulation strategy I because the reverse charging mode is eliminated when power flow is positive. The proposed modulation strategy demonstrates a better grid current waveform quality because the ZCD caused by disregarding the inductor voltage is eliminated via phase shifting. The details of the zero-crossing point are shown in Figs. 12(d), 12(e), and 12(f), which correspond to (a), (b), and (c). The ZCD of the proposed modulation strategy presents an apparent improvement compared with the two other modulation strategies, and a visible phase shifting is shown in Fig. 12(f).

Fig. 13 shows the conditions under the non-unity power factor operation. Modulation strategy II cannot work under the non-unity power factor operation, and a comparison between modulation I and the proposed modulation is provided. Figs. 13(a) and 13(b) represent the condition of modulation strategy I and the proposed modulation strategy with a lagging power factor of 0.9, respectively. Figs. 13(c) and 13(d) represent the conditions with a leading power factor of 0.9. The same conclusion can be drawn for the comparative analysis of the unity power factor operation. The deterioration of the differential mode voltage caused by the reverse charging mode is only effective when power flow is positive. When power flow is negative, the power transmission mode also exhibits reverse charging. In addition, the dead-time insertion will not influence the differential mode voltage. No reverse voltage occurs in the proposed modulation for the entire period. In the negative power flow interval, no reverse voltage occurs in modulation I. In addition, a current distortion exists at the voltage zero-crossing point when the inverter works under the non-unity power factor operation, particularly for the leading power factor, because the grid voltage cannot sufficiently magnetize the inductor with unipolar SPWM around the voltage zero-crossing point [23].

B. Validation of the Common-Mode Characteristics

Fig. 14 shows the experimental waveforms of the leakage current $I_{leakage}$, voltage U_{AN}, voltage U_{BN}, and common-mode voltage $2U_{CM}$ ($2U_{CM} = U_{AN} + U_{BN}$) with the unity power factor operation. Figs. 14(a), 14(b), and 14(c) represent the conditions of modulation strategy I, modulation strategy II, and the proposed modulation strategy, respectively. Based on the waveform quality of the common mode voltage, the proposed modulation strategy and modulation strategy II perform similarly and better than modulation strategy I. In accordance with the analysis in Section II.B, the transient charge and discharge process during mode changes causes an alteration in the CMV, thereby increasing leakage current. The root mean square (RMS) values of the leakage current of modulation strategy I, modulation strategy II, and the proposed modulation strategy are 99.0, 62.0, and 59.5 mA, respectively. Table III presents the leakage current comparison of the three modulation strategies under different power factors. As shown in the table, the proposed modulation strategy demonstrates better leakage current suppression performance compared with modulation strategy I. Moreover, the proposed strategy can make the inverter work under an arbitrary power factor, which is not achieved by modulation strategy II.

C. Efficiency Analysis

TABLE III
LEAKAGE CURRENT COMPARISON OF THE THREE MODULATION STRATEGIES WITH DIFFERENT POWER FACTORS

Modulation strategy	Power factor	Leakage current	Efficiency
Modulation strategy I	Unity	99 mA	92.2%
	0.9 lagging	98.5 mA	94.6%
	0.9 leading	97 mA	93.4%
Modulation strategy II	Unity	62 mA	93.4%
	0.9 lagging	Does not work	/
	0.9 leading	Does not work	/
Proposed modulation strategy	Unity	59.5 mA	93.8%
	0.9 lagging	60 mA	95.8%
	0.9 leading	59 mA	94.5%

As presented in Section II.B, the additional loss brought by reverse charging was analyzed, which occurs in modulation strategy I. Due to the mode changes, there will be a charge and discharge current I_s of the parasitic capacitance C_S and resistance R_S (or snubber capacitance and resistance) at a switch frequency. This process generates an additional loss. The charge and discharge current I_s also occurs when modulation strategy II and the proposed modulation strategy are used. However, the frequency is considerably less than that of the switch frequency, which is down to the power frequency. In addition, reverse charging during the positive power flow interval cancels out the effective time, and thus, compensation is required. This compensation introduces additional conduction time, extra conduction, and reversed recovery loss. In conclusion, the proposed modulation strategy demonstrates higher efficiency than modulation strategy I. The experimental results are listed in Table III. The results show a 1.6% improvement under unity power factor operation. The efficiency is 92.2% for modulation strategy I and 93.8% for the proposed modulation strategy. The reference peak value of the grid-in current is 10 A.

V. CONCLUSIONS

To broaden the operating range and improve the performance of the AC bypass transformerless single-phase PV inverter, an optimized hybrid modulation strategy based on the phase shift is proposed in this study. The proposed modulation strategy enables the reactive power output capability of the inverter. In addition, the leakage current is decreased by 40% because dead-time insertion is minimized. The total harmonic distortion of the grid-in current is decreased by 1.74% and its efficiency presents a 1.6% improvement. Therefore, the proposed modulation strategy exhibits the following characteristics:

(i) avoids the ZCD problem caused by disregarding inductor voltage and promotes the quality of the grid-in current,

(ii) possesses the capability of delivering reactive power,

(iii) minimizes dead-time insertion interval, eliminates the reverse-charging phenomenon, reduces leakage current, and improves system efficiency.

These metrics make the proposed hybrid modulation strategy a better candidate for the AC bypass transformerless inverter.

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