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A Novel Modulation Scheme and a DC-Link Voltage Balancing Control Strategy for T-Type H-Bridge Cascaded Multilevel Converters

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Abstract

The cascaded multilevel converter is widely adopted to medium/high voltage and high power electronic applications due to the small harmonic components of the output voltage and the facilitation of modularity. In this paper, the operation principle of a T-type H-bridge topology is investigated in detail, and a carrier phase shifted pulse width modulation (CPS-PWM) based control method is proposed for this topology. Taking a virtual five-level waveform achieved by a unipolar double frequency CPS-PWM as the output object, PWM signals of the T-type H-bridge can be obtained by reverse derivation according to its switching modes. In addition, a control method for the T-type H-bridge based cascaded multilevel converter is introduced. Then a single-phase T-type H-bridge cascaded multilevel static var generator (SVG) prototype is built, and a repetitive controller based compound current control strategy is designed with the DC-link voltage balancing control scheme analyzed. Finally, simulation and experimental results validate the correctness and feasibility of the proposed modulation method and control strategy for T-type H-bridge based cascaded multilevel converters.

Key words: Cascaded multilevel converter, Cascaded SVG, CPS-SPWM, DC-link voltage balancing control, T-type H-bridge, virtual five-level

I. INTRODUCTION

Multilevel converters are receiving more and more attention in high-voltage and large-power electronic applications, since an improved high output voltage can be obtained with a respective harmonic content reduction [1]-[5]. A lot of multilevel converter topologies have been proposed in the past thirty years. The most common topologies are the diode-clamped, capacitor-clamped and cascaded types. In order to operate the switches in the above mentioned topologies, switching schemes such as pulse width modulation (PWM), space vector pulse width modulation (SVPWM), selective harmonic elimination pulse width modulation (SHEPWM), nearest level modulation (NLM) and so on are effective solutions [6], [7].

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Recent studies on multilevel converters are still concentrated on novel multilevel converter topologies and advanced modulation strategies [8]-[14]. The former focus on structure simplification, modular implementation, and new topologies. While the latter aims at improving the output performance of multilevel converters, reducing switching losses, as well as proposing a proper modulation scheme for new topologies.

To satisfy specific application requirements or to improve the operating performance, modifications and combinations of common topologies have been suggested. One of them is a T-type converter [15]-[18]. It is known that the T-type converter is more efficient than other multilevel converter topologies up to the medium switching frequency range.

A single-phase T-type H-bridge converter [19] can generate five voltage levels with a reduced number of switches compared with the traditional H-bridge cascaded multilevel converter. Consequently, this topology takes advantage of simplifying the PWM drive circuit, reducing the device volume, and improving system reliability. The SHEPWM scheme is proposed for this converter topology [20]. It can theoretically

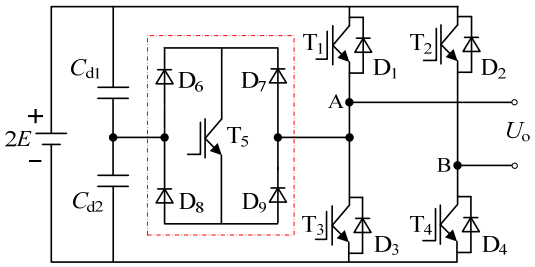


Fig. 1. Configuration of single-phase T-type H-bridge.

eliminate any output voltage harmonics and reduce switching losses. A difficulty is solving nonlinear equations with the Newton iterative method which is not suitable for online calculation. An improved method is a technique using the carriers-staggered SPWM control method [21]. This technique operates well when the carriers are staggered periodically with the modulation signal, with the modulation signal divided as layers and divisions at the same time. In other words, it is not effective when the frequency of the modulation signal varies or when multiple zero crossing points of the modulation signal occur.

With these facts in mind, this paper presents a novel carrier phase shifted PWM (CPS-PWM) control method for the so-called T-type H-bridge based multilevel converter. The rest of this paper is organized as follows. In Section II, the operation principle of the single-phase T-type H-bridge converter is investigated in detail. In Section III, a novel CPS-PWM scheme is proposed for T-type H-bridge following the principle of "changing the minimum number of switch status to achieve a certain voltage level", and a modulation scheme for the T-type H-bridge based cascaded multilevel converter is further designed. In Section IV, a single-phase T-type H-bridge based cascaded multilevel SVG is designed with a repetitive controller based compound current control strategy and a DC-link voltage balancing control scheme. In Section V, a SVG prototype is built and experimental results demonstrate the correctness and feasibility of the proposed modulation and the DC-link voltage balancing control strategy. Finally, Section VI summarizes the results of this paper and draws some conclusions.

II. Operation Principle of T-type H-Bridge

A single-phase T-type H-bridge converter is shown in Fig. 1. Inverter leg A and inverter leg B both consist of two active switches with diodes anti-parallel connected. the bidirectional switch (the part surrounded by the red dotted lines) connected between inverter leg A and the center-tap of the dc power supply is composed of an active switch and a single-phase rectifier bridge.

To facilitate the analysis of the operation principle of the T-type H-bridge, the switching function S_i of the active switch T_i (the anti-parallel diode D_i) is defined. S_i (i=1,2…,5) is set to 1 when the corresponding active switch or anti-parallel diode

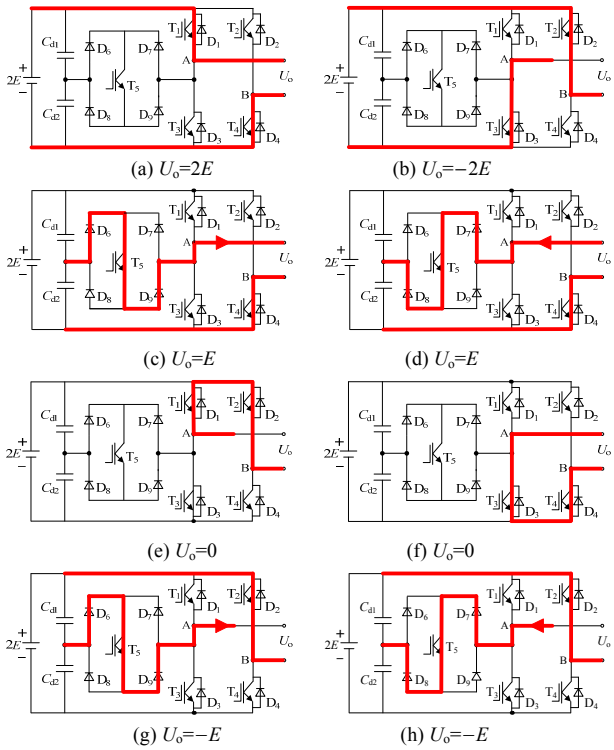


Fig. 2. Conduction paths of the T-type H-bridge.

TABLE I
Switching Modes of the T-type H-bridge

U_o	S_1	S_2	S_3	S_4	S_5
2E	**1**	0	0	**1**	0
E	0	0	0	**1**	**1**
0	0	0	**1**	**1**	0
0	**1**	**1**	0	0	0
-E	0	**1**	0	0	**1**
-2E	0	**1**	**1**	0	0

is turned on, whereas 0 indicates that both the active switch and its anti-parallel diode are turned off.

$$S_i = \begin{cases} 1, & T_i \text{ or } D_i \text{ turn on} \\ 0, & T_i \,\&\, D_i \text{ turn off} \end{cases} \quad (1)$$

Proper switching control of the auxiliary bidirectional switch can generate half a level of the dc supply voltage. Therefore, a five-level (2E, E, 0, -E and -2E) output voltage can be achieved. The operation of a single-phase T-type H-bridge converter can be divided into 8 switching states as illustrated in Fig. 2. It is obvious that only two active switches (or their anti-parallel diodes) can be turned on in each moment, one from inverter leg B, and the other from inverter leg A or the auxiliary switch, otherwise one or both of the DC link capacitors will be short-circuited which is not allowed. Then the switching modes of the power switches in a T-type H-bridge to produce a 5-level output voltage is listed in Table I.

III. SWITCHING STRATEGY FOR T-TYPE H-BRIDGE BASED CASCADED MULTILEVEL CONVERTERS

A. Switching Scheme for the Single-Phase T-type H-Bridge

A unipolar CPS-SPWM based switching scheme is proposed for the T-type H-bridge which is described with the aid of Fig. 3. As can be seen from Fig. 3(a), two triangle carrier signals, V_{c1} and V_{c2}, are required for the two virtual single-phase full-bridges. The two carrier signals are time shifted by $T_c/4$, where T_c is the period of these carrier signals, and the two virtual full-bridges share the same modulating sinusoidal signals V_{mL} and V_{mR}. With the unipolar CPS-SPWM implemented, the three-level output of the two virtual full-bridges can be achieved, noted as V_{3L-1} and V_{3L-2} in Fig. 3(b), respectively. The sum of the two virtual full-bridge outputs is a five-level signal noted as V_{5L} in Fig. 3(b), which is exactly the output target of the T-type H-bridge. Then the PWM signals for the active switches in the T-type H-bridge can be obtained by reverse derivation according to its switching modes.

It should be noted from Tab. I that there is only one switching state feasible for each non-zero-level output, but there are two switching states available for the zero-level output. In order to reduce the switching losses, the principle of "changing the minimum number of switch status to achieve an output level" should be followed, which means that the switching state to generate the zero-level output must be properly selected.

Considering all of these technical details, when the output voltage changes among non-negative levels, the active switch T_4 or anti-parallel diode D_4 is always turned on, while T_2 and D_2 are turned off:

1) To generate +2*E* levels, T_1 (or D_1) turns on, and T_3 (& D_3) and T_5 (& D_5) turn off;

2) To generate +*E* levels, T_5 (or D_5) turns on, and T_1 (& D_1) and T_3 (& D_3) turn off;

3) To generate 0 levels, T_3 (or D_3) turns on, and T_1 (& D_1) and T_5 (& D_5) turn off.

Conversely, when the output voltage changes among non-positive levels, the active switch T_2 (or D_2) is always turned on, while T_4 (& D_4) are turned off:

4) To generate 0 levels, T_1 (or D_1) turns on, and T_3 (& D_3) and T_5 (& D_5) turn off;

5) To generate -*E* levels, T_5 (or D_5) turns on, and T_1 (& D_1) and T_3 (& D_3) turn off;

6) To generate -2*E* levels, T_3 (or D_3) turns on, and T_1 (& D_1) and T_5 (& D_5) turn off.

Then the algorithm to generate PWM control signals for the T-type H-bridge is proposed whose flowchart is shown in Fig. 3(c). The algorithm works at each simulation step or each clock pulse of the field programmable gate array (FPGA) when practically implemented. PN is a binary (0-1) variable which is typically defined so that 1 means that the output voltage

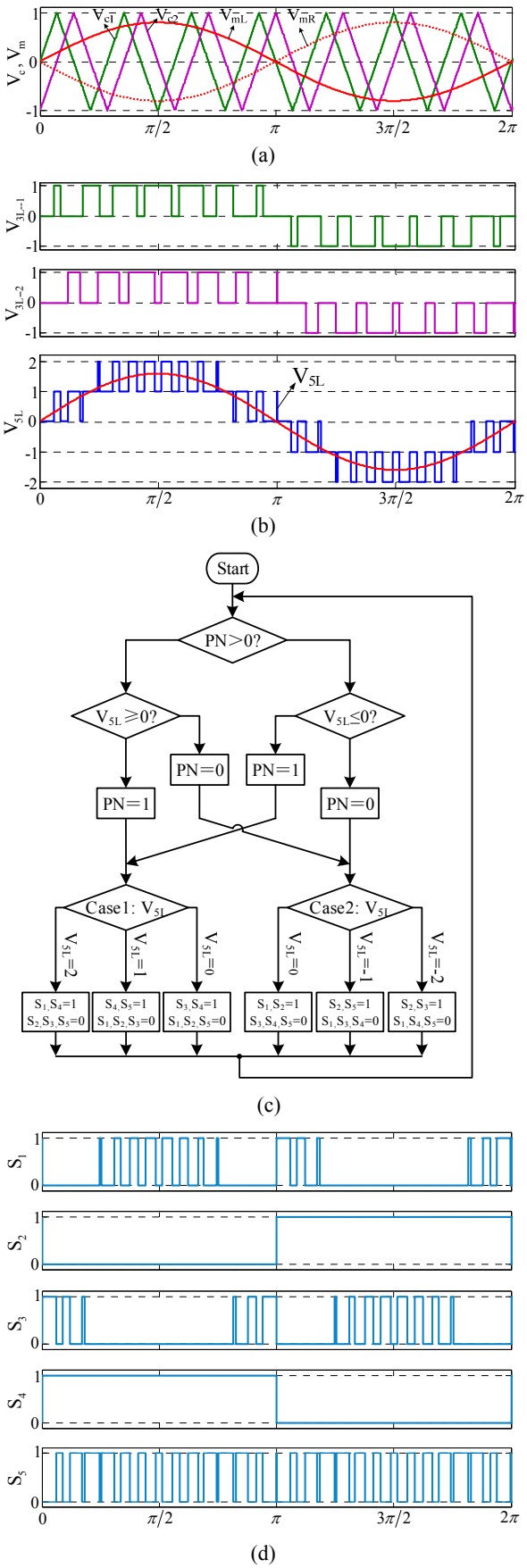


Fig. 3. CPS-PWM based switching scheme for T-type H-bridge.

changes among non-negative levels, while 0 means the output voltage changes among non-positive levels. PN is a binary (0-1) variable which is typically defined so that 1 means that V_{5L} is non-negative, while 0 means that V_{5L} is non-positive. When PN is 1 at the current simulation step or clock pulse of the FPGA, it judges whether V_{5L} is non-negative or not. PN is kept at 1 when the judgment result is true and it enters to the 'Case1' step. Meanwhile, PN is set to 0 when the judgment result is false and it enters the 'Case2' step. Vice versa, when PN is 0 at the current simulation step or clock pulse of the FPGA, it judges whether V_{5L} is non-positive or not. PN is kept at 0 if the judgment result is true and it enters to the 'Case2' step. Meanwhile, PN is set to 1 when the judgment result is false and it enters to the 'Case1' step. Finally, thanks to the switch-case algorithm, the PWM signals for the T-type H-bridge can be obtained as in Fig. 3(d).

B. T-type H-bridge Cascaded Converter and its Modulation

Fig. 4 shows the main structure of a T-type H-bridge cascaded single-phase multilevel converter which consists of N T-type H-bridge modules connected in series.

The modulation scheme plays an essential role in generating a multilevel output voltage which has a rather high equivalent switching frequency for the cascaded converter. The modulation strategy for each T-type H-bridge in the cascaded converter is the proposed scheme previously described, where the difference is the initial phase angle of the triangle carrier signal. As in Fig. 5, V_{mL} and V_{mR} are modulating sinusoidal signals, V_{c11} and V_{c12} are the carrier signals for the first T-type H-bridge, while V_{ck1} and V_{ck2} are the carrier signals for the k-th T-type H-bridge (k=1,2,⋯). The two carrier signals V_{ck1} and V_{ck2} are time shifted by $T_c/4$. In addition, V_{ck1} and V_{ck2} lag behind the corresponding carriers for the first T-type H-bridge (V_{ck1} and V_{ck2}), with the same phase-shift time φ_k which is calculated as (2), where N is the cascading number. Finally, $V_{5L\text{-}1}$ and $V_{5L\text{-}k}$ are the virtual five-level signals for the first and k-th T-type H-bridges, respectively.

$$\varphi_k = \frac{k-1}{4N}\cdot T_c \qquad (1 \le k \le N) \tag{2}$$

C. Simulation Analysis of the Proposed Modulation Strategy

In order to verify the validity of the proposed modulation scheme, a single-phase cascaded converter system is simulated in Matlab/Simulink. The DC input voltage is supplied by independent voltage sources (E=1000V), the fundamental frequency is set to 50 Hz, the modulation frequency (f_s) is 1.0 kHz, and the modulation index (m) set as 0.9.

Fig. 6 shows the output voltage and its spectrums of a single T-type H-bridge. Similarly, the output voltage and its spectrums of a multilevel converter cascading two T-type H-bridges (N=2) is shown in Fig. 7. The output voltage of the latter is a lot closer to a sinusoidal waveform because it has

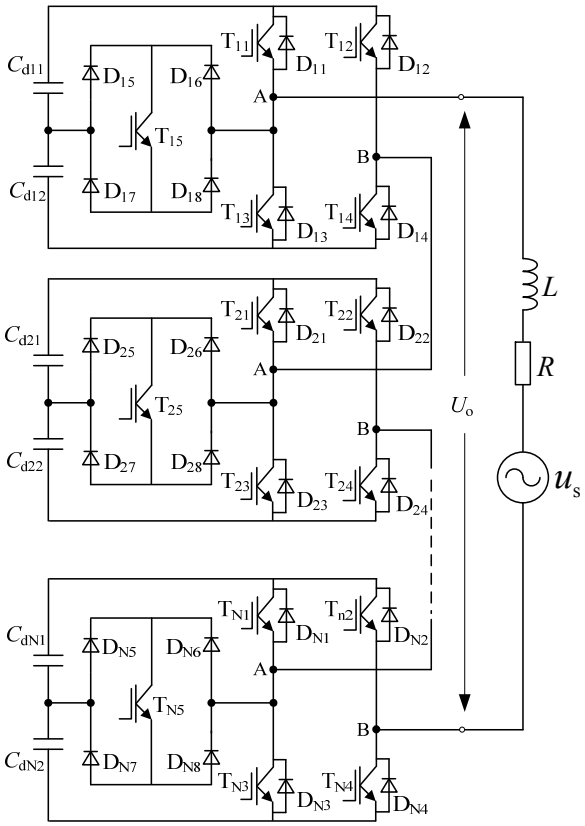


Fig. 4. Topology of T-type H-bridge based cascaded multilevel converter.

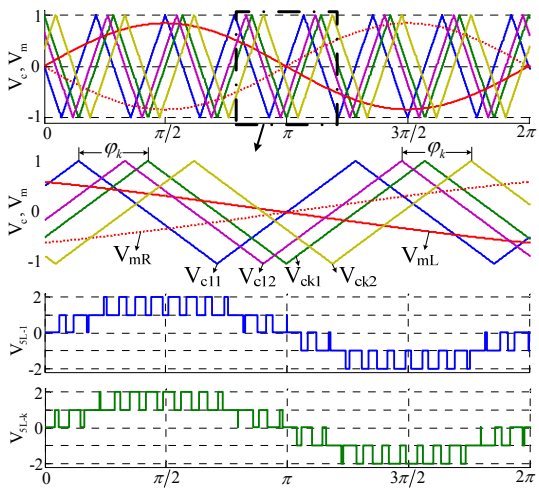


Fig. 5. Carriers and five-level signals for the first and k-th T-type H-bridges in a cascaded multilevel inverter.

more voltage levels. It is obvious from the two figures that the harmonics of the single H-bridge inverter output voltage only appear at the sidebands centered around a frequency of 4 kHz ($2f_s$) and its multiples, while the harmonics of the cascaded converter output voltage only appear around 8 kHz ($2Nf_s$), 16 kHz, and so on. Therefore, the resultant output voltage of the T-type H-bridge cascaded multilevel converter has a rather high equivalent switching frequency, even if the switching frequency of the individual active switch is not very high.

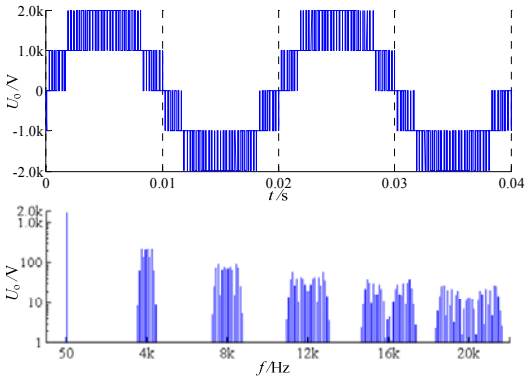


Fig. 6. Output voltage and its spectrums of a single T-type H-bridge.

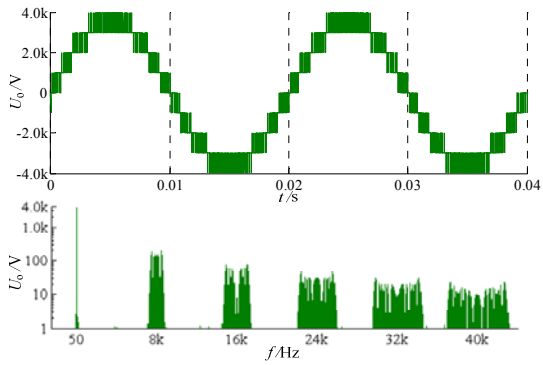
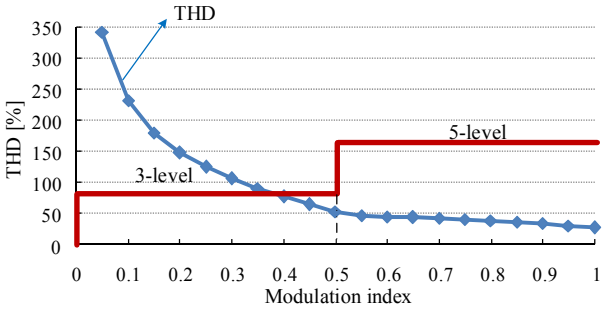


Fig. 7. Output voltage and its spectrums of a cascaded multilevel converter.

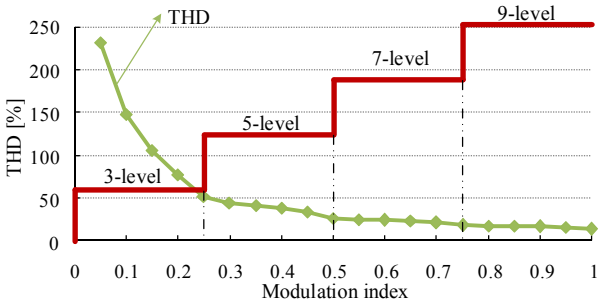
Fig. 8 shows the total harmonic distortion (THD) and voltage level for the output voltage with the simulation of a single T-type H-bridge and its cascaded multilevel converter with different values for the modulation index. With an increase of the modulation index, the voltage THD decreases, and the output voltage becomes closer to a sinusoidal waveform with more voltage levels. For a single T-type H-bridge, the output voltage is 3-level when the modulation index is less than 0.5, and the output voltage remains 5-level when the modulation index exceeds 0.5. For a multilevel converter which cascades two T-type H-bridges, the output voltage can be 3-level, 5-level, 7-level and 9-level with the modulation index boundaries of 0.25, 0.5 and 0.75. In addition, the voltage THD of the T-type H-bridge cascaded multilevel converter is much lower than that of a single T-type H-bridge with the same modulation index.

IV. Control Strategy for the T-type H-bridge Based Cascaded SVG

To verify the operation performance of a T-type H-bridge with a load current, a single-phase cascaded multilevel SVG based on a T-type H-bridge, as shown in Fig. 4, is studied in this paper. The SVG is connected to a single-phase AC source though an inductor L (with an equivalent resistance R) which makes an essential contribution to the filtering out of switching ripples.



(a) Single T-type H-bridge.



(b) Two T-type H-bridge cascaded multilevel converter.

Fig. 8. THD and voltage level for output voltage with different values of modulation index.

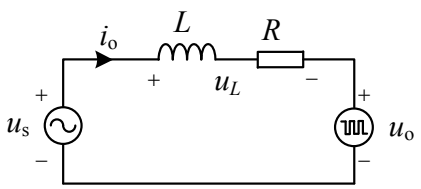


Fig. 9. Equivalent circuit of the single-phase SVG.

The equivalent circuit of a single-phase SVG is described in Fig. 9. When in operation, the DC-link voltage is stabilized at a given value, and T-type H-bridges switches according to the pulses generated by the proposed modulation scheme to obtain the desired output voltage u_o.

From Fig. 9, the time-domain model of a SVG is written in (3) based on based on Kirchhoff's Voltage Law (KVL). Then a s-domain transfer function of the controllable voltage source u_o to the grid current i_o can be derived as (4).

$$u_o - u_s = L\frac{\mathrm{d}i_o}{\mathrm{d}t} + Ri_o \tag{3}$$

$$G_P(s) = \frac{i_o(s)}{u_o(s)} = \frac{1}{Ls + R} \tag{4}$$

The entire control of the cascaded SVG is divided mainly into the following two parts: reactive-current control and DC-link voltage control.

A. Compound Current Control Strategy

Generally, the current reference of a single-phase SVG is a sinusoidal component, and there is no doubt that a proportional integral (PI) controller in the stationary frame

cannot track it with zero steady-state error. Originating from the internal model principle, the repetitive (REP) controller is well known as an effective solution for the rejection of periodic errors [22].

Therefore, the REP controller based compound current control strategy is designed to acquire high-precision performance. As shown in Fig.10, the compound current control strategy consists of a PI inner loop and a REP outer loop, where $i_{ref}(z)$ is current reference and $i_c(z)$ is output current.

For the PI inner loop, $G_P(z)$ is the control plant of the single-phase SVG, $PI(z)$ is the PI controller, and z^{-1} is the inherent unit delay of the digital implementation. The REP outer loop is composed with an internal model, a fundamental period delay element (z^{-M}) and a corrector ($z^hS(z)$), where M is the number of samples in one fundamental period, and $Q(z)$ is attenuation filter, which is usually a constant smaller than the unit.

In the compound current control, the PI inner loop plays a major role in tracking the fundamental signal and provides a stable control plant for the outer REP loop. The outer REP loop is responsible for improving the tracking accuracy. Considering that the compensation current is mainly 50Hz (grid frequency), it seems a wise choice to maintain good effects only at low frequencies. In addition, at medial and high frequencies the controller gain falls off sharply to avoid any chance of breaking the system stability condition.

Consequently, the desired bode diagram of the compound controller should have zero gain and zero phase shift at low frequencies, with the gain decreasing quickly and the phase shift trying to stay zero at medial and high frequencies. In practice, a conventional second-order filter $S(z)$ is required for high frequencies attenuation and z^{-M} provides the condition for using the leading element (z^h) to compensate the phase lag of the control because the ac signal is periodically repetitive in the steady-state.

From Fig. 10, the closed loop transfer function of the compound current control $G_{com}(z)$ is derived as follows.

$$\begin{cases} G_{com}(z)=\dfrac{1-z^{-M}Q(z)}{1-z^{-M}H(z)}\cdot\dfrac{1}{1+G_{PI}(z)} \\ H(z)=Q(z)-z^hS(z)G_{PIc}(z) \\ G_{PIc}(z)=\dfrac{G_{PI}(z)}{1+G_{PI}(z)} \\ G_{PI}(z)=z^{-1}PI(z)G_P(z) \end{cases} \tag{5}$$

where $G_{PI}(z)$ and $G_{PIc}(z)$ are the open-loop and closed-loop transfer functions of the PI inner loop, respectively. The PI controller is designed according to the zero-poles cancellation method with a cut-off frequency of 400Hz, the cut-off frequency and damping ratio of $S(z)$ are ω_n=2400π and ζ=0.707. In addition, $Q(z)$=0.92, M=200, h=7.

Fig. 11 shows a bode plot of $G_{PIc}(z)$ and $z^hS(z)G_{PIc}(z)$. The frequency characteristics of $z^hS(z)G_{PIc}(z)$ indicate zero gain and zero phase shift at low frequencies, with the gain descending abruptly at medial and high frequencies as depicted above.

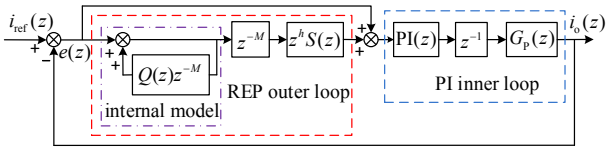


Fig. 10. Compound current control strategy for SVG.

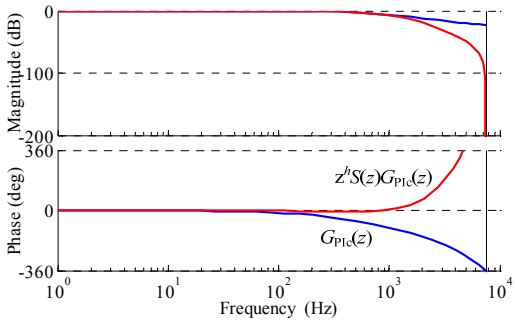


Fig. 11. Frequency characteristics of the compound current controller.

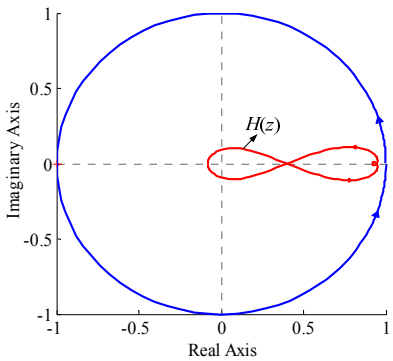


Fig. 12. Nyquist diagram of H(z).

From (3), a sufficient condition for system stability can be given as:

$$\left\|H(z)\right\|<1,\ z=e^{j\omega T_s},\omega\in(-\pi/T_s,\pi/T_s) \tag{6}$$

Using the above design parameters, a Nyquist diagram of $H(z)$ is plotted by MATLAB as shown in Fig. 12. In this figure, the locus of $H(z)$ is always inside the unity circle. As a result, the system is stable. In addition, the fairly large distance from the locus of $H(z)$ to the unity circle denotes a sufficiently large stability margin.

B. DC-link Voltage Control Strategy

The DC-link voltage control of a T-type H-bridge cascaded SVG can be classified into total voltage balancing control and balancing control among the T-type H-bridges as well as balancing control inside a T-type H-bridge. The former two have been widely studied in traditional H-bridge cascaded SVGs, and it is not necessity to introduce them in detail [23].

However, the T-type H-bridge has split-capacitor-type DC-link capacitors. The DC-link voltage balancing control

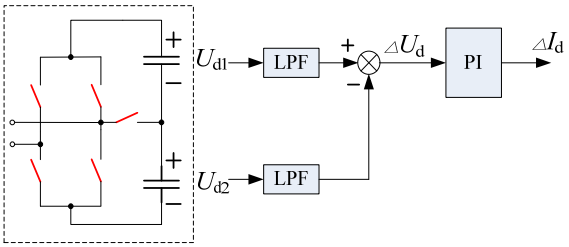


Fig. 13. DC-link voltage balancing control strategy of a T-type H-bridge.

inside a T-type H-bridge is of great importance for the proper operation of a cascaded SVG. For each mode, as shown in Fig. 2, it is set as a positive current (i_c>0) when the current is flowing from the AC source to the bridge arm A (Fig. 2 (d) as example).

In modes (a), (b), (e) and (f), the current flowing through the top capacitor (C_{d1}) and bottom capacitor (C_{d2}) are the same. Thus, it would not destroy the balancing of the two capacitors. In other cases, the conclusion is no longer valid. When i_c<0, the current only charges the top capacitor (mode (g)) or just discharges the bottom capacitor (mode (c)). In other words, the DC-link voltage of the top capacitor rises while that of the bottom capacitor falls. Conversely, the DC-link voltage of the bottom capacitor rises (mode (d)) while that of the top capacitor falls (mode (h)) when i_c>0.

It can be concluded that when there is no DC component in the output current of the SVG, the voltage of the split-capacitors is automatically balanced. However, a voltage ripple exists due to the sinusoidal reactive current exchanges between the SVG and the AC source, and the average value during a fundamental period is a constant. Meanwhile, the voltage balance of the split-capacitors will be destroyed when there is some DC component in the output current. In addition, several factors such as the difference of the split-capacitors, the switching loss, the parallel loss, and the time delay of the drive pulse may cause voltage unbalance of split-capacitors.

In order to eliminate the voltage unbalance, a proper DC component should be added to the current reference to balance the charge and to discharge of each the DC-link capacitors, and maintain the balance of the DC-link voltage inside the T-type H-bridge. The DC-link voltage balancing control strategy is described in Fig. 13.

The DC-link voltage inside a T-type H-bridge can be well balanced with the proposed controller. When there is a DC-link voltage unbalance between the two capacitors, U_{d1}>U_{d2} for instance, the difference $\triangle U_d$ is larger than zero, and consequently the output of the PI controller is positive. In other words, a positive DC component is added to the current reference which may charge the bottom capacitor but discharge the top capacitor. Finally U_{d1} becomes equal to U_{d1}, and vice versa.

From the above analysis, the relationship between the DC current component and the DC-link voltage difference is:

$$C_{d1}\frac{dU_{d1}}{dt}-C_{d2}\frac{dU_{d2}}{dt}=i_d \tag{7}$$

When translated to the s-domain (C_{d1}=C_{d2}=C_d), this can be written as:

$$\frac{C_d}{2}s\Delta U_d(s)=i_d(s) \tag{8}$$

Then the transfer function of the control plant for the DC-link voltage balancing control can be obtained by:

$$G_d(s)=\frac{\Delta U_d(s)}{i_d(s)}=\frac{2}{C_d s} \tag{9}$$

It can be seen that the control plant is a first-order integrator whose cut-off frequency depends on the value of the DC-link capacitor. The main component of the T-type H-bridge cascaded SVG output current is the grid frequency reactive current, while the control object of the DC-link voltage unbalancing control system is the DC component. Therefore, a PI controller is required to provide zero error tracking for the DC component. However, it should not disturb the current control loop. This means that a low bandwidth DC-link PI controller is a wise choice. In practice, low pass filters (LPFs) can be employed for medium and high frequency attenuation.

V. Simulation and Experimental Results

A simulation model and a prototype, as shown in Fig. 14, of a single-phase SVG cascading two T-type H-bridges is built and tested with the proposed modulation and control strategy.

Firstly, it acts as a multilevel inverter unconnected to an AC source to verify the proposed modulation strategy, and a DC-link voltage is supplied by transformer-isolated diode-rectifiers parallel connected to each of the DC-link capacitors (E=120V). Then it works as the SVG connected with an AC source generated by the regulator when the DC-link voltage is self-balanced with the proposed balancing control strategy. The prototype is controlled by a concentrated control platform composed of a digital signal processing (DSP) from TI (TMS320F2812) and a FPGA from ALTERA. Table II lists some of the main parameters of the SVG simulation model as well as the prototype system.

A. Simulation Results

Simulation waveforms and spectrums of the output voltage for a single T-type H-bridge and its cascaded converter have been given in Fig. 6 and Fig. 7, respectively. Fig. 15 shows the simulation results of the T-type H-bridge cascaded SVG. It can be seen that the output current changes from capacitive reactive to inductive reactive at t=0.5s, where u_s is the source voltage, i_o is the SVG output current, u_c is the SVG output voltage, u_{dc}, u_{d1} and u_{d2} are the total DC-link voltage and DC-link voltage of the split capacitors of a T-type H-bridge, respectively. The DC-link voltage is well balanced during the

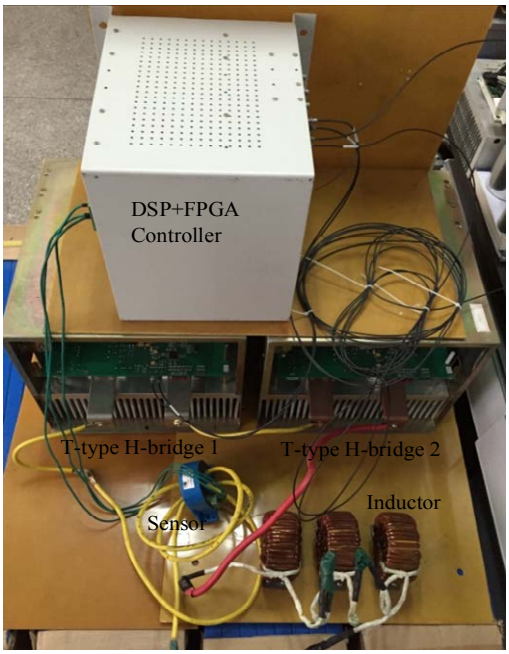


Fig. 14. Photo of T-type H-bridge cascaded single-phase SVG prototype.

TABLE II
MAIN PARAMETERS OF SVG PROTOTYPE SYSTEM

AC source voltage (u_s, RMS)	280 V
Source frequency (f_o)	50 Hz
AC inductor (L)	2 mH
Equivalent resistance (R)	15 $m\Omega$
DC-link capacitor (C_d)	5.0 mF
DC-link voltage (E)	240 V
Cascading number (N)	2
Dead time of CPS-SPWM	2 μs
Switching frequency (f_s)	1.0 kHz
Equivalent Switching frequency (f_{sequ})	8.0 kHz
Sampling frequency (f_{sam})	10.0 kHz

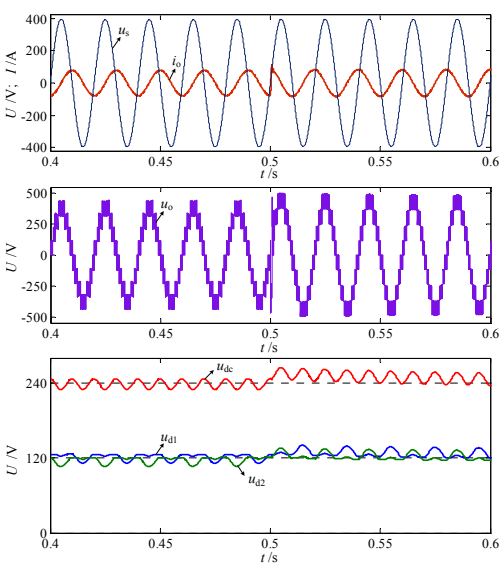


Fig. 15. Simulation results of T-type H-bridge based cascaded SVG.

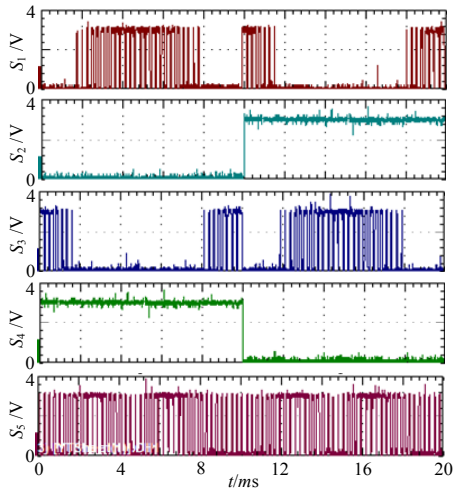


Fig. 16. PWM signals for a single T-type H-bridge.

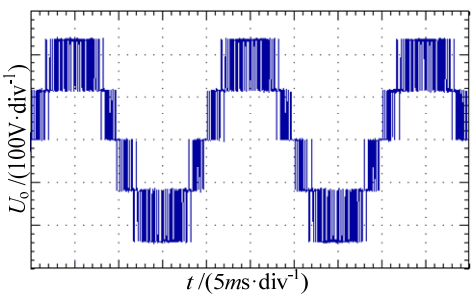


Fig. 17. Output voltage of single T-type H-bridge r (m=0.9).

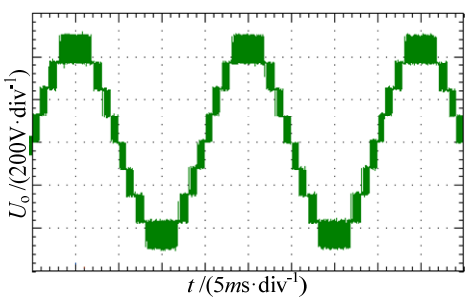
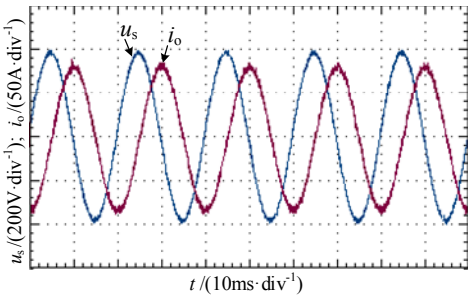


Fig. 18. Output voltage of T-type H-bridge based cascaded multilevel converter (m=0.9).

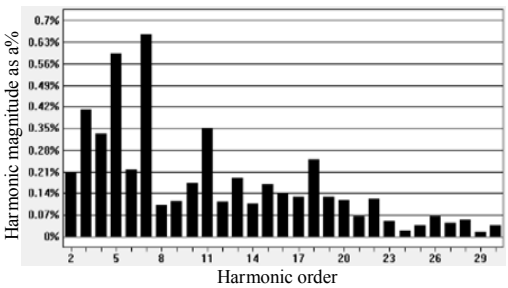
whole process. A ripple of double the grid frequency in the total DC-link voltage is generally due to the reactive current exchanges between the SVG and the AC source.

B. Experimental Results

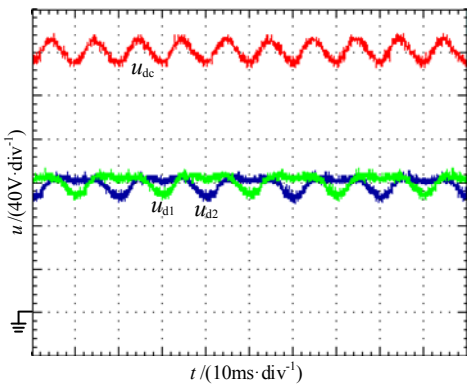
Fig. 16 shows PWM signals generated by the FPGA for a single T-type H-bridge with a modulation index of m=0.9. The corresponding output voltage of the single T-type H-bridge is shown in Fig. 17. In addition, Fig. 18 shows the 9-level output voltage of the T-type H-bridge based cascaded multilevel converter. All of the experimental results are consistent with the simulation results. Consequently, both the simulation and experimental results confirm the validity and feasibility of the proposed modulation strategy for the T-type H-bridge and its cascaded converter.



(a) Source voltage and SVG output current.

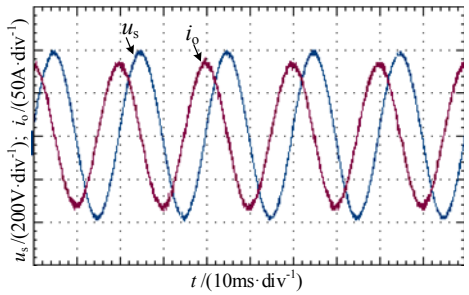


(b) Spectrums analysis of SVG output current.

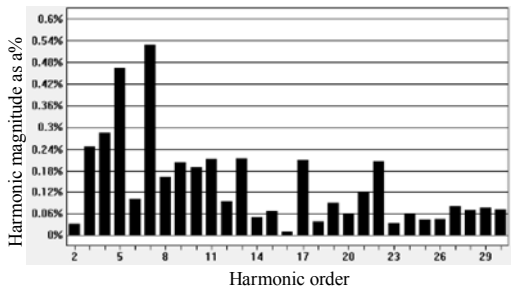


(c) DC-link voltage of a T-type H-bridge.

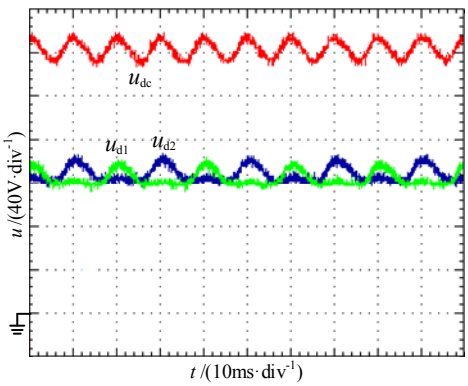
Fig. 19. Experimental waveforms when SVG outputting inductive reactive current.



(a) Source voltage and SVG output current.



(b) Spectrums analysis of SVG output current.



(c) DC-link voltage of a T-type H-bridge.

Fig. 20. Experimental waveforms when SVG outputting capacitive reactive current.

Fig. 19 and Fig. 20 show experimental waveforms when the single-phase cascaded SVG outputs inductive reactive current and capacitive reactive current, respectively. A spectrum analysis indicates that the THD of the SVG output current is less than 1.8%. In addition, the DC-link voltage inside a T-type H-bridge of SVG is well balanced.

VI. Conclusions

This paper presents a novel CPS-PWM based control strategy for the T-type H-bridge converter. In the proposed method, a virtual five-level signal achieved by unipolar CPS-PWM is taking as the output object, and PWM signals for the T-type H-bridge can be obtained by reverse derivation according to its switching modes following the principle of "changing the minimum number of switch status to achieve an output level." In addition, the modulation scheme for the T-type H-bridge based cascaded multilevel converter is introduced. Then a single-phase T-type H-bridge cascaded multilevel SVG prototype is designed with the repetitive controller based compound current control strategy and the DC-link voltage balancing control scheme analyzed. Finally, the validity and feasibility of the proposed modulation and DC-link voltage balancing control strategy are confirmed by simulation and experimental results.

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