JPE 16-6-9

http://dx.doi.org/10.6113/JPE.2016.16.6.2076
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Common-Mode Voltage Elimination for Medium-Voltage Three-Level NPC Inverters Based on an Auxiliary Circuit

Quoc Anh Le*, Sangmin Lee*, and Dong-Choon Lee†

*,†Department of Electronic Engineering, Yeungnam University, Gyeongsangbuk, Korea

Abstract

In this paper, a novel scheme to eliminate common-mode voltage (CMV) is proposed for three-level neutral-point clamped (NPC) inverters. In the proposed scheme, a low-power full-bridge converter is utilized to produce compensatory voltage for CMV, which is injected into an NPC inverter through a single-phase four-winding transformer. With the proposed circuit, the power range for applications is not limited, and the maximum modulation index of the inverter is not reduced. These features are suitable for high-power medium-voltage machine drives. The effectiveness of the proposed method is verified by simulation and experimental results.

Key words: Active circuit, Common-mode voltage, High-power medium-voltage drives, Neutral-point clamped inverter, Space vector modulation

I. INTRODUCTION

High-power medium-voltage induction machine drives are widely utilized in industrial applications because of the development of multilevel inverters with high-speed switching devices [1]-[4]. Pulse-width modulation (PWM) voltage-source inverters (VSIs), especially neutral-point clamped (NPC) inverters, are popularly used; these inverters present high output performance [1]-[5]. However, PWM inverters generate common-mode voltage (CMV), which may cause serious problems, such as leakage current through stray capacitors, bearing current, shaft voltage, and motor winding-to-ground voltages [6]-[17]. Therefore, the CMV of VSIs must be reduced or eliminated to preserve the life time of motors and transformers.

Many of the solutions proposed to reduce or cancel CMV can be classified into modulation approaches and auxiliary circuit schemes. In modulation techniques, only voltage vectors producing low CMV are utilized [6], [18], [19]. The peak and root mean square (RMS) values of CMV are reduced, whereas the fundamental voltage component is retained. However, these methods cannot fully eliminate the CMV of inverters. Other CMV elimination methods have been proposed to cancel leakage current by utilizing only the zero- and medium-voltage vectors of three-level NPC inverters [20, 21]. Although the leakage current can be fully cancelled by these techniques, the use of the DC-link voltage is only 86.6% due to the exclusion of large-voltage vectors. Another drawback of modulation approaches is the increase in the switching losses and total harmonics distortion (THD) of the output voltage.

Meanwhile, CMV elimination methods based on auxiliary circuits with complementary-symmetry transistors have been recommended for two-level inverters [7, 9]. With additional circuits, the CMV of inverters can be fully eliminated without any adverse effect on the fundamental component of the output voltage. However, auxiliary circuits cannot be applied to medium-voltage inverters because of the power limit of the complementary-symmetry transistors. In addition, the transformer in the auxiliary circuit must be carefully designed because of the power dissipation constraint of the transistors.

In this study, a novel scheme for CMV elimination in three-level NPC inverters is proposed; the scheme involves the use of an auxiliary circuit and modified space-vector pulse-width

Manuscript received May 13, 2016; accepted Jul. 9, 2016
Recommended for publication by Associate Editor Kyo-Beum Lee.
†Corresponding Author: dclee@yu.ac.kr
Tel: +82-53-810-2582, Fax: +82-53-810-4767, Yeungnam University
*Dept. of Electrical Engineering, Yeungnam University, Korea

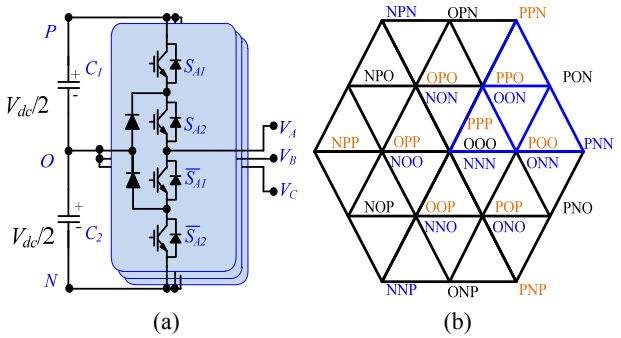

Fig. 1. Three-phase three-level NPC inverters. (a) Circuit. (b) Space voltage vector diagram.

TABLE I
SWITCHING STATES OF THREE-LEVEL NPC INVERTERS

Switching states	S_{A1}	S_{A2}	Pole voltage (v_{AO})
P	1	1	$V_{dc}/2$
O	0	1	0
N	0	0	$-V_{dc}/2$

modulation (SVPWM) [17] and is applicable to medium-voltage inverter systems. The auxiliary circuit consists of a common-mode transformer (CMT) and a low-power H-bridge converter to generate compensatory CMV. The modified SVPWM of the NPC inverter is utilized to reduce the peak value of CMV. The proposed method is verified by simulation results for a high-power three-level NPC inverter and experimental results for a prototype hardware.

II. THREE-LEVEL NPC INVERTERS

A. Structure of NPC Inverters

NPC inverters are widely utilized in high-power medium-voltage applications [1]-[5]. The simplified structure of three-phase, three-level NPC inverters (Fig. 1(a)) includes two common capacitors arranged in a series for the DC link and three phase legs. Each phase leg involves four active switches with antiparallel diodes connected in a series and two clamped diodes connected to the neutral point of the DC link. The four active switches are separated into two complementary pairs, namely, S_{A1} and $\overline{S}_{A1}$ and S_{A2} and $\overline{S}_{A2}$. The switching states and pole voltages of phase leg "A" are provided in Table I, where "1" and "0" denote the on-state and off-state of the switches, respectively.

B. SVPWM with Seven-Segment Switching Pattern

An NPC inverter produces 27 voltage vectors for modulation (Fig. 1(b)) [4] generated from the switching states of the three phase legs. These voltage vectors are classified as zero, small, medium, and large according to their magnitude (Table II).

For modulation, the hexagon in the space vector diagram is divided into six triangular sectors, which are further split into

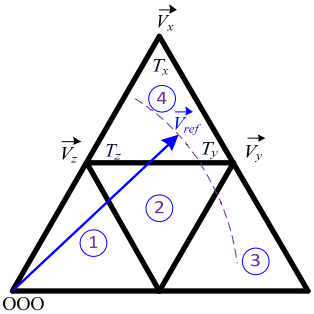

Fig. 2. Voltage vector in sector 1 for SVPWM of three-level NPC inverters.

TABLE II
CLASSIFICATION OF VOLTAGE VECTORS FOR NPC INVERTERS

Group	*Voltage vectors*	CMV value	Vector magnitude
Zero-voltage vector	NNN	$-V_{dc}/2$	*0*
	OOO	0	
	PPP	$V_{dc}/2$	
Small voltage vector	ONN	$-V_{dc}/3$	$V_{dc}/3$
	NNO		
	NON		
	OON	$-V_{dc}/6$	
	NOO		
	ONO		
	POO	$V_{dc}/6$	
	OPO		
	OOP		
	PPO	$V_{dc}/3$	
	OPP		
	POP		
Medium voltage vector	PON	0	$\frac{V_{dc}}{\sqrt{3}}$
	OPN		
	NPO		
	NOP		
	ONP		
	PNO		
Large voltage vector	PNN	$-V_{dc}/6$	$2V_{dc}/3$
	NPN		
	PPN		
	NNP	$V_{dc}/6$	
	NPP		
	PNP		

four small triangular regions composed of three voltage vectors at the vertices (Fig. 1(b) and Fig. 2, respectively) [4]. Therefore, the reference voltage vector can be synthesized by the nearest three voltage vectors based on the "voltage-second balance," which is expressed as

$$\vec{V}_{ref}T_S = \vec{V}_x T_x + \vec{V}_y T_y + \vec{V}_z T_z, \qquad T_S = T_x + T_y + T_z \tag{1}$$

where T_x, T_y, and T_z are the dwell times of vectors $\vec{V}_x, \vec{V}_y$, and $\vec{V}_z$, respectively, at the vertex of the triangle where the reference voltage vector is located. The voltage vectors and their dwell time are determined. Then, the seven-segment SVPWM of the NPC inverter is selected to reduce the THD

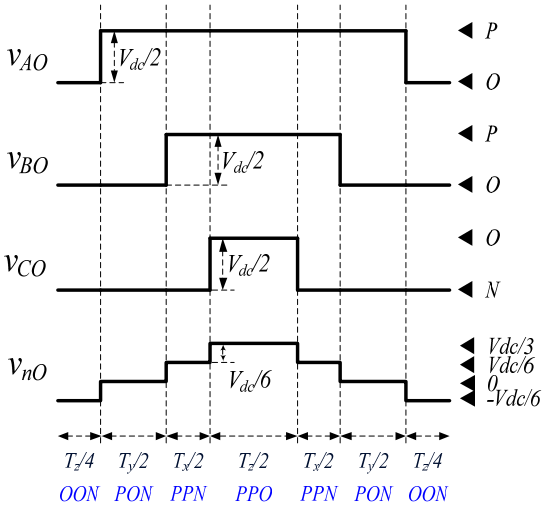

Fig. 3. Pole voltages and CMV in three-level NPC inverters with seven-segment switching sequence.

and switching losses of the inverter, the pole voltage of which is shown in Fig. 3.

C. CMVs

For the machine drive system, the CMV of the NPC inverter, v_{nO}, is defined as the voltage difference between the neutral point of the machine and the mid-point of the DC link in the inverter; it is expressed as the average of the three-phase pole voltages as follows:

$$v_{CMV} = v_{nO} = \frac{v_{AO} + v_{BO} + v_{CO}}{3}, \quad (2)$$

where v_{AO}, v_{BO}, and v_{CO} are the pole voltages of the inverter [18].

As listed in Table II, the large voltage vectors produce a CMV of $-V_{dc}/6$ or $V_{dc}/6$. The CMV generated by the small voltage vectors varies from $-V_{dc}/3$ to $V_{dc}/3$, except for the value of 0 V with a step change of $V_{dc}/6$. The medium voltage vectors and voltage vector [OOO] generate zero CMV. Normal seven-segment SVPWM for three-level NPC inverters usually produces four voltage levels of CMV in a switching cycle. As shown in Fig. 3, CMV, which includes four voltage levels, varies from $-V_{dc}/6$ to $V_{dc}/3$ with a voltage step of $V_{dc}/6$. By selecting other redundant small voltage vectors, the CMV of the inverters varies from $-V_{dc}/3$ to $V_{dc}/6$. With normal seven-segment SVPWM, a three-level NPC inverter generally produces CMV varying from $-V_{dc}/3$ to $V_{dc}/3$ with a voltage step of $V_{dc}/6$.

III. Existing CMV Elimination Methods Based on Active Circuits

An active circuit for CMV elimination that utilizes a pair of complementary transistors (Q_1 and Q_2), three capacitors (C_1), and a CMT (shown in Fig. 4) was introduced in [7]. In this circuit, the capacitors, C_1, are connected to detect the CMV at the inverter output terminals. The complementary-symmetry

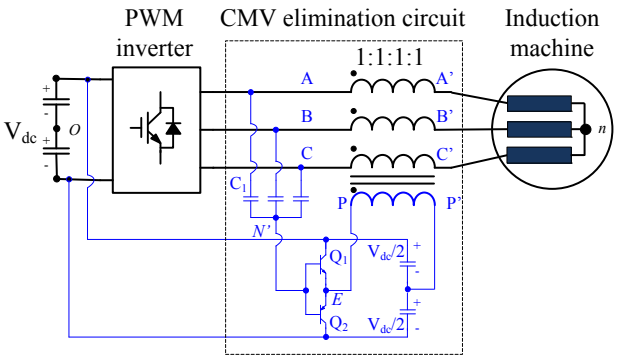

Fig. 4. Active circuit with linear devices for CMV elimination [7].

transistors, Q_1 and Q_2, operate in the linear region. Therefore, the emitter voltage of the transistors to the DC link mid-point, v_{EO}, is equal to the detected CMV of $v_{N'O}$ and the CMV of v_{nO}. The three secondary windings of the CMT are connected in series between the inverter output and the load terminals; thus, the CMV of the induction motor drive system, v_{nO}, can be eliminated by adding compensatory voltage for CMV to the primary winding of CMT.

An improved active circuit that can compensate for CMV through CMT with an appropriate turn ratio was presented in [9]. In the circuit, the voltage rating of the transistors is reduced compared with the DC-link voltage of the inverter, but the current rating of transistors is increased due to the change in the transformer turn ratio.

Although active circuits can successfully eliminate CMV, their application is limited because of the power rating of the transistors operating in the linear region. Furthermore, the CMT in these circuits requires a large magnetizing inductance. Thus, active circuits are inapplicable to medium-voltage motor drive systems.

IV. Proposed CMV Elimination Method

A. Modification of SVPWM for CMV Reduction

To reduce CMV, instead of using all 27 voltage vectors in the regular SVPWM, only 19 voltage vectors possessing a low CMV value are utilized [18]. The division of triangle regions for SVPWM is rearranged to reduce the level change in the CMVs. Therefore, the CMV varies only by two voltage levels, such as 0 V and $V_{dc}/6$ in a switching cycle or $-V_{dc}/6$ and 0 V in another cycle. However, this SVPWM method incurs increments in switching losses and THD because the three nearest voltage vectors are not utilized in several regions.

In this research, SVPWM was modified by dividing each sector into four equilateral triangles (Fig. 5) and utilizing 19 voltage vectors only. The three nearest voltage vectors were applied to the region of equilateral triangles; reduced THD and switching losses were thus obtained. With the modified SVPWM, the CMVs of the inverter vary among $-V_{dc}/6$, 0 V, and $V_{dc}/6$, as shown in Fig. 6. In addition, the switching losses of the NPC inverter with the five-segment switching pattern is

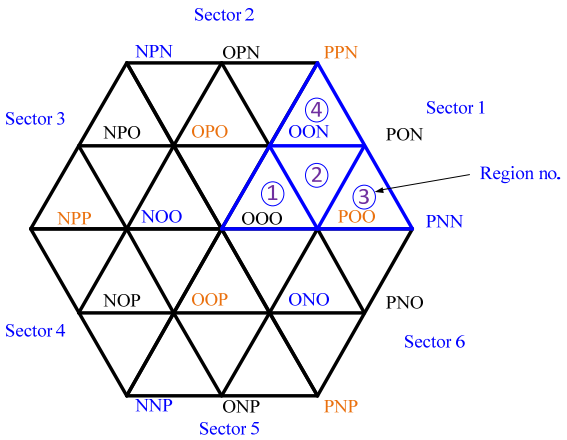

Fig. 5. Modified SVPWM utilizing only 19 voltage vectors for a three-level NPC inverter.

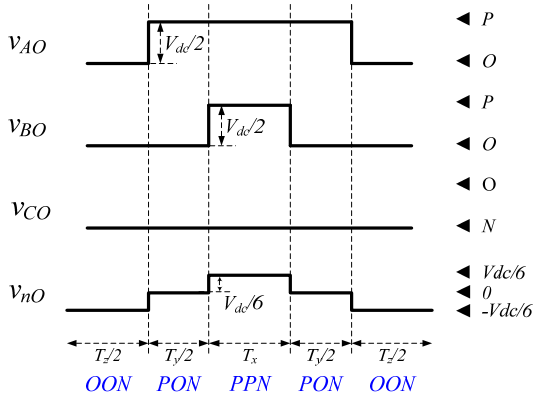

Fig. 6. Pole voltages and CMV in a three-level NPC inverter with a five-segment switching pattern in the modified SVPWM.

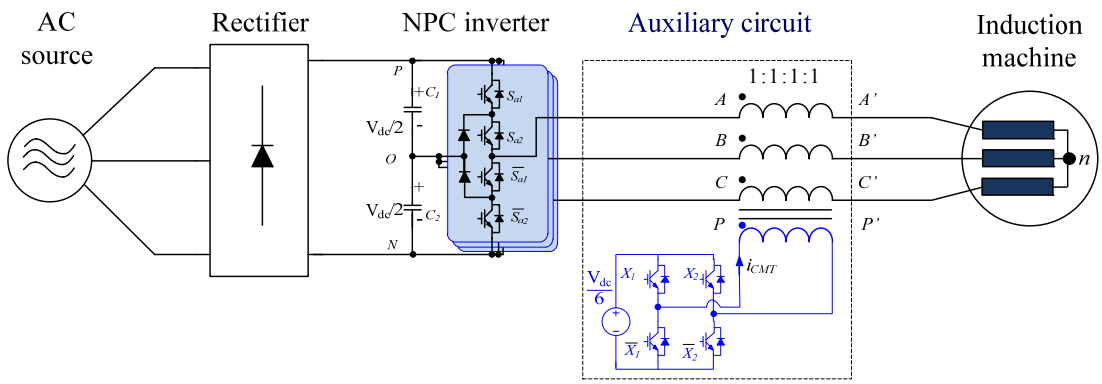

Fig. 7. Induction motor drive system with an auxiliary circuit for CMV elimination.

further reduced to two-thirds of those of the seven-segment pattern under identical PWM periods [4], [22]. Furthermore, the fundamental component of the output voltage is maintained similar to that in the normal seven-segment SVPWM. The neutral-point voltage can be balanced by adjusting an offset voltage [18].

B. Proposed Auxiliary Circuit

The CMV generated by the inverter can be eliminated with an auxiliary circuit, which can produce compensatory voltage for the CMV of the NPC inverter. For the three-level NPC inverter with the modified SVPWM, CMV varies among three-level voltages of $-V_{dc}/6$, 0, and $V_{dc}/6$, which can be fully eliminated by the auxiliary circuit generating the three-level voltages. In this work, an H-bridge converter with a DC input voltage of $V_{dc}/6$ is used to compensate for CMV, which can generate three-level voltages of $-V_{dc}/6$, 0, and $V_{dc}/6$.

The proposed circuit, shown in Fig. 7, is composed of an H-bridge converter with a DC voltage of $V_{dc}/6$ and a CMT. The H-bridge converter consists of X_1, $\overline{X}_1$, X_2, and $\overline{X}_2$ switches with two complementary pairs of X_1 and $\overline{X}_1$ and X_2 and $\overline{X}_2$. Notably, the additional DC source and H-bridge converter are rated at low power due to their low current requirements. The H-bridge converter feeds the primary winding of the CMT indicated as *PP'*. The secondary windings of the CMT are connected in series with the output terminal of the inverter to insert the compensatory CMV to the inverter output voltage.

C. Operating Principle of the Auxiliary Circuit

The H-bridge circuit can generate compensatory voltage, which is similar to the CMV produced by the NPC inverter with the modified SVPWM. That is,

$$v_{AA'} = v_{BB'} = v_{CC'} = v_{PP'} = v_{CMV}. \tag{3}$$

With the auxiliary circuit, the CMV of the NPC inverter system is modified from Equation (2) to

$$v_{CMV'} = \frac{v_{A'O} + v_{B'O} + v_{C'O}}{3}. \tag{4}$$

Substituting Equation (2) into Equation (4) yields

$$v_{CMV'} = \frac{-(v_{AA'} + v_{BB'} + v_{CC'})}{3} + v_{CMV}. \tag{5}$$

Substituting Equation (3) into Equation (5) yields

$$v_{CMV'} = 0. \tag{6}$$

The resulting expressions indicate that the CMV of the NPC inverter is eliminated successfully with the proposed method. The line-to-line voltage of the converter is unaltered and verified as

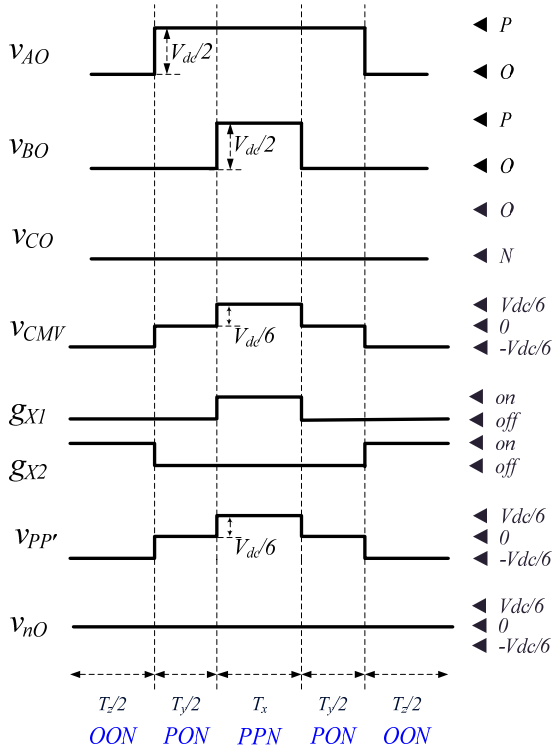

Fig. 8. Operating principle of the proposed method.

$$v_{A'B'} = v_{A'A} + v_{AB} + v_{BB'} = v_{AB}. \quad (7)$$

Eq. (3) can be implemented by a single-phase four-winding transformer supplied by an H-bridge circuit (Fig. 7).

To generate the compensatory voltage, the gating signals of the H-bridge converter depend on the switching states of NPC inverter voltages. The gating signal of g_{X1} is ON and that of g_{X2} is OFF for the voltage vectors producing a CMV of $V_{dc}/6$. Meanwhile, the gating signal g_{X2} is ON and that of g_{X1} is OFF for the voltage vectors generating a CMV of $-V_{dc}/6$. During the interval of the CMV with 0 V, the gating signals of g_{X1} and g_{X2} are either ON or OFF. By requiring these gating signals of the H-bridge converter, the dwell times of g_{X1} and g_{X2} can be obtained from T_x, T_y, and T_z given by the modified SVPWM of the NPC inverter.

Fig. 8 shows the operating principle of the proposed scheme. The three pole voltages, the CMV of the inverter, the gating signals of the H-bridge circuit, and compensatory voltage waveform $v_{PP'}$ are illustrated when the voltage reference is located in region ④ in Fig. 5. For voltage vector *OON* with a CMV of $-V_{dc}/6$, the gating signal g_{X1} is OFF and g_{X2} is ON during T_z. During the dwell time of T_y (state *PON*), the gating signals of g_{X1} and g_{X2} are OFF. For voltage vector *PPN*, by generating a CMV of $V_{dc}/6$, the gating signals of g_{X1} and g_{X2} are ON and OFF, respectively, during T_x. With these gating signals, the generated compensatory voltage $v_{PP'}$ is similar to the CMV of the NPC inverter, v_{CMV}, in terms of phase and magnitude. Therefore, CMV and its effects on the load are eliminated.

TABLE III
SYSTEM PARAMETERS FOR SIMULATION

Parameters	Values
DC input voltage	6,500 V
DC-link capacitance	3,000 μF
Switching frequency	2,000 Hz
Rated output frequency	60 Hz
Rated output voltage (V_{ll} rms)	4,160 V
Rated output power	2,000 kW

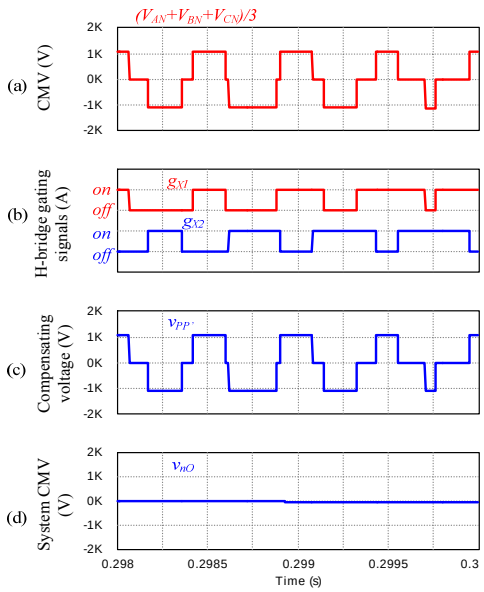

Fig. 9. Voltage waveforms for CMV compensation. (a) CMV generated. (b) Gating signals of the H-bridge converter. (c) Output voltage of the H-bridge converter. (d) CMV of the load.

V. SIMULATION RESULTS

PSIM simulation tests were conducted for the high-power medium-voltage NPC inverter system to verify the effectiveness of the proposed scheme. The parameters of the inverter used for simulation are listed in Table III.

Fig. 9 shows the voltage waveforms for the proposed method in four switching cycles. Fig. 9(a) displays CMV, which varies among three voltage levels of −1,083, 0, and 1,083 V. Fig. 9(b) shows the gating signals of the H-bridge converter, in which only g_{X1} is ON during positive CMV and only g_{X2} is ON during negative CMV. Meanwhile, both g_{X1} and g_{X2} are OFF when the CMV value is zero. Fig. 9(c) shows the output voltage waveform of the H-bridge converter applied to the primary windings of the CMT, $v_{PP'}$, by which the CMV of the load can be eliminated (Fig. 9(d)).

Fig. 10 illustrates the voltages and currents of the three-level NPC inverter with the normal seven-segment SVPWM method. The line-to-line voltage is shown in Fig. 10(a), in which five voltage levels of $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, and V_{dc} exist. The THD of the line-to-line voltage is 33.2%. Fig. 10(b) shows the three phase currents, which are sinusoidal and

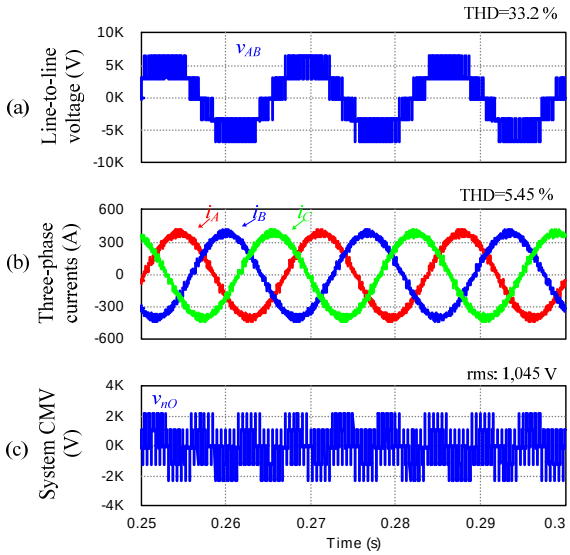

Fig. 10. Output performance of the NPC inverter with normal seven-segment SVPWM. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of the load.

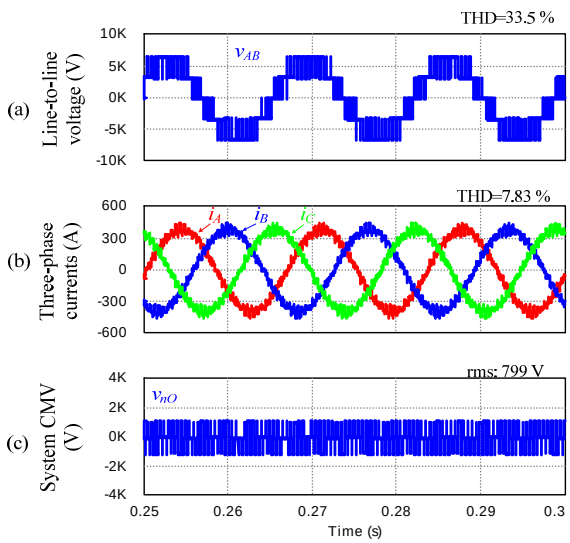

Fig. 11. Output performance of the NPC inverter with the modified SVPWM. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of the load.

balanced, with a THD of 2.25%. Fig. 10(c) shows the CMV of the inverter that varies from −2,167 V to 2,167 V with five voltage steps. The RMS value of the CMV is 1,045 V.

The simulation results for the NPC inverter with the modified SVPWM without the auxiliary circuit are illustrated in Fig. 11. Fig. 11(a) shows the line-to-line voltage, which is similar to that that in Fig. 10(a); its THD is 33.2%. Fig. 11(b) displays the three phase currents, which are sinusoidal and balanced; their THD increases to 3.25% because of the five-segment switching pattern. Fig. 11(c) shows the CMV of the inverter that varies from −1,063 V to 1,063 V with three voltage steps. The RMS value of the CMV of the inverter, v_{nO}, is 797 V.

The simulation results of the proposed technique are shown in Fig. 12. Fig. 12(a) illustrates the line-to-line voltage, which

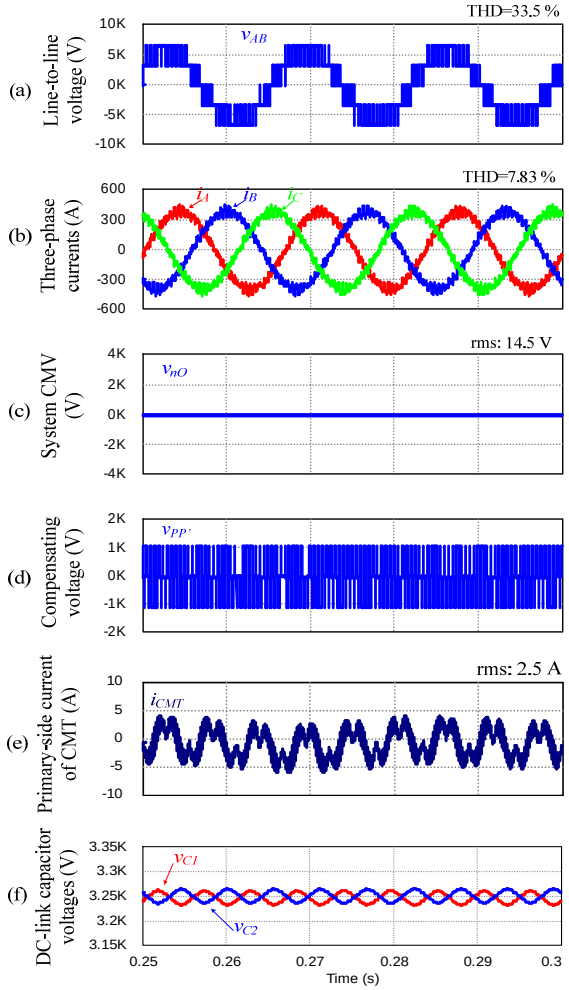

Fig. 12. Output performance of the NPC inverter with the proposed scheme. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of the load. (d) Output of the H-bridge converter. (e) Primary-side current of CMT. (f) DC-link capacitor voltages.

contains five voltage levels. The THD of the voltage is about 33.2%, which is similar to that of the normal seven-segment SVPWM method. The three phase currents are shown in Fig. 12(b); they are sinusoidal and balanced as in Fig. 10(b). The current THD with the auxiliary circuit operation is 3.10%, which is slightly reduced due to the increase in load inductance when the CMT windings are connected in series. The effect of the proposed scheme is shown in Fig. 12(c). The CMV of the NPC inverter is almost eliminated. The RMS value of the CMV for the proposed scheme is 14.5 V, which is about 1.8% and 1.4% compared with that of the modified SVPWM without the auxiliary circuit and the normal seven-segment SVPWM method, respectively. Fig. 12(d) shows the compensatory voltage generated by the H-bridge converter. The primary-side current of the CMT consists of the magnetizing current only as shown in Fig. 12(e), where the peak value is about 1% that of the load currents, which is a design parameter for the CMT. The DC-link capacitor voltages of the NPC inverter, v_{C1} and v_{C2}, are kept balanced.

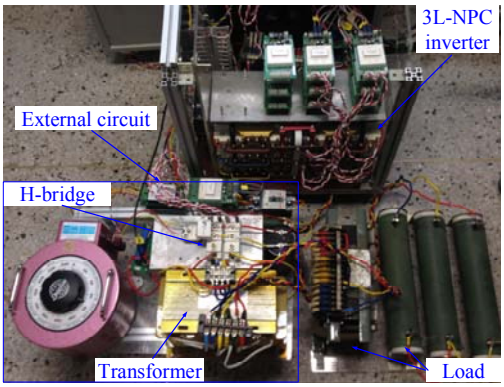

Fig. 13. Experimental setup.

TABLE IV
PARAMETERS OF THE HARDWARE SETUP

Parameters	Values
DC input voltage	200 V
DC-link capacitance	3.3 mF
Switching frequency	5 kHz
Output frequency	60 Hz
Rated output voltage (V_{line} rms)	140 V
Rated output power	4 kW
Resistive load	10 Ω
Inductive load	5 mH
CMT turn ratio	2.444:1:1:1

Their fluctuation is less than 1% of the rated value, as shown in Fig. 12(f).

VI. EXPERIMENTAL RESULTS

The proposed method was tested on a prototype of an NPC inverter system (shown in Fig. 13). The parameters of the hardware setup are listed in Table IV. IGBTs (SKM75GB12T4) were used for the NPC and H-bridge converters. These IGBTs are controlled by a DSP chip (TMS320F28335). The system includes 16 PWM gating signals implemented by a Xilinx FPGA device (XC3S400-PQG208EGQ1321), among which 12 and 4 gating signals are arranged for the NPC and H-bridge converters, respectively. The switching frequency of the inverter is 5 kHz.

Fig. 14 shows the output performance in the unity modulation index with the normal seven-segment SVPWM method. Fig. 14(a) shows the line-to-line voltage of the inverter, where five voltage levels of $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, and V_{dc} exist. Its THD is about 26.7%. The three phase currents of the NPC inverter, which are balanced and sinusoidal, are presented in Fig. 14(b). Fig. 14(c) shows the CMV of the NPC inverter, which includes five voltage levels of −66.7, −33.3, 0, 33.3, and 66.7 V; the RMS value is 26.4 V.

The output performance of the NPC inverter with the modified SVPWM method is also illustrated in Fig. 15. The line-to-line voltage, three phase currents, and system CMV correspond to those in Fig. 14. Fig. 15(a) and (b) show that

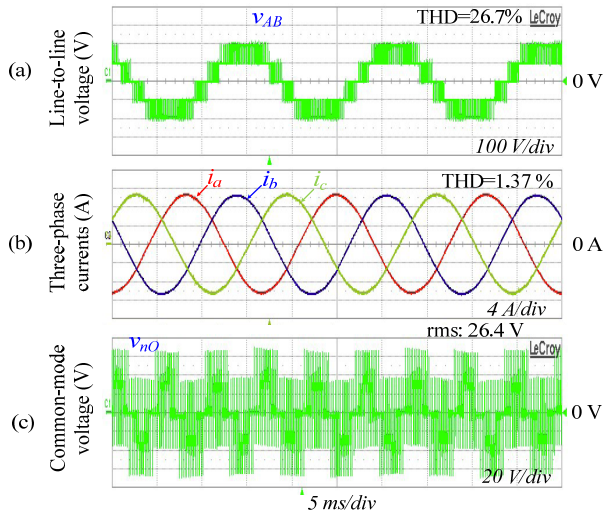

Fig. 14. Output performance of the NPC inverter with the seven-segment SVPWM. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of load.

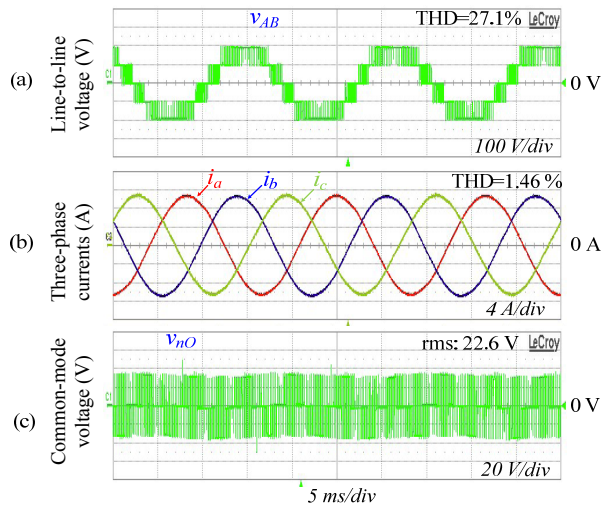

Fig. 15. Output performance of the NPC inverter with the modified SVPWM. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of load.

the THDs of line-to-line voltage and currents are slightly higher than those in Fig. 14(b) and 14(c), respectively, since in the two SVPWM methods, the PWM sampling periods, not the switching frequencies, are similar [22]. However, the CMV of the NPC inverter with modified modulation is 33.3 and 22.6 V in the peak and RMS values, respectively. As shown in Fig. 15(c), the CMV varies only in three voltage levels of −33.3, 0, and 33.3 V.

Fig. 16 shows the performance of the proposed scheme. The line-to-line voltage of the NPC inverter with CMV eliminated is shown in Fig. 16(a), where the THD is similar to that in Fig. 15(a). Fig. 16(b) shows the three phase currents of the NPC inverter, which are balanced and sinusoidal with a THD of 1.48%. Notably, the output performance of the NPC inverter is well maintained with the proposed scheme. Fig. 16(c) shows CMV, where the peak and RMS values are

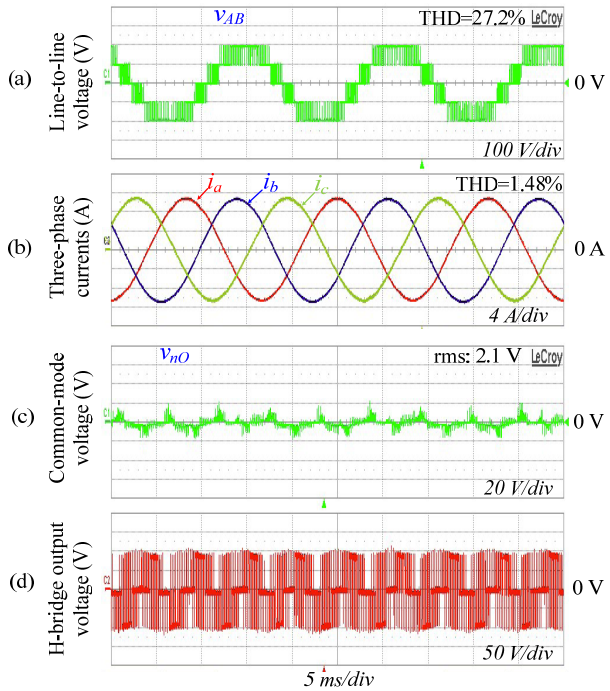

Fig. 16. Output performance of the NPC inverter with the proposed scheme. (a) Line-to-line voltage. (b) Three-phase currents. (c) CMV of load. (d) Output voltage of the H-bridge converter.

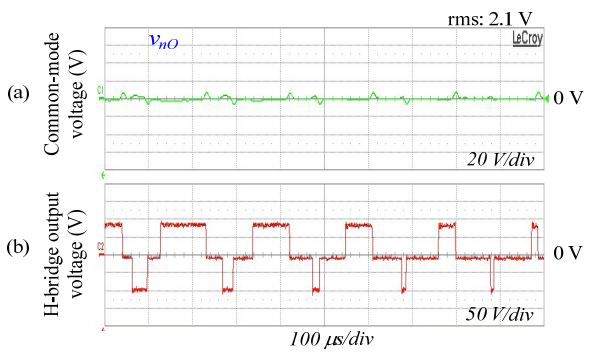

Fig. 17. Magnified waveforms from Fig. 16(c) and (d). (a) CMV. (b) Output voltage of the H-bridge converter.

reduced to 8 and 2.1 V, respectively, compared with those in Fig. 14(c) and Fig. 15(c). However, given the parasitic components in the CMT and the load, the CMV of the NPC inverter is not fully eliminated. The compensatory voltage generated by the H-bridge shown in Fig. 16(d) involves three voltage levels of −33.3, 0, and 33.3 V.

The magnified waveforms of CMV and the compensatory voltage in the proposed method are shown in Fig. 17(a) and (b), respectively. CMV contains small ripples, and the compensatory voltage involves three voltage levels.

VII. Conclusion

A novel method to eliminate CMV in three-level NPC inverters is proposed. This method utilizes not only the modified SVPWM method but also the proposed circuit with the H-bridge converter and CMT. The auxiliary circuit can overcome the power range drawback of existing methods. The simulation and experimental results proved the effectiveness of the proposed method. The RMS value of CMV in the proposed method is only about 8.0% of that in the seven-segment SVPWM method. Furthermore, the maximum modulation index is not reduced with the modified SVPWM.

Acknowledgment

This research was supported by the National Research Foundation of Korea (NRF-2014R1A2A1A11052748).

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Quoc Anh Le was born in Can Tho, Vietnam, in 1988. He received his B.S. degree in electrical engineering from Can Tho University, Can Tho, Vietnam, in 2010. He received his M.S. degree from Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2013. He is presently working to complete his Ph.D. degree in the Department of Electrical Engineering, Yeungnam University, Gyeongbuk, Korea. In 2011, he was an assistant lecturer in the College of Technology, Can Tho University. His current research interests include high-power converters and multi-level converters.

Sangmin Lee was born in 1990. In 2015, he received his B.S. degree in electrical engineering from Yeungnam University, Gyeongsan, Korea, where he is currently working to accomplish his M.S. degree in Power Electronics and Machine Control Laboratory. His research interests include high-power DC–DC converters and energy storage systems.

Dong-Choon Lee received his B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1985, 1987, and 1993, respectively. He was a research engineer in Daewoo Heavy Industry, Korea, from 1987 to 1988. He has been a faculty member in the Department of Electrical Engineering, Yeungnam University, Gyeongsan, Korea, since 1994. As a visiting scholar, he joined the Power Quality Laboratory, Texas A&M University, College Station, TX, USA, in 1998; the Electrical Drive Center, University of Nottingham, Nottingham, UK, in 2001; the Wisconsin Electric Machines and Power Electronic Consortium, University of Wisconsin, Madison, WI, USA, in 2004; and the FREEDM Systems Center, North Carolina State University, Raleigh, NC, USA, from September 2011 to August 2012. His current research interests include AC machine drives, power converter control, wind power generation, and power quality. Professor Lee is currently the Editor-in-Chief for the Journal of Power Electronics of the Korean Institute of Power Electronics.