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Implementation of One-Cycle Control for Switched Capacitor Converters

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Abstract

An extension of the one-cycle control (OCC) method for switched-capacitor (SC) converters is proposed in this paper, featuring a fast dynamic response, wide line and load operation ranges, and simplicity in implementation. To illustrate the operation principle of this nonlinear control method and to demonstrate its simplicity in design, a dual-phase unity gain SC converter is examined. A new control loop based on the charge balance in a flying capacitor is formulated for the OCC technique and implemented with a 15W dual-phase unity gain SC converter on a circuit board for control verification. The obtained experimental results show that external disturbances can be rejected in one switching cycle by the OCC controlled SC converter with good line and load regulations. When compared to other control methods, the proposed nonlinear control loop exhibits superior dynamic performance in suppressing input and load disturbances.

Key words: Nonlinear control, One-cycle control (OCC), Switched-capacitor (SC) converter

I. INTRODUCTION

An ideal DC power supply for mobile electronics such as cellular phones, tablets and internet-of-things (IOT) edge devices, must possess the features of light weight, small form factor, and high power density. A switched-capacitor (SC) converter, comprised of only switches and capacitors, has advantages over inductor based converters in this regard [1]-[3]. Furthermore, a SC converter has the potential for system-on-chip (SOC) implementation, since high quality magnetic components (e.g., inductors and transformers) are not readily available in silicon [4]. However, for practical use, a SC converter must have the capability of rendering a stable output voltage independent of loads and source. It must also exhibit fast external disturbance rejection.

The majority of controller designs in SC converters employ a conventional open-loop control method, pulse-width modulation (PWM), frequency modulation (FM) [5], or current mode control [6]. Among them, conventional open-loop control is widely used owing to its ease of implementation. Alternatively, a proportional-integral-derivative (PID) control design based on a small signal model and a state-space averaging method was proposed and demonstrated in [7]. It can operate effectively under narrow input voltage and load ranges. However, due to the nonlinear characteristics of SC converters with an exponential profile of charging and discharging currents and very short time constant τ, such linear control methods have a limited use. Typically, a nonlinear control method taking these characteristics into consideration can provide better performance for SC converters [8].

Recently, a nonlinear variable structure control (VSC) method was applied to a dual-phase SC converter [8]-[9]. It achieved improvements in the dynamic and steady-state performances of the SC converter. However, this control method requires several switching cycles for the system to reject external disturbances. In order to satisfy the existence and stability conditions of sliding mode (SM) operation, the input voltage and load of a SC converter should be restricted to a limited range [9]. Furthermore, this VSC method is one form of constant frequency SM control implemented in the PWM mode. It is complex and not easy to implement. Another control method that adopted an adaptive mixed-on time and a variable frequency to reduce input current spikes was proposed in [10]. It was used in interleaving SC cells to achieve a seamless charging current from a power source. In a wide operation range, this control method has a high risk of "overlap" or "underlap" interleaving. A phase-shift interleaving control

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for variable-phase SC converters was presented in [11]. By adopting multiple SC converters connected in parallel and the N-state hysteresis unit selection control scheme, it performed voltage conversions with little electromagnetic interference (EMI) over wide operating conditions. However, a very complicate control circuit was required to measure the precise output current for unit selection.

Based on the aforementioned discussion, an alternative simple nonlinear control method with a fast dynamic response speed and a simple topology is worth exploring to extend the current applications of SC converters.

The one-cycle control (OCC) method, which was developed for switching converters [12]-[22], has the ability to control the duty-ratio of switches so that the average diode-voltage is exactly equal to the control reference in each switching cycle. It completely rejects external disturbances and enables the output voltage to rapidly follow the control reference. In addition, the OCC controller is simple, robust, and cost-effective without any current sensor or ramp generator. However, the translation of the OCC technique from a conventional inductor-based converter or inverter to a dual-phase SC converter is not straightforward. This is due to the specific composition of the output voltage, which is provided by two symmetrical SC cells operating in a dual-phase switching manner [9]. In this paper, this method is extended to the application of SC converters based on the charge balance of a flying capacitor for the SC converter model. It exhibits a fast one cycle dynamic response time, a wide operation range, good line and load regulations, and automatic switching error correction.

This paper is organized as follows. In section II, the design and operation principle of the OCC technique for SC converters are presented in combination with a basic step-down dual-phase SC converter as an illustration example. Experimental verification is given in section III. Then some conclusions and discussions follow in section IV.

II. Operational Principle of the OCC Technique

A basic step-down dual-phase SC converter with one capacitor per stage, similar to the circuit topology in [10], [11] and [23], is chosen for illustrative purposes and shown in Fig. 1(a). This allows for the use of a simple SC converter for discussing the theoretical and analytical framework of the OCC control method. Its timing diagram and four operation states are shown in Fig.1(b) and Fig.2, respectively.

Dual-phase SC converters have the symmetrical property. The flying capacitors C_1 and C_2 work complementarily with each other. In the first half cycle (State 1 and State 2), as shown in Fig. 2, C_1 is charged by the input voltage source for the T_{on} time period, while C_2 discharges its storage energy to the load for $0.5T_s$. In the second half cycle (State 3 and State 4), the roles of C_1 and C_2 are interchanged. Each capacitor has a

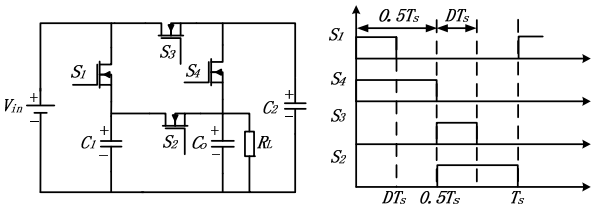


Fig. 1. Basic step-down dual-phase SC converter. (a) Topology of dual-phase SC converter, (b) Timing diagram.

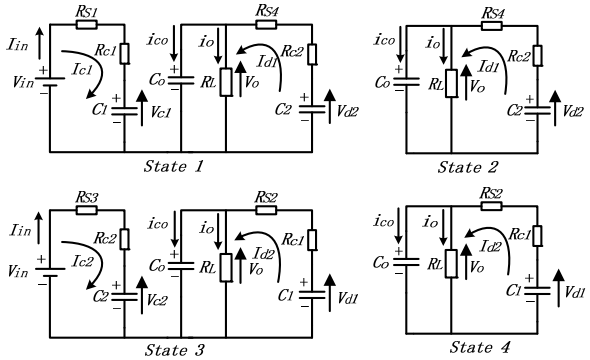


Fig. 2. Four operation states of step-down dual-phase SC converter.

charging period and a discharging period in each switching cycle. In order to facilitate the control model derivation, the following assumptions are made. (1) The capacitors C_1 and C_2 are identical, with the same capacitance and the same equivalent series resistance (ESR). (2) S_1 and S_3 are identical, while S_2 and S_4 are identical with same "on resistance." (3) When S_1 is ON, S_3 must be OFF, and vice versa. When S_2 is ON, S_4 must be OFF, and vice versa.

A. Operation Theory of the OCC Method

Due to the symmetrical topology of this SC converter, a half circuit model is adequate for an analysis of the OCC technique design. It is only necessary to consider the charging and discharging operations of the flying capacitor C_1. Based on the charge balance of the flying capacitor C_1 [24], the increase in the voltage of C_1 during the charging period is equal to the negative voltage drop of C_1 during the discharging period, i.e.:

$$\Delta V_{c1(charging)} = -\Delta V_{c1(discharging)} \quad (1)$$

For State 1 in Fig.2, during the charging period, the instantaneous charging current of the flying capacitors C_1 can be expressed as:

$$I_{c1(t)} = \frac{V_{in}-V_{c1(t)}}{R_{in1}} = C_1 \frac{d_{V_{C1(charging)}}}{dt} \quad (2)$$

Where V_{in} is the input voltage, $V_{c1(t)}$ is the instantaneous voltages of the flying capacitor C_1 during the charging operation, and R_{in1} is equivalent resistance in the charging loop, i.e., $R_{in1} = R_{s1} + R_{c1}$. Here, R_{s1} is the "on resistance" of the switch S_1, and R_{c1} is the ESR of the flying capacitor C_1.

During the charging period, the relationship between the voltage of the flying capacitor C_1 and the input voltage can be derived as:

$$V_{c1max} = V_{in} - (V_{in} - V_{c1min})e^{\frac{-D_1 T_S}{R_{in1}C_1}} \quad (3)$$

For State 3 and State 4 in Fig.2, during the discharging period, the instantaneous discharging current of the flying capacitor C_1 can be obtained with the following equation:

$$I_{d1(t)} = \frac{V_{d1(t)} - V_o}{R_{dis1}} = -C_1 \frac{d_{V_{c1}(discharging)}}{dt} \quad (4)$$

Where $V_{d1(t)}$ is instantaneous voltage of the flying capacitor C_1 during the discharging period, V_o is the output voltage of the SC converter, and R_{dis1} is the equivalent resistance of the discharge loop, i.e., $R_{dis1} = R_{s2} + R_{c1}$. Here, R_{s2} is the "on resistance" of the switch S_2.

The increase in the voltage of the flying capacitor C_1 during the charging period (State 1in Fig.2) can be derived as:

$$\Delta V_{c1(charging)} = \int_0^{d_1 T_S} \frac{V_{in} - V_{c1(t)}}{R_{in1}C_1} dt \quad (5)$$

Where d_1 is the duty-ratio of the switch S_1, and T_s is the time period of one switching cycle.

During the discharging period (State 3 and State 4 in Figure 2), assume that the discharging period is linear since the discharging time period $0.5T_s$ is much smaller than the discharging time constant $\tau_{discharging} = (R_L + R_{c1})C_1$. As a result, the decrease in the voltage of the flying capacitor C_1 can be derived as:

$$\Delta V_{c1(discharging)} = -\frac{\overline{V_{d1(t)}} - V_o}{R_{c1}C_1} 0.5T_s \quad (6)$$

Where $\overline{V_{d1(t)}}$ is the average voltage of the flying capacitor C_1 during the discharging period.

Considering the charge balance of the flying capacitor C_1 and the complementarily operation of the flying capacitors C_1 and C_2, the following equation can be derived as:

$$C_1(V_{c1max} - V_{c1min}) = 0.5\, I_o T_s \quad (7)$$

Based on the voltage-gap modeling method for the single stage SC converter in [25], the voltage gap between the minimum voltage V_{c1min} of the flying capacitor C_1 in the discharging period and the load voltage V_o can be expressed as:

$$V_{c1min} - V_o = (V_{c1max} - V_o)e^{\frac{-0.5T_S}{R_{dis1}C_1}} \quad (8)$$

Substituting (3) and (7) into (8), the voltage conversion ratio of the SC converter can be derived by the following equation:

$$\frac{V_o}{V_{in}} = \frac{2R_L C_1(1-e^{-\alpha})(1-e^{-\beta})}{2R_L C_1(1-e^{-\alpha})(1-e^{-\beta}) + T_S[(1-e^{\alpha})e^{-\beta} + (1-e^{-\beta})]} \quad (9)$$

Here, $\alpha = \frac{D_1 T_S}{R_{in1}C_1}$ and $\beta = \frac{0.5T_S}{R_{dis1}C_1}$.

The voltage conversion ratio of equation (9) is plotted in a three-dimensional (3D) plot as a function of the frequency and the duty-cycle as shown in Fig.3. The parameters of the SC converter are set as in Table I. As shown in Fig.3, with a wide range of frequency, the duty-ratio regulation capability is prominent. In addition, the output voltage gain ratio is adjusted rapidly in a small duty-ratio scope. Therefore, the "overlap" interleaving of the dual-phase SC converter is prevented with the charge balance modeling method in a wide operation range.

Substituting (5) and (6) into (1), the charge balance of the flying capacitor C_1 in one switching cycle can then be

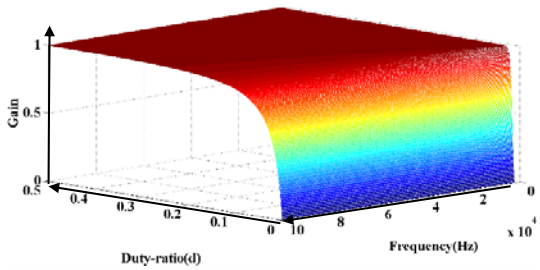


Fig. 3. Voltage gain ratio as function of frequency and duty-cycle at load resistance 5Ω .

TABLE I
PARAMETERS OF SC CONVERTER

Parameter	Value
R_L	5Ω
C_1	47uF
R_{in1}	0.19Ω
R_{dis1}	0.06Ω
d	0-0.5
f	100Hz-100KHz

expressed as:

$$\frac{2}{T_S}\int_0^{d_1 T_S} \frac{V_{in} - V_{c1(t)}}{R_{in1}C_1} dt = \frac{\overline{V_{d1(t)}} - V_o}{R_{c1}C_1} \quad (10)$$

Letting $K_1 = \frac{2}{T_S R_{in1} C_1}$ and $K_2 = \frac{1}{R_{C1}C_1}$, equation (10) can be rearranged as:

$$K_1 \int_0^{d_1 T_S} (V_{in} - V_{c1(t)})dt = K_2(\overline{V_{d1(t)}} - V_o) \quad (11)$$

In order to obtain the charge balance equation for the flying capacitor C_2, the following definitions are made. (a) $\overline{V_{d2(t)}}$ is the average voltage of the flying capacitor C_2 during the discharging period (State 1 and State 2 in Fig.2). (b) $V_{c2(t)}$ is the instantaneous voltage of the flying capacitor C_2 during the charging period (State 3 in Fig.2). (c) R_{c2} is the ESR of the flying capacitor C_2, R_{s3} is the "on resistance" of the switch S_3, and R_{in2} is the equivalent resistance in the charging loop (State 3 in Fig.2), i.e., $R_{in2} = R_{s3} + R_{c2}$. (d) d_3 is the duty-ratio of the switch S_3 ($d_1 = d_3$). Using the same principle and letting $K_3 = \frac{2}{T_S R_{in2} C_2}$ and $K_4 = \frac{1}{R_{c2}C_2}$, the charge balance of the flying capacitor C_2 in one switching cycle can be derived as:

$$K_3 \int_0^{d_3 T_S} (V_{in} - V_{c2(t)})\, dt = K_4(\overline{V_{d2(t)}} - V_o) \quad (12)$$

The discharging period of the flying capacitor C_1 can be divided into two stages (Stage I and Stage II) as shown in Fig.4. During Stage I, the flying capacitor C_1 discharges its storage energy to the filter capacitor C_o. This period is very short and has a very little effect on the output voltage. Therefore, it can be ignored. For Stage II, the flying capacitor C_1 and the filter capacitor C_o concurrently deliver their storage energy to the load resistor R_L. The relationship between the load current and the instantaneous discharging currents of the capacitors C_1 and C_o can be written as:

$$i_o = i_{d1} + i_{co} \quad (13)$$

During the discharging period of Stage II, the change in the

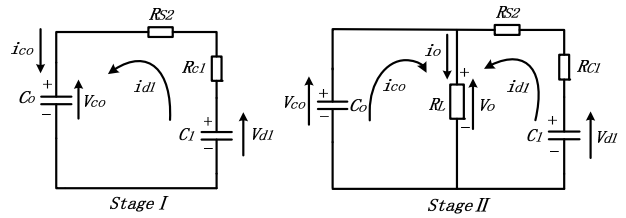


Fig. 4. Two Stages of flying capacitor C_1 during the discharging period.

voltage of the flying capacitor C_1 is equal to the change in voltage of the parallel connected capacitors C_1 and C_o, the following equation can be derived as:

$$\frac{\Delta Q1}{C_1} = \frac{\Delta Q2}{C_1+C_o} = \frac{i_{d1}\Delta t}{C_1} = \frac{(i_{d1}+i_{co})\Delta t}{C_1+C_o} \quad (14)$$

Where $\Delta Q1$ is the stored charge change of the flying capacitor C_1. $\Delta Q2$ is the stored charge change of the parallel connected capacitors C_1 and C_o. Δt is the time period of Stage II in Fig.4.

According to equations (13) and (14), the difference in average voltage of the flying capacitor C_1 during the discharging period Stage II and output voltage V_o can be expressed as:

$$\begin{aligned}\Delta V_{dif} &= \overline{V_{d1(t)}} - V_o = i_{d1} \times (R_{C1} + R_{s2}) \\ &= \frac{C_1}{C_1+C_0} \times \frac{V_o}{R_L} \times (R_{c1} + R_{s2})\end{aligned} \quad (15)$$

Where R_{s2} is the "on resistance" of the switch S_2.

Examining equation (15) with the assumption that the output voltage (V_o) and the load resistance (R_L) are constant, it can be observed that the difference voltage ΔV_{dif} is kept constant. This implies that the average voltage of the flying capacitor C_1 ($\overline{V_{d1(t)}}$) during the discharging period has a linear relationship with the output voltage (V_o). If the average voltages ($\overline{V_{d1(t)}}$ and $\overline{V_{d2(t)}}$) of the flying capacitors C_1 and C_2 during the discharging period are replaced by the reference voltage v_{ref}, the output voltage V_o of the SC converter can be controlled linearly to the target voltage v_{ref}. This can be expressed as:

$$V_o = v_{ref} - \Delta V_{dif} \quad (16)$$

Replacing the average voltage of the flying capacitor C_1 ($\overline{V_{d1(t)}}$) and the average voltage of the flying capacitor C_2 ($\overline{V_{d2(t)}}$) during the discharging period by v_{ref}, the charge balance equations (11) and (12) can be respectively rewritten as:

$$K_1 \int_0^{d_1 T_s} (V_{in} - V_{c1(t)})\, dt = K_2 (v_{ref} - V_o) \quad (17)$$

$$K_3 \int_0^{d_3 T_s} (V_{in} - V_{c2(t)})\, dt = K_4 (v_{ref} - V_o) \quad (18)$$

It is worth mentioning that equations (17) and (18) are the key control equations for the OCC method.

The two integrations (V_{int1} and V_{int2}) of the difference between the input voltage V_{in} and the voltage of the flying capacitor C_1 ($V_{c1(t)}$) and that of the flying capacitor C_2 ($V_{c2(t)}$) are expressed in the left hand side of equations (17) and (18), respectively. The control decreased voltage signal V_e of the flying capacitor C_1 or C_2 is obtained from the right hand side of the equations, i.e.:

$$V_e = K_2(v_{ref} - V_o) = K_4(v_{ref} - V_o) \quad (19)$$

A dual-phase SC converter can be properly controlled by the OCC technique with the key control equations (17) and (18). The control signals for the switches S_1 and S_3, i.e., U_{s1} and U_{s3}, are determined by equations (17) and (18), respectively. As illustrated in the key control equations, the control decreased voltage signal (V_e) is equal to the integration (V_{int1} or V_{int2}) in each of the switching cycles. The duty-ratios $d_1(U_{s1})$ and d_3 (U_{s3}) of the current switching cycle are independent of the history states of the previous switching cycles. The transient disturbance of the integration or the control decreased voltage signal can be completed within one switching cycle. The control signals determined by (17) and (18) are nonlinear functions of the input voltage, the voltage of the flying capacitor, the output voltage and the control reference. With an aid of the OCC nonlinear control, the output voltage of the SC converter is transformed to be linearly dependent on the control reference voltage v_{ref}.

B. OCC Controller for Dual-Phase SC Converters

Stable operation of dual-phase SC converters can be implemented by the OCC controller as shown in Fig.5(a). The operation waveforms for this configuration are depicted in Fig.5(b). This control system is comprised of two resettable integrators, two comparators, two nor-gate level triggered SR flip-flops and some other passive components. It is simple and easy for implementation.

The resettable integrator of the OCC controller in this paper is constructed by a RC circuit and a reset switch as shown in Fig.6. For the RC circuit, the integration function can be achieved when the following requirements are satisfied:

(a) The time constant $\tau = RC$ should be much larger, when compared to the time period of the input signal.
(b) The resistance of R should be higher (minimum 10 times) than the capacitive reactance r_{ch}.

Based on the above assumptions, the integration relationship between the input signal and the output signal can be derived as the following equation:

$$V_o = \frac{1}{RC} \int_0^t V_{in} dt \quad (20)$$

The integration time is determined by the control signal of the reset switch W as shown in Fig.6. The slope of the integration is proportional to the value of the input signal V_i.

clock 1 signal in Fig.5(a) set Flip-Flop 1 ($Q = 1$ and $\bar{Q} = 0$) to turn on the switch S_1 of the dual-phase SC converter (in Fig.1(a)) and to turn off the reset switch W_1 of the resettable integrator (in Fig.5(a)). The reset switch W_1 will be kept OFF for the $t_{w1off} = d'T_s$ time period. When the flying capacitor C_1 starts charging, the difference between the input voltage and the voltage of the flying capacitor C_1 $[V_{in} - V_{c1(t)}]$ is integrated

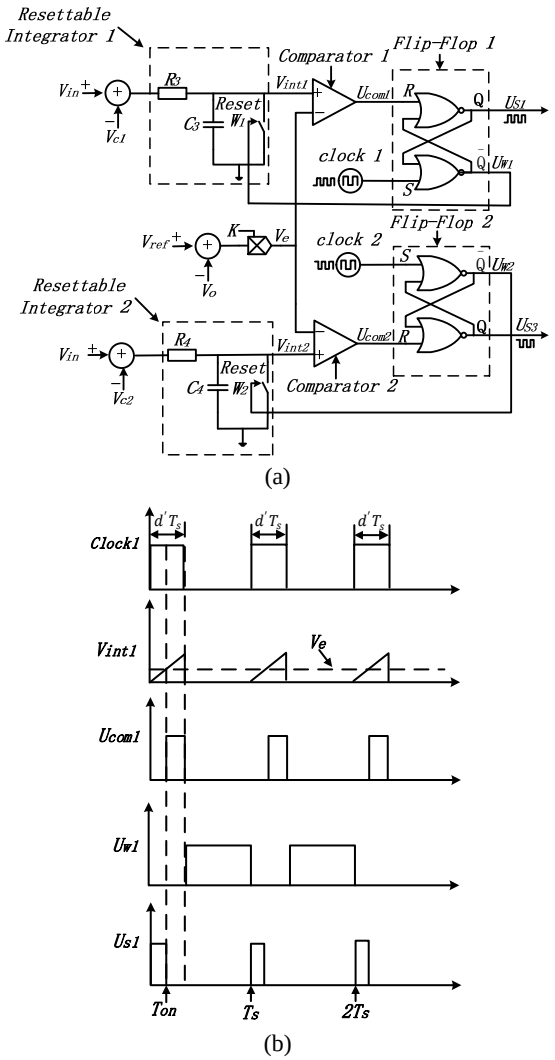


Fig. 5. OCC controller for dual-phase SC converter (a)Logic circuit (b)Operation waveforms of OCC controller.

by the resettable integrator and is continuously compared with the control decreased voltage signal V_e [$V_e = K_1(V_{ref} - V_o)$]. When the integration V_{int1} [$K_1 \int_0^{d_1 T_s}(V_{in} - V_{c1(t)})dt$] reaches the control decreased voltage signal V_e, the comparator changes its state (from 0 to 1) and Flip-Flop 1 is set the second state ($Q = 0$ and $\bar{Q} = 0$). At this point in time, the switch S_1 of the dual-phase SC converter is tuned off, and the reset switch W_1 is kept in the OFF state. Then the $d'T_s$ high state of the clock signal is over. Flip-Flop 1 sets the third state ($Q = 0$ and $\bar{Q} = 1$). The reset switch W_1 is turned on and the integration will be set to zero. The resettable integrator is then ready for the next switching cycle. When the next clock 1 signal arrives, the resettable integrator is turned on again.

As shown in Fig. 5(b), the clock 1 signal with the duty-ratio d' turns on the resettable integrator 1 for the $d'T_s$ time period. Meanwhile, the switch S_1 will be turned on by the control signal U_{s1}. When the integration V_{int1} reaches the control decreased voltage signal V_e, the output of comparator 1 in

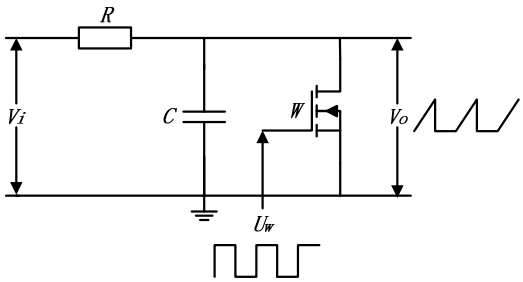


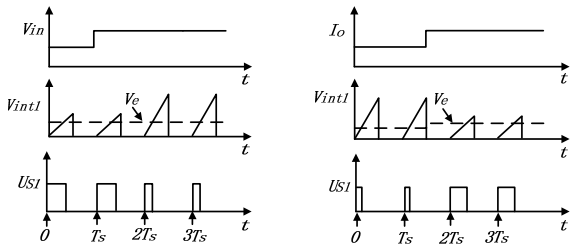
Fig. 6. Resettable RC integrator with reset switch W.

Fig.5(a) changes from low to high. Then the switch S_1 is turned off immediately. Therefore, in one switching cycle, the control signal U_{s1} for the switch S_1 in Fig.1(a) will be generated with the duty-ratio $d_1 = T_{on}/T_s$ (T_s is one cycle time period of the signal clock 1, which is equal to the one cycle time period of U_{s1}). The duty-ratio of U_{s1} (d_1) is set to less than the duty-ratio of the clock 1 signal (d'). The reset switch W_1 is turned on and the resettable integrator is turned off when the high state of the clock 1 signal is over, at the time point $d'T_s$. After $(1 - d')T_s$, the operation cycle repeats as the next clock 1 signal shows up.

In Fig.5(a), the generation of the control signal U_{s3} is similar to that of U_{s1}. They share the same duty-cycle yet with a 180^0 phase shift, due to the 180^0 phase shift clock signals (clock 1 and clock 2). The control signals for the switches S_2 (U_{s2}) and S_4 (U_{s4}) are 50% duty-cycle pulses complementary to each other. The control signals U_{s2} and U_{s4} are generated by two different square signal generators and no regulations are required.

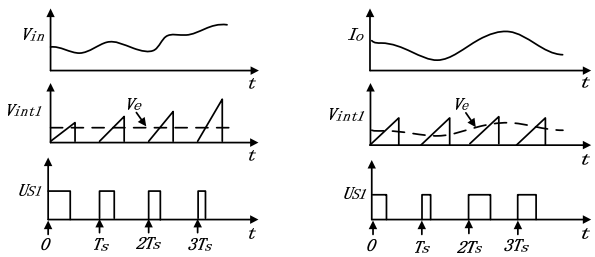
To explain the operation of the SC converter with the OCC method for rejecting the dynamical linear input voltage or load disturbance, the operation waveforms are illustrated in Fig.7. As shown in Fig.7(a), it is assumed that the input voltage changes with a step-up function and that the load and reference voltage are kept constant. As a result, the control decreased voltage signal V_e remains constant. Since the slope of the integration V_{int1} is directly proportional to [$V_{in} - V_{c1(t)}$], the slope becomes steeper than before, when a higher input voltage appears. As a result, the OCC controller takes less time to reach the control decreased voltage signal V_e, and requires a smaller duty-ratio of U_{s1} than the previous switching cycle. On the other hand, when the input voltage is lowering, a larger duty-ratio of U_{s1} is observed.

In Fig.7(b), it is assumed that the load current changes with a step-up function and that the input voltage and reference voltage are kept constant. Since the slope of the integration V_{int1} remains constant, the output voltage declines and the control decreased voltage signal V_e immediately follows to reach a higher value. As a result, the OCC controller will take more time for the integration V_{int1} to reach the control decreased voltage signal V_e, requiring a larger duty-ratio of U_{s1}. However, when the load current is lowering, a smaller duty-ratio of U_{s1} can be observed.



(a) (b)

Fig. 7. Operation waveforms of OCC controller for SC converter with dynamical linear external disturbance (a) Input voltage step-up, (b) Load current step-up.



(a) (b)

Fig. 8. Operation waveforms of OCC controller for SC converter with dynamical nonlinear external disturbance (a) Input voltage disturbance, (b) Load current disturbance.

On the other hand, as shown in Fig.8, the dynamic nonlinear external disturbance (such as a sinusoidal signal) is injected into the power source and load current. In Fig.8(a), it is supposed that the load and reference voltage are constant. In addition, with the dynamic nonlinear input signal, the slope of the integration V_{int1} changes immediately and instantaneously to follow the trend of the input voltage in one switching cycle.

In Fig.8(b), it is supposed that the input voltage and reference voltage are constant. In addition, with the dynamical nonlinear load current, the value of the control decreased voltage signal V_e instantaneously follows the trend of the load current in one switching cycle. As a result, the nonlinear external disturbance can be rejected by instantaneously adjusting the duty-ratio of the PWM control signal U_{s1}.

With the OCC method, the dynamic response time to reject an external disturbance in the input voltage or load is one switching cycle.

C. Comparison with Other Control Methods

Thanks to the resettable integrator and the level triggered SR flip-flop, the memory states of the OCC controller are cleared in each switching cycle. Whenever an external disturbance occurs in the input voltage or in the load current, it is instantaneously mirrored by the key control equations (17) and (18). There is no steady-state error or dynamic error between the integration and the control decreased voltage signal. In comparison, the PI and SM control methods for SC converters adopt the same structure as the conventional PWM voltage-mode controller. In the SM control method, as shown in [9], an additional current sensor is required for constructing the control signal and two sets of auxiliary circuits are required for generating the ramp signals. The historical states in both of the control methods need to consider and be compared with the new control signal to adjust the duty-cycle to handle external disturbances. As a result, the dynamic response time is longer than the OCC method. A detailed comparison with other control methods is shown in Table II.

III. EXPERIMENT VERIFICATION

Derived from the key equations (17) and (18), an OCC circuit is developed for a 15W(5V,3A) dual-phase SC converter. The experiments were conducted to evaluate dynamic response to external disturbances in the power source or load current of a SC converter with the OCC method. The operating conditions of the SC converter are $V_{in} = 7V - 15V, f = 25KHz$ and $100KHz$, flying capacitors $C_1 = C_2 = 47uF (R_{ch1} = R_{ch2} = 0.03\Omega)$ and filter resistor $C_o = 100uF$. Based on the minimum switching frequency $f = 25KHz$, a resistor with a resistance of $R = 200\Omega$ ($R \gg R_{ch1} = R_{ch2}$), and a capacitor with a capacitance of $C = 1uF$ of the RC integrator were selected. The RC time constant ($200uS$) is 10 times longer than the half switching time period ($20uS$) at a minimum switching frequency of $f = 25KHz$. This satisfies the two requirements for the operation of the RC integrator. The duty-ratio of the clock signal is 0.5. Therefore, the constant integration time period of the integrator is $0.5T_s$.

A. Dynamic Performance Evaluation

Fig.9 depicts the waveforms of the input voltage V_{in}, the output voltage V_o, the load current I_o, the integration V_{int} (a, b, c, d, e and f) and the control PWM signal (U_{s1}) for the switch S_1 (h and i). In order to show the whole period of the power source disturbance, the switching frequency was selected at 25KHz. Fig.9(a), (b) and (c) show the operation waveforms of the OCC controlled SC converter under the no load condition ($I_o = 0A$). The slope of the integration V_{int} was kept constant with the constant power source in Fig.9(a). Meanwhile, it was in proportion to the step-down function (13-9V) power source signal in Fig.9(b) and the ramp-up (7-11V) function power source signal in Fig.9(c). The output voltage V_o had a good regulation with or without disturbances in the power source signal. Therefore, this nonlinear control method for SC converters was verified under the no load condition. In Fig.9(d) and (e), the load current and reference voltage were held constant. As a result, the control decreased voltage signal V_e was constant. A step-down function (13-9V) in Fig.9(d) and a ramp-up function (7-11V) in Fig.9(e) were injected into the power source, at a load current of 1A and a switching frequency of $25KHz$. Note that the spikes on the power source voltage were caused by the non-zero impendence of the power

TABLE II
COMPARISON OF DIFFERENT CONTROL METHODS FOR SC CONVERTER

Description	Open-Loop Control	PI Control in [9]	VSC in [9]	OCC
Control Type	Linear	Linear	Nonlinear	Nonlinear
Control Topology	Simple	Simple	Complex	Simple
Response Time		Several cycles	Several cycles	One cycle
Operation Range	Large	Narrow	Middle	Large
Load Voltage Ripple	Large	Large	Small	Small
Operation Condition	No limited	No limited	Limited	No Limited
Input Range		12-15V	12-15V	7-15V
Regulation Property*		0.8%(V_o)	0.6%(V_o)	0.5%(V_o)

Regulation Property*:Output voltage V_o deviation from reference voltage V_{ref}(5V).

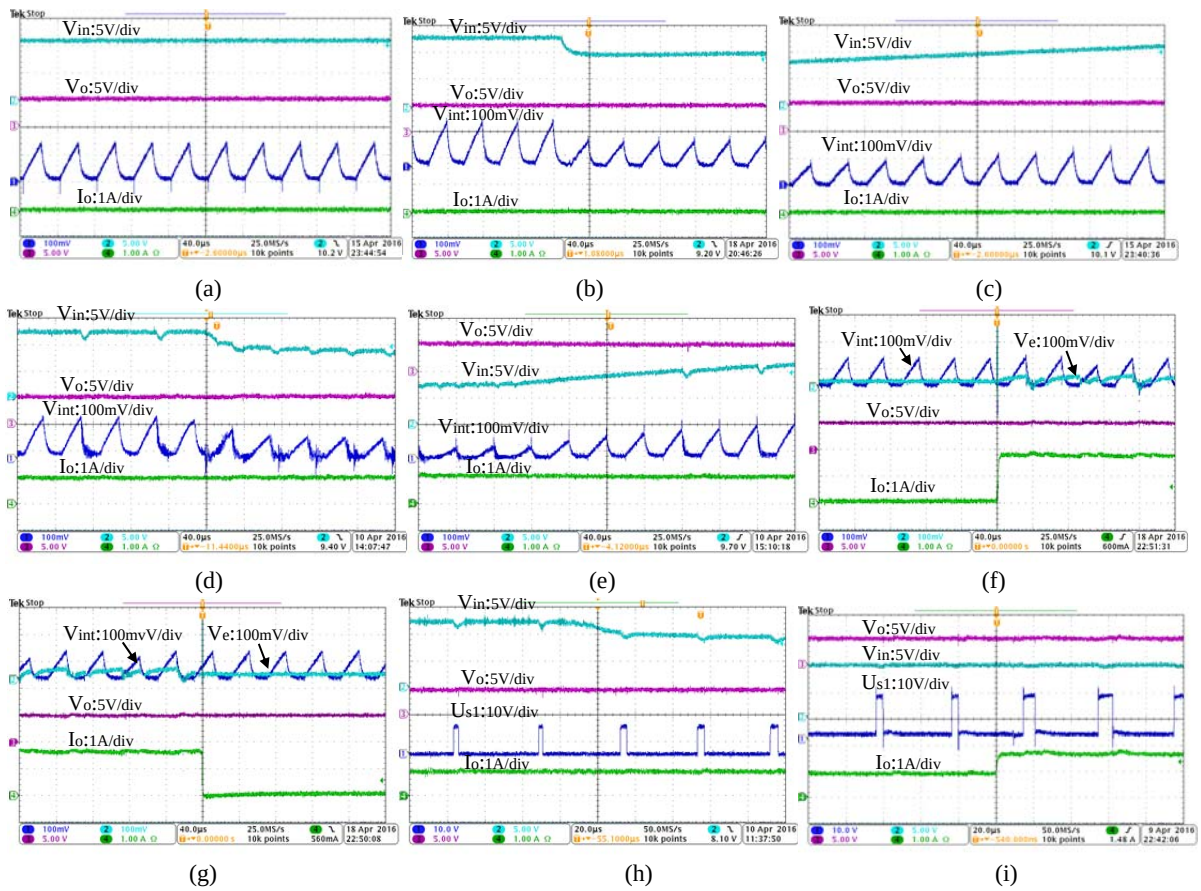


Fig. 9. Operation waveforms of input voltage, load current, output voltage, integration (a-g) and the control signal U_{S1}(h and i) of the OCC controlled SC converter with the external disturbance measured at switching frequency 25KHz. (a)10V constant input voltage in no load condition. (b) input voltage step-down(13-9V) in no load condition. (c) input voltage ramp-up(7-11V) in no load condition. (d) input voltage step-down(13-9V) at load current 1A (e) input voltage ramp-up(7-11V) at load current 1A (f)load current step-up(1.0-1.9A) at input voltage 10V. (g)load current step-down(1.9-1.0A) at input voltage 10V. (h) input voltage step-down(13-9V) at the load current 1A(i)load current step-up(1-1.9A) at input voltage 10V.

source. These spikes did not influence the average value of the difference between the input voltage and the voltage of the flying capacitor. They were included in the integration V_{int} which was compared with the control decreased voltage signal V_e. It can be seen from Fig.9(d) and (e), that the slope of the integration V_{int} was kept proportional to the input voltage V_{in}, and that it was changed instantaneously. As a result, the duty-ratio was adjusted in one switching cycle. Fig.9(h) shows the related duty-ratio adjustment to reject the power source step-down (13-9V) function perturbation. In Fig.9(f) and (g), the power source and reference voltage were held constant. Therefore, the slope of the integration V_{int} was kept constant.

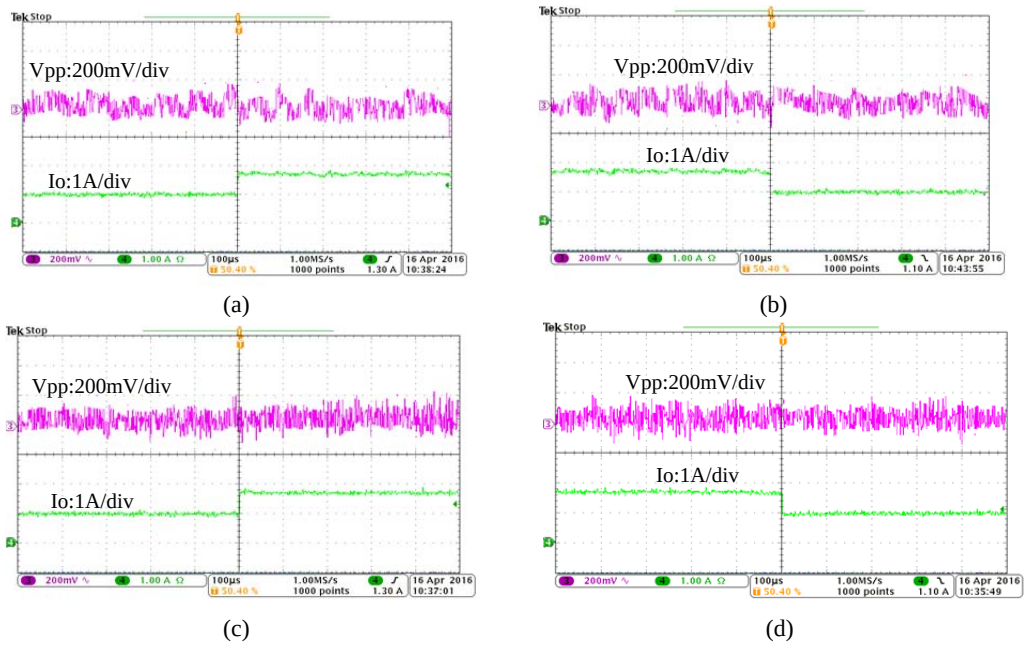


Fig. 10. Operation waveforms of the output voltage ripple v_{pp} and load current I_o of OCC controlled SC converter operating at the input voltage 10V measured at switching frequency 25KHz (a and b) and 100KHz (c and d). (a) Load current step-up (1.0-1.9A). (b) Load current step-down (1.9-1.0A). (c) Load current step-up(1.0-1.9A). (d) Load current step-down(1.9-1.0A).

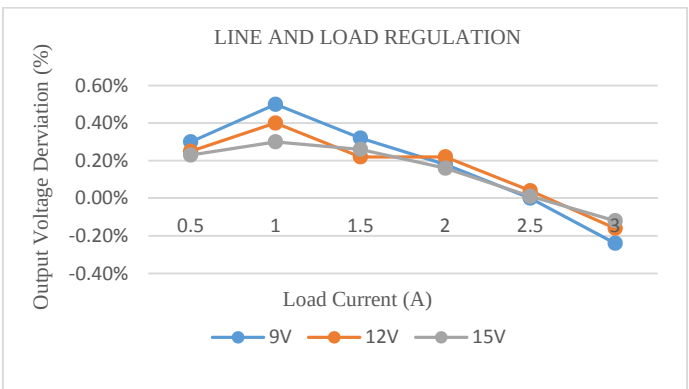


Fig. 11.Steady-state dc output voltage deviation v_d in percentage from control reference voltage versus load currents of SC converter measured at input voltage V_{in} 9V,12V and 15V.

A step-up function (0-1.9A) shown in Fig.9(f) and a step-down function (1.9-0A) shown in Fig.9(g) were injected into the load current, at an input voltage of 10V and a switching frequency of $25KHz$ .As shown in Fig.9(f) and (g), with the load disturbance, the slope of the integration V_{int} was kept constant. The load current directly and instantly affected the load voltage. The control decreased voltage signal V_e has a linear relationship with the load voltage [$V_e = K_2(v_{ref} - V_o) = K_4(v_{ref} - V_o)$]. With the variable load current, the control decreased voltage signal V_e was changed instantaneously. Therefore, the duty-ratio was adjusted in one switching cycle. Fig.9(i) shows the related duty-ratio adjustment to reject the load current step-up function (1-1.9A) disturbance. The experiment results are in good agreement with the theory analysis and the principle of the OCC technique.

Fig.10 shows the output voltage ripple and load current of the SC converter operating at an input voltage of 10V and at switching frequencies of $f_1 = 25KHz$ (a and b) and $f_2 = 100KHz$ (c and d). The load current alternated between 1.0 A and 1.9A. Thanks to the fast OCC response speed and memory states insensitivity, as evident from the results, the output voltage was kept stable with a small voltage ripple during transient responses.

B. Steady-state Regulation

Fig.11 illustrates the output voltage V_o deviation from the reference voltage V_{ref} as a function of the load currents when measured at input voltages of 9V, 12V and 15V and a switching frequency of $100KHz$. In the input voltage range, the largest output voltage deviation from the reference voltage V_{ref} was a 0.5% error (0.025V) when the input voltage is

decreased to 9V. On the other hand, when it comes to the load current range, the largest output voltage deviation from the reference voltage V_{ref} was a 0.5% error (0.025V) when the load current was measured at 1A. These results confirm that the OCC controlled SC converter has good line and load regulation under wide input voltage and load current ranges.

IV. Conclusions and Discussions

This paper presents an extension of the OCC method for dual-phase SC converters. The method for modeling the dual-phase SC converter using the charge balance principle is illustrated. Experiments results demonstrate that with this control method, external disturbances in the input voltage and load current of a SC converter can be one cycle controlled in a wide operation range. Moreover, good line and load regulation of SC converters is also verified. The concept of the OCC method is more straightforward due to its simple logic control circuit, when compared to other nonlinear control methods. The OCC method is generally applicable to other types of SC converters, which broadens the application usage of SC converters. With the development of the SC circuit design and OCC technique, OCC controlled SC converters can be a promising candidate for future integrated DC-DC converters.

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