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A Wide Input Range, 95.4% Power Efficiency DC-DC Buck Converter with a Phase-Locked Loop in 0.18 μm BCD

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Abstract

This paper presents a DC-DC buck converter with a Phase-Locked Loop (PLL) that can compensates for power efficiency degradation over a wide input range. Its switching frequency is kept at 2 MHz and the delay difference between the High side driver and the Low side driver can be minimized with respect to Process, Voltage and Temperature (PVT) variations by adopting the PLL. The operation mode of the proposed DC-DC buck converter is automatically changed to Pulse Width Modulation (PWM) or PWM frequency modes according to the load condition (heavy load or light load) while supporting a maximum load current of up to 1.2 A. The PWM frequency mode is used to extend the CCM region under the light load condition for the PWM operation. As a result, high efficiency can be achieved under the light load condition by the PWM frequency mode and the delay compensation with the PLL. The proposed DC-DC buck converter is fabricated with a 0.18 μm BCD process, and the die area is 3.96 mm^2. It is implemented to have over a 90 % efficiency at an output voltage of 5 V when the input range is between 8 V and 20 V. As a result, the variation in the power efficiency is less than 1 % and the maximum efficiency of the proposed DC-DC buck converter with the PLL is 95.4 %.

Key words: DC-DC buck converter, Frequency mode control, High efficiency, PLL, PWM, Wide input range

I. INTRODUCTION

In recent years, portable products have been trending towards reductions in size and weight, and they incorporate power management systems for efficient operation. The use of DC-DC buck converters has increased in various fields since advanced technology is being applied to a wider range of applications. As a result, high-efficiency DC-DC buck converters with a wide input voltage range and a wide load current range are needed [1], [2].

However, the power efficiency can be varied by switching frequency variations and delay mismatches between the High side driver and the Low side driver due to PVT variations.

In this paper, a DC-DC buck converter with a Phase-Locked Loop (PLL) has been proposed to overcome power efficiency degradation over a wide input voltage range and a wide load current. The proposed DC-DC buck converter with a PLL operates either in the PWM or the PWM frequency mode according to the given load conditions. The proposed PLL generates a constant switching frequency which is robust to PVT variations [1]. In addition, the delay mismatch issue between the High side driver and the Low side driver according to PVT variations is automatically compensated by the PLL.

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II. ARCHITECTURE OF THE DC-DC BUCK CONVERTER WITH A PLL

A. The DC-DC Buck Converter

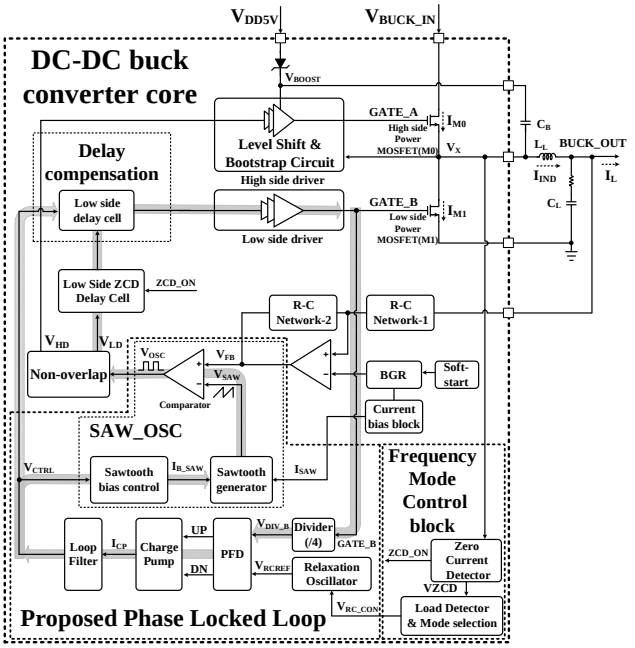


Fig. 1. The block diagram of the proposed DC-DC buck converter with the PLL.

Fig. 1 shows a block diagram of the proposed DC-DC buck converter using a PLL. The proposed DC-DC buck converter consists of a PLL, a Band-Gap Reference (BGR), an error amplifier, a frequency mode control block, High / Low side drivers, a non-overlap and a delay compensation block.

The PLL of the proposed DC-DC buck converter generates a constant switching frequency and a constant delay regardless of the effect of the external environment and PVT variations. It is designed to automatically select the PWM or the PWM frequency mode by sensing the V_X node from the frequency mode control block according to heavy load or light load current conditions. Therefore, the proposed DC-DC buck converter operates under PWM from 300 mA to 1.2A and enters into the PWM frequency mode under 300 mA.

The input voltage, $V_{BUCK\_IN,}$ is from 8 V to 20 V. In order to use all of the voltage ranges, the V_{GS} voltage of the High side Power MOSFET (M0) should be constant, depending on the process. The GATE_A voltage guarantees the constancy of the V_{GS} voltage of the High side Power MOSFET (M0) when the MOSFET is operating in the saturation region. As for the High side driver, a level shifter is used to generate a higher voltage level. The V_{BOOST} voltage that is generated by the V_X node voltage and the Zener diode from the bootstrap circuit guarantees that the V_{GS} voltage of the High side Power MOSFET (M0) can operate in the saturation region.

The operation of the Low side driver is different depending on whether there is a heavy load or a light load. Under a heavy load, the duty is determined by the load current, and it controls the Power MOSFET. Under a light load, the reverse current is generated at the V_X node. The reverse current that is generated is sensed by the Zero Current Detector (ZCD), and during the on-duty state of the Low side driver, GATE_B turns on and off to prevent a reverse current.

B. Phase-Locked Loop

A general DC-DC buck converter has a switching frequency variation and a delay mismatch issue due to the external environment or PVT variations. These problems cause an overall reduction in the efficiency, and can result in a malfunction of the DC-DC buck converter [3].

The total loss can be described as a summation of the switching loss, conduction loss, dead-time loss, diode reverse recovery loss, and other losses of the DC-DC buck converter as shown in Eq. (1) [4], [5].

$$P_{Total\_Loss} = P_{SW} + P_{Cond} + P_{Other} \quad (1)$$

where, P_{Total_Loss}, P_{SW}, P_{Cond}, and P_{Other} are the DC-DC buck converter total loss, switching loss, conduction loss, and other losses (dead-time loss, diode reverse recovery loss, gate driver loss, and etc.), respectively [4], [5].

If the switching frequency or delay is changed, the switching loss will be increased as described in Eq. (2). When the conduction loss is increased, the efficiency is reduced by Eq. (3) [4], [5].

$$P_{SW} = \frac{V_{DS} \times I_{DS}}{2} \times (T_{RISE} + T_{FALL}) \times f_S \quad (2)$$

$$P_{Cond} = \begin{pmatrix} (I_{rms,HS}^2 \times D \times R_{HS}) \\ +(I_{rms,LS}^2 \times (1 - D) \times R_{LS}) \end{pmatrix} \quad (3)$$

where, V_{DS}, I_{DS}, T_{RISE}, T_{FALL}, $f_{S,}$ $I_{rms,HS}$, $I_{rms,LS}$, R_{HS}, R_{LS}, and D are the source-drain voltage, source-drain current, switching rising time, switching falling time, switching frequency, $\sqrt{I_{rms,HS}^2 + \frac{\Delta I_L^2}{3}}$, $\sqrt{I_{rms,LS}^2 + \frac{\Delta I_L^2}{3}}$, the High side Power MOSFET resistance, the Low side Power MOSFET resistance, and the duty cycle of the switching clock, respectively [4-5]. Therefore, variations of the switching frequency and delay mismatch in the conduction loss, switching loss, dead-time loss, diode reverse recovery loss, and other losses are increased and the efficiency of the DC-DC buck converter is reduced.

Fig. 2 shows a block diagram of the proposed PLL. It consists of a relaxation oscillator, Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), SAW_OSC circuit, and Divider (/4). The SAW_OSC circuit is composed of a comparator, Sawtooth bias control, and Sawtooth generator. The SAW_OSC circuit operates as the Voltage Controlled Oscillator (VCO) of a conventional PLL.

To control the duty cycle of V_{OSC} in the PWM operation, the SAW_OSC needs a Sawtooth generator that is different from the ring oscillator. The duty of the PWM is determined using comparator to compare V_{FB} with V_{SAW} to make the output of V_{OSC}. The loop bandwidth of the proposed PLL was determined by considering the stability characteristics of the PLL and the parameters, such as the loop filter capacitor, the resistor, the Charge Pump current (I_{CP}), and the SAW_OSC gain.

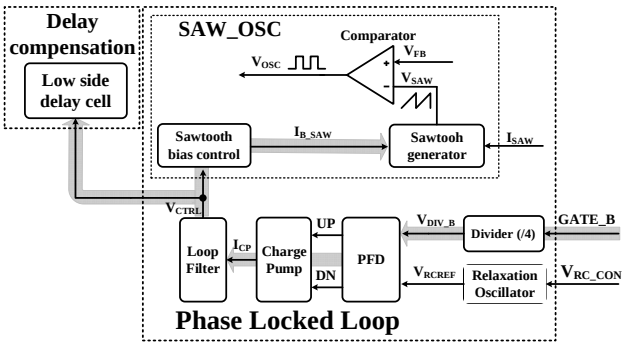


Fig. 2. The block diagram of the proposed PLL.

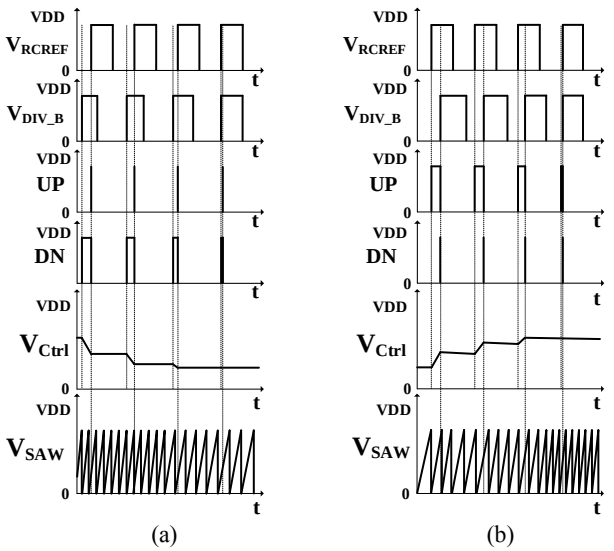


Fig. 3. The waveforms of the proposed PLL when (a) $f_{RCREF} < f_{DIV\_B}$ (b) $f_{RCREF} > f_{DIV\_B}$.

Fig. 3(a) and (b) show waveforms of the proposed PLL when the frequency for V_{DIV_B} (f_{DIV_B}) is lower than and higher than the frequency of V_{RCREF} (f_{RCREF}), respectively.

As shown in Fig. 3(a), if f_{DIV_B} is higher than f_{RCREF}, the DN signal is generated, and its duration is determined by the difference in the phase and frequency. Therefore, V_{CTRL} decreases according to the DN signal. On the other hand, if f_{DIV_B} is lower than f_{RCREF}, it generates the UP signal, as shown in Fig. 3(b). In addition, V_{CTRL} increases due to the UP signal.

The frequency of the Sawtooth generator is determined by Eq. (4). In order to generate the frequency from the PLL loop, the constant parameters C_{SAW}, V_{REF_H}, I_{SAW} and I_{B_SAW}, which are determined by the V_{CTRL} voltage, are needed [6].

If the input voltage V_{CTRL} increases, the I_{B_SAW} current of the Sawtooth bias control block increases, and the frequency of V_{SAW} generated by the Sawtooth generator also increases. In contrast, if the V_{CTRL} voltage decreases, the I_{B_SAW} current decreases. Thus, the frequency of V_{SAW} also decreases.

$$f_{SAW} = \frac{(I_{SAW} + I_{B\_SAW})}{C_{SAW} \times V_{REF\_H}} (Hz) \quad (4)$$

where, f_{SAW}, I_{SAW}, I_{B_SAW}, C_{SAW}, and V_{REF_H} are the frequency of the Sawtooth generator, Sawtooth generator default bias current, Sawtooth generator compensation bias current, Sawtooth generator capacitor, and comparator reference voltage.

When the dead-time is increased, the reliability of the DC-DC buck converter is improved. The duration of the dead-time is related to the efficiency. If the duty of the dead-time is increased, the efficiency is decreased. On the other hand, if the duty of the dead-time is decreased, the efficiency can be improved. However, the shoot through current may flow since the duration of the dead-time is too short.

Conventional structures only use a Non-overlap circuit without delay compensation, which can cause reliability problems due to PVT variations or the external environment. It is difficult to get an optimized dead-time with conventional structures.

Therefore, the proposed DC-DC buck converter senses the frequency and delay information related to the GATE_B signal to generate dead-time. After that, the proposed DC-DC buck converter continuously compensates for variations of the dead-time through the PLL and Delay compensation.

A delay mismatch can affect the Non-overlap period for the outputs of the Low side driver and the High side driver which consist of the level shifter and bootstrap circuit. Therefore, the proposed delay mismatch compensation method controls the Low side delay cell to optimize the delay since the High side driver has a larger delay than the Low side driver.

Fig. 4(a) shows waveforms with respect to the delay mismatch between GATE_A and GATE_B when GATE_B is slower than GATE_A. The dead-time between GATE_A and GATE_B decreases since the delay of GATE_B increases. A shoot through current occurs because of the reduced dead time, and this shoot through current issue can be solved by lowering the V_{CTRL} voltage of the PLL.

On the other hand, Fig. 4(b) shows waveforms with respect to the delay mismatch between GATE_A and GATE_B when GATE_B is faster than GATE_A. The dead-time between GATE_A and GATE_B decreases since the delay of GATE_B decreases. In this case, the shoot through current also occurs in the same way as the case of Fig. 4(a) and this issue can be solved by increasing the V_{CTRL} voltage of the PLL.

As can be seen from the two cases explained in Fig. 4(a) and (b), when the PLL is turned off, the shoot through current occurs by variations of the dead-time. This shoot through current issue can be solved by compensating the dead-time variation between GATE_A and GATE_B by turning on the PLL.

Generally, the current mismatch of the charge pump in the PLL can cause a Spur or Noise of the frequency generated by the PLL. Therefore, the proposed DC-DC buck converter

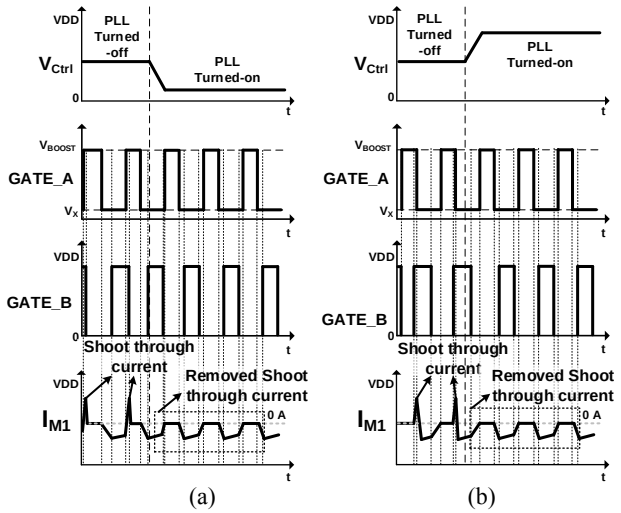


Fig. 4. The waveforms with respect to delay mismatch between GATE_A and GATE_B (a) when GATE_B is slower than GATE_A, and (b) when GATE_B is faster than GATE_A.

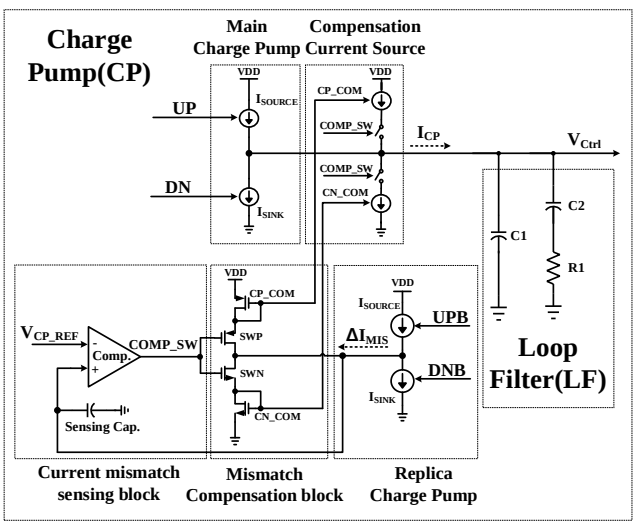


Fig. 5. The proposed Charge Pump and Loop Filter.

which adopts a PLL can have fluctuations in the switching frequency due to the current mismatch of the charge pump.

Fig. 5 shows the proposed CP and LF to solve this problem. When the CP is implemented, the current mismatch between the UP current (I_{SOURCE}) and the DN current (I_{SINK}) needs to be compensated. If there is a mismatch between the UP current and the DN current, there will be fluctuations in V_{CTRL} by the phase difference.

In order to solve this problem, the proposed CP uses a replica charge pump to minimize the current mismatch. This generates constant UP and DN currents from the main charge pump.

The mismatch occurs from the replica charge pump and is compensated by recharging to the compensation current source through the mismatch compensation block. By comparing I_{SOURCE} and I_{SINK}, the CP charges the current with the amount of ΔI_{MIS} as shown in Eq. (5) from the current

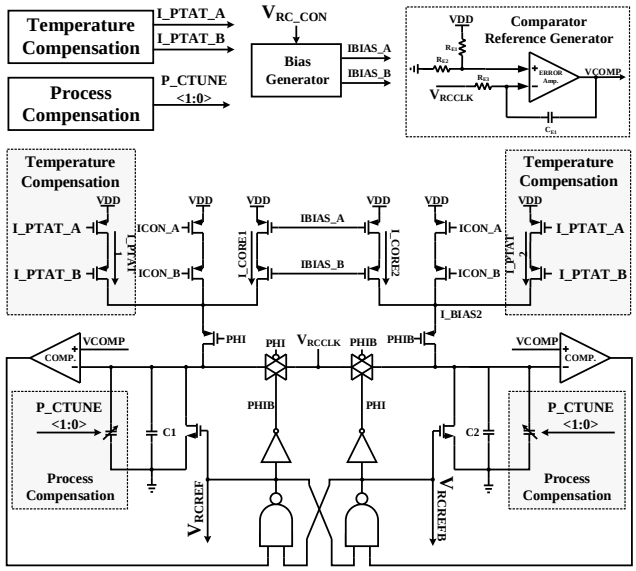


Fig. 6. The block diagram of the proposed Relaxation Oscillator.

mirror [8]. As a result, the current mismatch is minimized.

$$\Delta I_{MIS} = I_{SOURCE} - I_{SINK} \quad (5)$$

where, I_{SOURCE} is the charge pump charging current, and I_{SINK} is the charge pump discharging current.

C. Relaxation Oscillator

Fig. 6 shows a block diagram of the proposed relaxation oscillator. The proposed relaxation oscillator compensates for frequency variations due to process and temperature variations. At first, the input current is changed by the temperature compensation circuit according to temperature variations. This compensates the switching frequency. Secondly, the capacitor is adjusted by the process compensation circuit according to the process variation. In addition, it compensates the switching frequency.

The proposed relaxation oscillator adopts a resistor with a positive temperature coefficient (PTC).

The external factors and temperature have a minimum effect on the supply voltage and the capacitor. However, the current changes depending on the temperature as a result of the transistor characteristics. In order to compensate for this effect, a proportional to absolute temperature (PTAT) circuit and a gain-boosting circuit are adopted [9].

The temperature compensation circuit is designed to increase I_PTAT1 and I_PTAT2, according to the temperature variation. Since I_TOTAL1 and I_TOTAL2 are added as values of I_CORE1, I_PTAT1, I_CORE2, and I_PTAT2, the frequency can be compensated.

The relaxation oscillator frequency is decided by I_{REX} (I_TO the TAL1, 2) and C_{REX} (C1, C2). If the frequency of the relaxation oscillator is set to high, C_{REX} decreases, but I_{REX} (I_TOTAL1, 2) increases, which increases the current consumption. Moreover, if a high frequency is used, variations in the frequency according to PVT variations

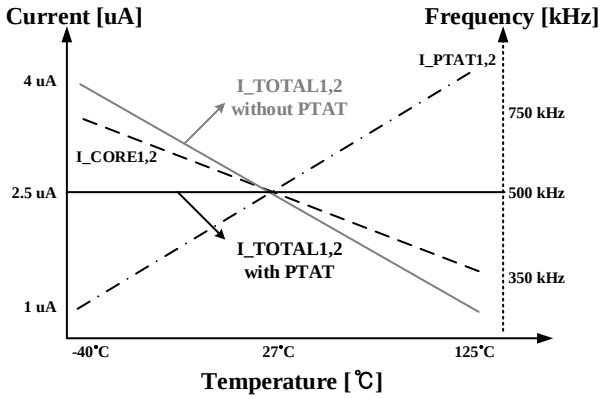


Fig. 7. Operating principle of the proposed Temperature Compensation circuit using PTAT.

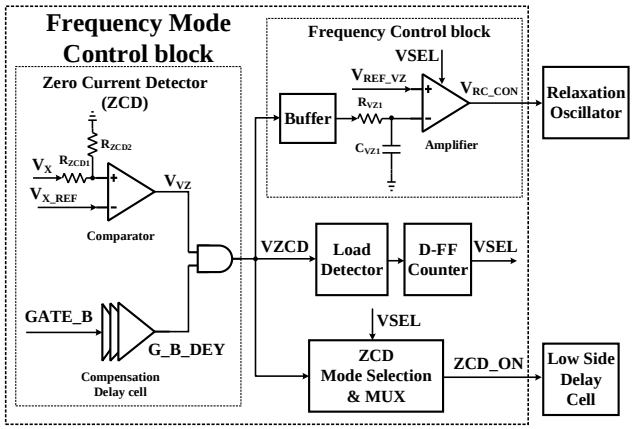


Fig. 8. The block diagram of the proposed Frequency Mode Control block.

increases relative to the low frequency.

The frequency of the relaxation oscillator is proposed to oscillate at 500 kHz, which is one fourth of the switching frequency of the DC-DC buck converter. By setting the frequency of the relaxation oscillator to 500 kHz, the frequency variation is reduced in relative terms.

Fig. 7 shows the operating principle of the proposed temperature compensation circuit using PTAT. In Fig. 7, if PTAT is not applied, the frequency varies from 350 kHz to 750 kHz. In order to control the current of the relaxation oscillator, the PTAT of the BGR senses the temperature. If it is relatively low, the current flow into the core increases, and V_{PTAT} decreases.

D. Frequency Mode Control Block

In order to achieve better results, a frequency mode control block is proposed, as shown in Fig. 8. The frequency mode control block consists of the ZCD, frequency control block, load detector, D-FF counter, ZCD mode selection and MUX [10].

Under a load current below 300 mA, the ZCD senses the V_X node so that the VSEL is changed from low to high. As a result, it can be changed to the PWM frequency mode. The frequency of the relaxation oscillator becomes faster since V_{RC_CON} is increased. Through this high frequency, the inductor ripple can be reduced and the CCM region can be increased. As a result, the proposed PWM frequency mode increases the CCM region under a certain light load condition. When the load becomes lighter and when it enters the DCM region, the ZCD is enabled through the internal ZCD block.

Fig. 9 (a) and 9(b) show waveforms of the proposed variable switching frequency when the frequency control is turned off and on, respectively. In Fig. 9(a), the ZCD is turned off to show the difference between the PWM and the PWM frequency mode depending on the load variation. Another method that has been proposed to reduce reverse current is to change the switching frequency more quickly by controlling V_{RC_CON}, which is the control voltage of the relaxation oscillator. In general, a low frequency affects the inductor

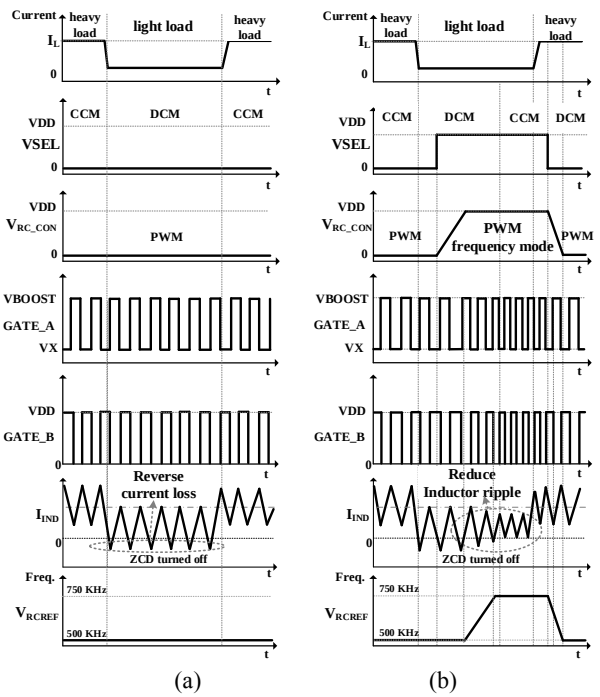


Fig. 9. The waveforms of the proposed variable switching frequency when the frequency control is (a) turned off (b) and turned on.

ripple to become higher, and the reverse current of the inductor decreases.

In Fig. 9 (a), when the load condition is changed from a heavy load to a light load, the DC-DC converter is operated in the DCM region since a fixed frequency is used and inductor ripples occurs as before. In Fig. 9 (b), the DC-DC is operated in the PWM frequency mode. Under the same load conditions, the switching frequency can be increased after a certain time and the inductor ripple can be reduced so that the CCM region is increased.

When the VSEL signal shown in Fig. 9 (b) becomes high under a light load, the V_{RC_CON} signal begins to increase and later, it settles down to a constant voltage. When the load current is also changed from a light load to a heavy load, the

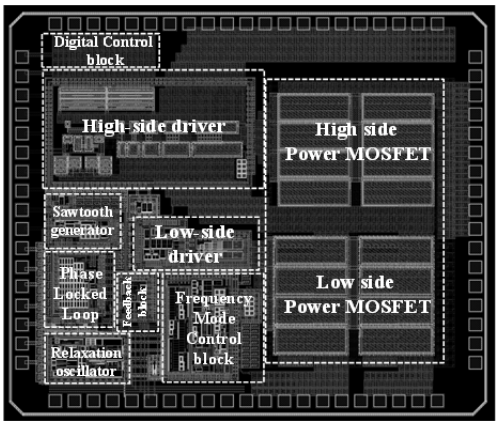


Fig. 10. The chip layout pattern of the proposed DC-DC buck converter with PLL.

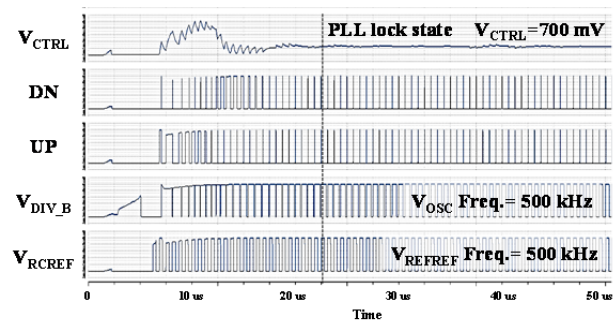


Fig. 11. The simulation results of the proposed PLL.

VSEL is changed to 'Low', and the switching frequency is changed from 750 kHz to 500 kHz when the voltage level of the relaxation V_{RC_CON} is low. By the PWM frequency mode, the CCM region is extended compared to the PWM mode with a fixed frequency. Therefore, a high efficiency can be achieved by reducing the reverse current loss under light load conditions below 300 mA.

III. Experimental Results

The proposed DC-DC buck converter with a PLL was fabricated in 0.18 μm BCD 1 poly 4 metal process with MIM capacitors and high sheet resistance poly resistors. Fig. 10 shows the chip layout pattern of the proposed DC-DC buck converter with a PLL, which has an area of 3.96 mm^2.

Fig. 11 shows the PLL operation of the proposed DC-DC buck converter. After an initial 23 μs, the PEN becomes 'High', and the proposed DC-DC buck converter begins to operate.

The UP signal is generated since V_{DIV_B} is lower than V_{RCREF}, and about 30 μs after PEN, V_{CTRL} settles to 700 mV. The V_{DIV_B} frequency is 500 kHz after settling.

Fig. 12 shows the results of a simulation of the proposed DC-DC buck converter with a PLL. After an initial 23 μs, when the PEN signal becomes high, the DC-DC buck converter starts to operate. When the input voltage (V_{BUCK_IN}) is 12 V and the load current is 1.2 A, V_{CTRL} settles to 700 mV, and the frequency for GATE_A and GATE_B that is decided

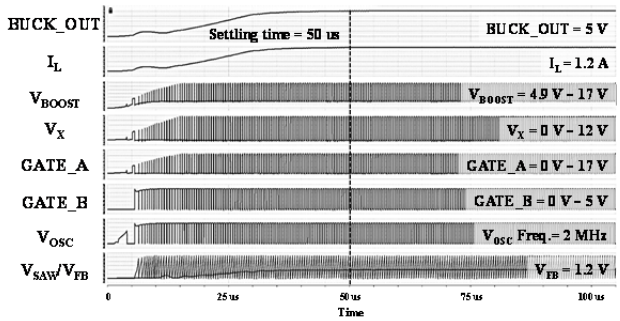


Fig. 12. The simulation results of the proposed DC-DC buck converter with PLL.

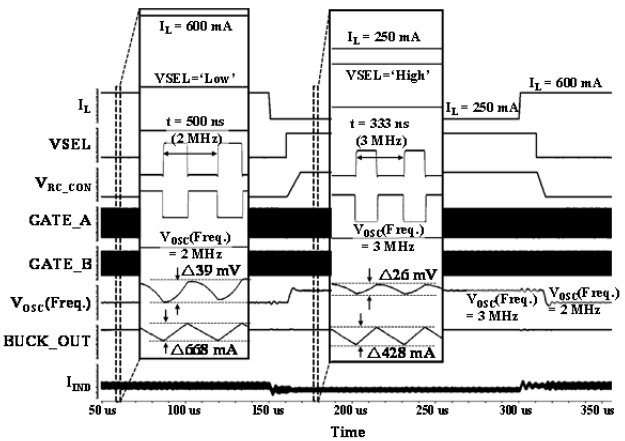


Fig. 13. The simulation results of the proposed DC-DC buck converter at PWM mode and PWM frequency operation with respect to the load current.

by the PLL is 2 MHz. V_{BOOST}, the input voltage for GATE_A, is 4.9 V ~ 16.9 V, and GATE_B is 0 V ~ 5 V. The BUCK_OUT voltage is 5 V and the settling time of the DC-DC buck converter is about 50 μs.

Fig. 13 shows waveforms of the proposed DC-DC buck converter under the PWM and PWM modes with respect to the load current. When the load current (I_L) is 600 mA, the switching frequency of the DC-DC buck converter is 2 MHz and the VSEL signal is changed to Low. The ripple of the inductor current (I_{IND}) is 668 mA and the voltage ripple of BUCK_OUT is 39 mV, from Fig. 13.

On the other hand, when the load current (I_L) is 250 mA, the switching frequency of the DC-DC buck converter is 3 MHz, and the VSEL signal is changed to High.

From Fig. 13, the ripple of the inductor current (I_{IND}) is 428 mA, and the voltage ripple of BUCK_OUT is 26 mV. In the PWM frequency mode, the switching frequency of the DC-DC buck converter becomes faster than the PWM mode, which reduces the inductor current (I_{IND}) ripple.

Fig. 14 shows the test board of the proposed DC-DC buck converter with a PLL.

Fig. 15 shows measured waveform of the proposed DC-DC buck converter with a PLL for a load current of 700 mA. When the load current becomes 700 mA, the duty ratios for GATE_A, GATE_B, and the dead-time are 67 % (335 ns), 32 % (160 ns),

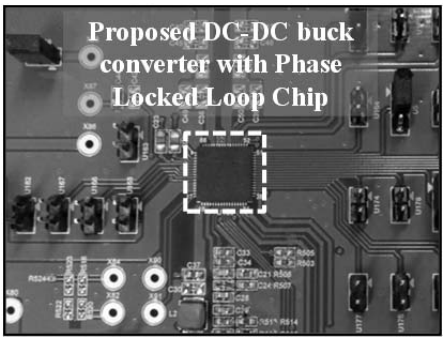


Fig. 14. The test board of the proposed DC-DC buck converter with PLL.

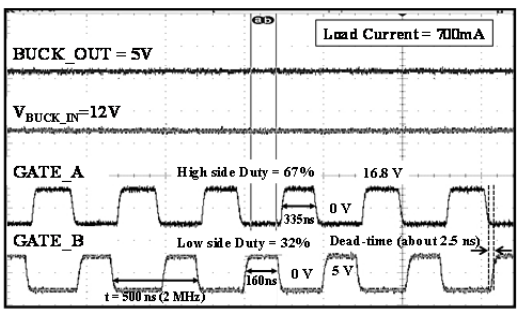


Fig. 15. The measured waveforms of the proposed DC-DC buck converter with PLL for a load current of 700 mA.

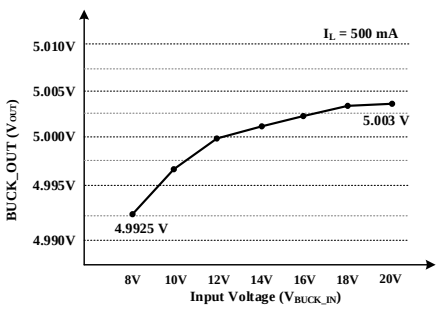


Fig. 16. The measured line regulation characteristics.

and 1 % (about 5 ns), respectively. The duty ratios of GATE_A and GATE_B change, and the constant dead-time period occurs according to the load current.

Fig. 16 shows the measured line regulation characteristics. The total line regulation characteristic of the DC-DC buck converter is 0.875 mV/V when changing the input voltage (V_{BUCK_IN}) from 8 V to 20 V. This means that the output voltage varies from 4.9925 V to 5.003 V.

Fig. 17 shows the measured load regulation characteristics. The load regulation characteristics are measured as 11 mV/A when the load current changes from 0 A to 1.2 A, and the output varies from 4.997 V to 5.008 V.

Figs. 18(a) and 18(b) show the power efficiency measured at a load current of 1.2 A with respect to a variable input voltage when the PLL compensation is turned off and on, respectively. When the PLL compensation is turned off, the switching frequency changes considerably from 1.6 MHz to 2.5 MHz with respect to temperature variations, as shown in Fig. 18(a).

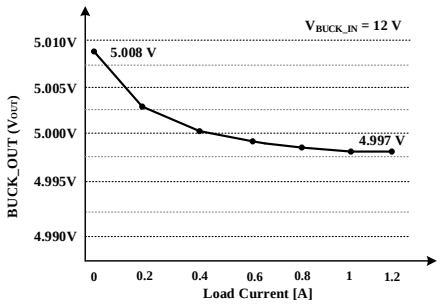
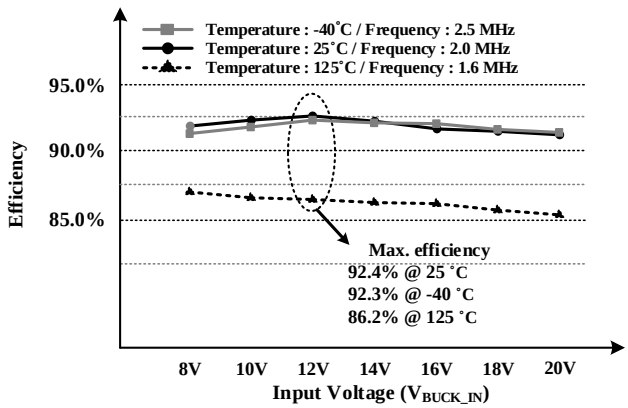
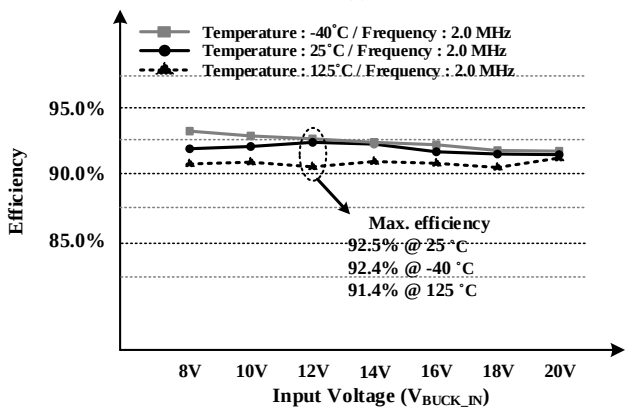


Fig. 17. The measured load regulation characteristics.



(a)



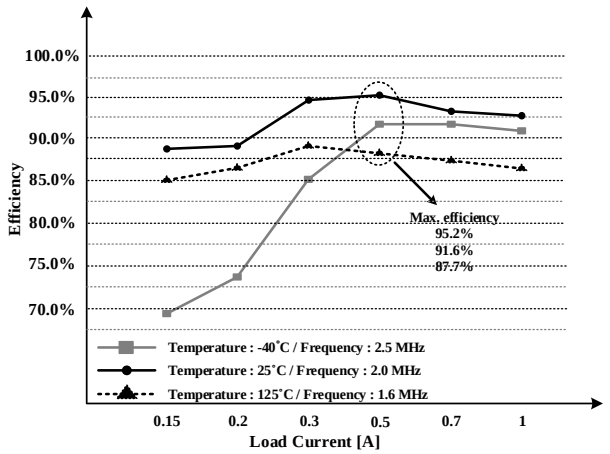
(b)

Fig. 18. Power efficiency measured for the proposed DC-DC buck converter when the PLL Compensation is (a) turned off, and (b) turned on.

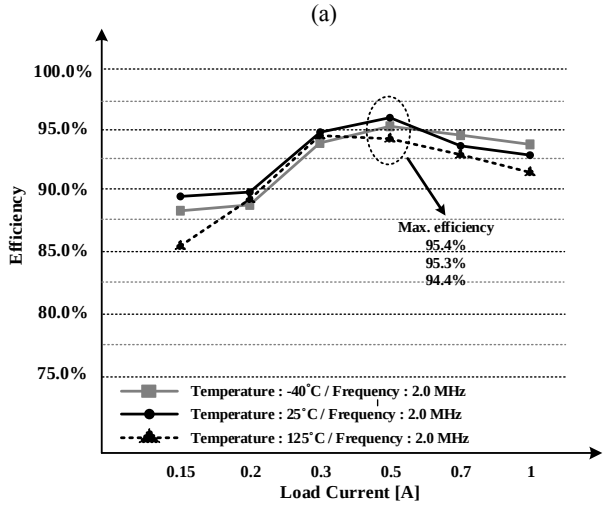
On the other hand, when the PLL compensation is turned on, the switching frequency is constant at 2 MHz, as shown in Fig. 18(b). Therefore, the efficiency is almost the same (within a 1 % error) for all of the cases at 25 °C, -40 °C and, 125 °C, as shown in Fig. 18(b).

This causes a frequency problem and a delay mismatch issue that decreases the efficiency of the DC-DC buck converter. As shown in Fig. 18(a) and 18(b), when the PLL is turned off and the input voltage is 12 V, the power efficiency difference is 6.3 %; and when the PLL is turned on and the input voltage is 12 V, the power efficiency difference is 0.9 %.

According to Eq. (1), (2) and (3), when the PLL



(a)



(b)

Fig. 19. Power efficiency of the proposed DC-DC buck converter with respect to the various load currents when the PLL compensation is (a) turned off, and (b) turned on.

compensation is turned off and the temperature is 25°C, the calculated conduction loss and the switching loss are 115.79 mW and 36.8 mW, respectively. However, the conduction loss and switching loss are 155 mW and 206 mW at 125 °C. The efficiency is decreased by the changed frequency and the delay mismatch at 125 °C. When the dead-time decreases or disappears, the diode reverse recovery loss and switching loss increase degrading the power efficiency.

Figs. 19(a) and (b) show the power efficiency measured at an input voltage of 12 V with respect to a variable load current when the PLL compensation is turned off and on, respectively. When the PLL compensation is off, the frequency changes considerably from 1.6 MHz to 2.5 MHz with respect to temperature variations, as shown in Fig. 19(a).

As shown in Fig. 19(a), when the PLL is turned off and the load current is 0.5 A, the power efficiency difference is 7.7 %; and when the PLL is turned on and the load current is 0.5 A, the power efficiency difference is 1 %. On the other hand, when the PLL compensation is turned on, the switching frequency becomes constant at 2 MHz due to the PLL

TABLE I
THE MEASUREMENTS FOR THE PROPOSED DC-DC BUCK CONVERTER WITH PLL

Parameter	Value		
I_L	0.15 A	0.5 A	1.2 A
BUCK_OUT	5 V	5 V	5 V
Output Power	750 mW	2.5 W	6 W
I_{IN}	66.7 mA	214 mA	537.4mA
V_{BUCK_IN}	12 V	12 V	12 V
Input Power	833.8 mW	2.62 W	6.4938 W
Sub-block Power consumption	37 mW	40 mW	45 mW
Quiescent Current	4.5mA (@ No Load)		
Power MOSFET Ron	50 mohm (W : 120 mm / L : 1.3 um, Load current : 0.5 A)		
Total loss	83.8 mW	120 mW	493.8 mW
Efficiency	89.9 %	95.4 %	92.5 %

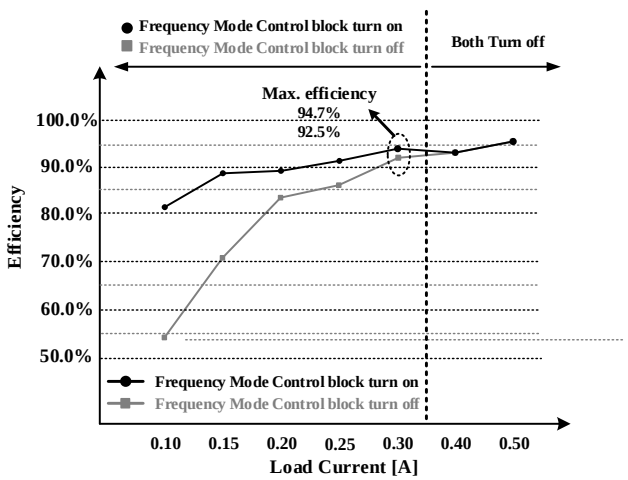


Fig. 20. Power efficiency measured for the proposed DC-DC buck converter with PLL when the Frequency Mode Control block is turned on or off.

operation, as shown in Fig. 19(b).

As shown in Fig. 19(a), the power efficiency is decreased by the change of the switching frequency and delay mismatch at 125 °C and -40 °C. When the dead-time decreases or disappears, the diode reverse recovery loss and switching loss increase degrading the power efficiency.

Table I shows the measured details according to the load current (I_L) of the proposed DC-DC buck converter with a PLL. When the load current is 1.2 A, the output power is 6 W, and the input power, including the sub-block power consumption and loss, is 6.4938 W. Thus, the efficiency is 92.5 %

Fig. 20 shows the power efficiency measured at an input voltage of 12 V with respect to a variable load current when the frequency mode control block is turned on and off,

TABLE II
A SUMMARY OF THE MEASURED PERFORMANCE

Reference	[11]	[12]	[13]	This Work
Technology	1 μm SOI	0.35 μm BCD	0.18 μm CMOS	0.18 μm BCD
Input Voltage range (V)	20	2.9-4.5	2.7-5.5	8-20
Switching freq. (MHz)	1	1	2.5	2
Output DC voltage (V)	5	4.9	0 – 5	5
Max. Load current (A)	1.2	0.3	2	1.2
Value of Indictor (μH)	4.7	10	1	2.2
Duty Ratio (%)	N/A	N/A	N/A	25~62
Max. PCE (%)	91	90.5	91	95.4
Die Area (mm^2)	6	2.94	4.13	3.96

respectively. When the frequency mode control block is turned on, the proposed DC-DC buck converter has an efficiency of over 80 % under a light load through the operation of the PWM frequency mode.

As shown in Table II, the proposed DC-DC buck converter is designed to generate an output of 5 V under a wide input voltage range of 8 V to 20 V compared to the reference [11]-[13].

In particular, a load current range of 0 A to 1.2 A is even wider when compared to reference [11].

A smaller inductor value is used, compare with references [11], [12], by adopting a high switching frequency. In addition, the maximum Power Conversion Efficiency (PCE) is 95.4 %, which is superior to that in references [11]-[13].

IV. CONCLUSION

In this paper, a DC-DC buck converter using a PLL is proposed to generate a constant switching frequency and to compensate for the delay mismatch between the High side and Low side drivers. It also controls the operation mode automatically from the PWM mode to the PWM frequency mode by sensing the load current in order to achieve a high efficiency. The PWM frequency mode is used to extend the CCM region under a light load for the PWM operation. As a result, a high efficiency can be achieved under the light load condition by the PWM frequency mode and delay compensation with a PLL.

Therefore, the proposed DC-DC buck converter has an efficiency of over 80% under light loads (under 300 mA) through the operation of the PWM frequency mode.

The proposed chip was fabricated with a 0.18 μm BCD process, and the area is 3.96 mm^2. The maximum power efficiency of the proposed DC-DC buck converter with a PLL is 95.4 %.

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