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Input-Constrained Current Controller for DC/DC Boost Converter

Woo Jin Choi*, Seok-Kyoon Kim**, Juyong Kim***, and Kyo-Beum Lee†

*,†Department of Electrical and Computer Engineering, Ajou University, Suwon, Korea
**Vehicle Component Technology Center, LG Electronics, Seoul, Korea
***Smart Power Distribution Lab, Korea Electric Power Co., Daejeon, Korea

Abstract

This paper presents a simple input-constrained current controller for a DC/DC boost converter with stability analysis that considers the nonlinearity of the converter model. The proposed controller is designed to satisfy the inherent input constraints of the converter under a physically reasonable assumption, which is the first contribution of this paper. The second contribution is providing a rigorous proof of the proposed control law, which keeps the closed-loop system along with the internal dynamics stable. The performance of the proposed controller is demonstrated through an experiment employing a 20-kW DC/DC boost converter.

Key words: Current controller, DC/DC boost converter, Input-constraints

I. INTRODUCTION

DC/DC converters are used in several applications, such as solar PV systems, personal computers, computer peripherals, and adapters of consumer electronic devices [1]. For these applications, DC/DC converters with acceptable output voltage tracking performance and stability guarantee are necessary despite its inherent input constraints [2]-[10].

Traditionally, the cascade output voltage strategy [11], which employs an inner-loop current controller and an outer-loop voltage controller in a cascaded manner, has been commonly adopted in many industrial applications. Both inner- and outer-loop controllers have been implemented using the proportional-integral (PI) control method due to its simplicity [11]-[13]. However, in the case of boost and buck-boost converters, the closed-loop performance of the PI-type inner-loop current control system clearly varies as the output voltage operation mode changes because of nonlinearities of these converters. Moreover, it is unclear whether the closed-loop stability is still preserved in the presence of input constraints or remains unknown.

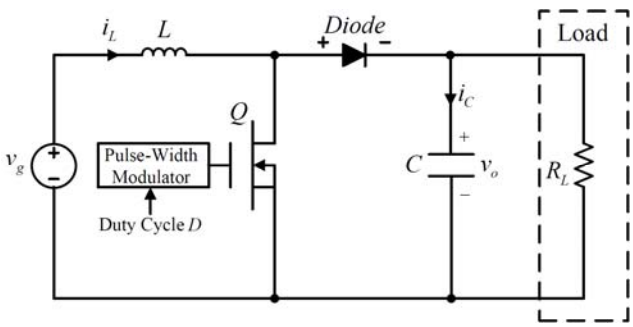

Fig. 1. DC/DC boost converter.

Many solutions have been proposed to improve the closed-loop performance by using advanced control algorithms, such as deadbeat controllers [14], [15], predictive controllers [16], [17], sliding mode controllers [18], [19], and adaptive controllers [20]-[21], which guarantee closed-loop stability without considering the input constraints of the converter. Recently, in [22], a novel current controller that considered the parameter uncertainties was developed. In this controller, the optimality is obtained by solving an optimization problem that involves the lower and upper bounds of the parameters.

The model predictive control (MPC) method, which is an

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Recommended for publication by Associate Editor Chun-An Cheng.
†Corresponding Author: kyl@ajou.ac.kr
Tel: +82-31-219-2376, Fax: +81-31-212-9531, Ajou University
*Dept. of Electrical and Computer Eng., Ajou University, Korea
**Vehicle Component Technology Center, LG Electronics, Korea
***Smart Power Distribution Lab, Korea Electric Power Co., Korea

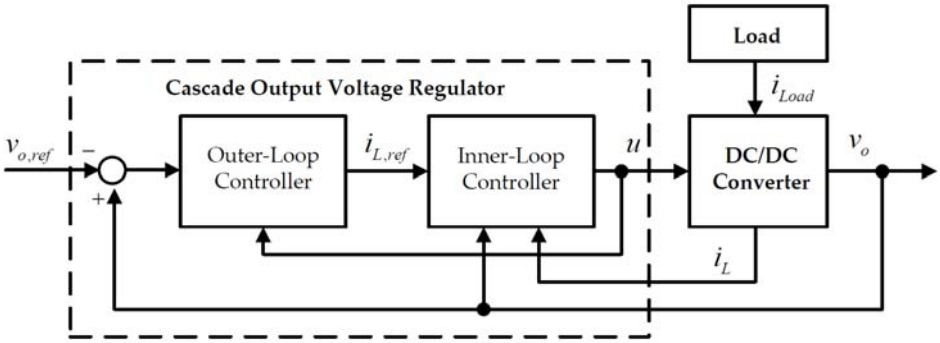

Fig. 2. Cascade voltage control system.

efficient method to stabilize plants, numerically optimizes a cost function on-line to handle the input/state constraints [23]. Recently, deadbeat-based [24], [25] and explicit MPCs [26], [27] have been developed to reduce online computational burden and implement the method using practical digital signal processors (DSPs) with acceptable sample period.

This paper proposes an input-constrained current controller for the inner-loop utilized in the cascade output voltage control strategy. The proposed method has the following novelties: a) the physical input constraints are handled effectively by a simple membership test without any numerical method unlike in [26], [27], while guaranteeing closed-loop stability, b) the proposed method has to be capable of stabilizing the current error dynamics and the closed-loop system, including the first-order internal dynamics. In particular, the proposed control law is designed to stabilize the inductor current tracking error dynamics by assigning the tracking error damping term after simple nonlinearity cancellations. The damping gain is adjusted in order to ensure that the proposed control law satisfies the input constraints at all time while maintaining the stability of the current tracking error dynamics. The closed-loop system, which includes the first-order internal dynamics, is also shown to be asymptotically stable using the Lyapunov stability theorem. Simulation and experimental verifications indicate that the proposed method is a promising alternative solution to the classical PI controller.

II. Mathematical Model of DC/DC Boost Converter

This study is concerned with the standard DC/DC boost converter depicted in Fig. 1, where $D \in [0,1]$ denotes the duty ratio acting as the control input $i_L(t)$ whereas $v_o(t)$ represent the inductor current and capacitor voltage, respectively, as state variables. Duty ratio D determines the switching action through pulse width modulation (PWM). For example, duty ratio $D \in [0,1]$ commands the switch to be turned off for a period of $(1-D)T$, where T refers to the PWM period. Considering the PWM operation, the averaged converter model is easily derived as

$$L\frac{di_L(t)}{dt} = -R_{ON}i_L(t) - v_o(t) + (v_o(t) + v_D)u(t) + v_g - v_D, \ \forall t, \quad (1)$$

$$C\frac{dv_o(t)}{dt} = (1-u(t))i_L(t) - \frac{1}{R_L}v_o(t), \ \forall t, \quad , (2)$$

where $u(t)$ represents duty ratio D because the control input that must be designed to be constrained into the closed interval $[1,0]$, i.e., $u(t) \in [0,1]$, $\forall t$. R_{ON} and v_D denote the switch ON-resistance and diode voltage, respectively. For a detailed derivation of the averaged model (1)–(2), see [4].

Before designing the current controller for dynamics (1)–(2), we considered the following assumptions:

1) $i_L(t) \geq 0$ and $v_o(t) \geq 0$ for all time [28].

2) The inductor current and output (capacitor) voltage can be measured.

III. Input-Constrained Current Controller Design

This section derives an input-constrained current control law for a DC/DC boost converter whose dynamics are governed by bilinear differential equations (1)–(2) under the three assumptions given in Section 2. The control objective of the current controller is given by

$$\lim_{t\to\infty} i_L(t) = i_{L,ref}, \quad (3)$$

under the following input constraints,

$$u(t) \in [0,1], \ \forall t. \quad (4)$$

Note that the inner-loop controller which guarantees the control objective (3), can be utilized for the classical cascade output voltage regulator shown in Fig. 2.

Section III. *A.* shows the design of the input-constrained current controller, whereas Section III. *B.* provides a rigorous analysis of the closed-loop stability.

A. Controller Design

The dynamical equation (1) of the inductor current can be rewritten in terms of the tracking error:
$e_1(t) := i_L(t) - i_{L,ref},\ \forall t$:

$$\begin{aligned} L\dot{e}_1(t) &= -R_{ON}e_1(t) - v_o(t) + (v_o(t) + v_D)u(t) \\ &\quad + v_g - v_D - R_{ON}i_{L,ref},\ \forall t. \end{aligned} \tag{5}$$

To stabilize the tracking error dynamics (5), the proposed control input is given as follows:

$$\begin{aligned} u(t) = \frac{1}{v_o(t) + v_D}(v_o(t) - v_g + v_D + R_{ON}i_{L,ref} \\ - k(t)e_1(t)),\ \forall t, \end{aligned} \tag{6}$$

where the time-varying damping gain $k(t)$ is defined as

$$k(t) := \begin{cases} k \text{ if } u(t)\big|_{k(t)=k} \in [0,1], \\ 0 \text{ if } u(t)\big|_{k(t)=k} \notin [0,1], \end{cases} \tag{7}$$

with $k > 0$ as a design parameter.

At this point, the feasibility of the proposed control law (6) for all time remains uncertain, i.e., $u(t) \in [0,1]$ and $\forall t$. Therefore, Theorem 1 proves the feasibility of the proposed controller (6) under the assumption that the output voltage $v_o(t)$ is bounded below for some constant such that

$$v_o(t) \geq \max\{v_g - v_D - R_{ON}i_{L,ref}, 0\},\ \forall t \geq 0. \tag{8}$$

Theorem 1: For any $i_{L,ref}$ satisfying

$$0 < i_{L,ref} < \frac{v_g}{R_{ON}}, \tag{9}$$

assume that inequality (8) holds. The proposed control law (6) fulfills the input constraints (4) for all time. i.e.

$$u(t) \in [0,1],\ \forall t. \tag{10}$$

Proof: Considering the definition of the proposed control input (6)–(7), the proof can be completed by showing that

$$u(t)\big|_{k(t)=0} \in [0,1],\ \forall t. \tag{11}$$

Inequality (8) with $i_{L,ref} > 0$ implies that

$$\begin{aligned} u(t)\big|_{k(t)=0} &= \frac{1}{v_o(t) + v_D}(v_o(t) - v_g + v_D + R_{ON}i_{L,ref}) \\ &\geq 0,\ \forall t, \end{aligned} \tag{12}$$

and inequality (9) means that

$$u(t)\big|_{k(t)=0} = 1 - \frac{v_g - R_{ON}i_{L,ref}}{v_o(t) + v_D} \geq 1,\ \forall t. \tag{13}$$

Therefore, it can be concluded that

$$u(t)\big|_{k(t)=0} \in [0,1],\ \forall t. \tag{14}$$

Remark 1: Because of $R_{ON} \approx 0$, the admissible range of the inductor current reference described in (9) would be sufficiently large. Thus, condition (9) is not considerably restrictive.

Remark 2: The inductor current $i_L(t)$ driven to its reference $i_{L,ref} > 0$ by the proposed controller (6) boosts the output voltage $v_o(t)$ to some value $v_o^* > v_g$, where $v_o^*(t)$ is the output voltage reference.

Remark 3: The proposed input constrained-current controller of (6)–(7) can be implemented through IF-THEN logic as follows:

If

$$\left[0 < \frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref} - ke_1)\right]$$

and $\left[\frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref} - ke_1) < 1\right]$

then,

$$u(t) = u(t)|_{k(t)=k} = \frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref} - ke_1).$$

Else, i.e.,

$$\left[\frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref} - ke_1) < 0\right]$$

or $\left[\frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref} - ke_1) > 1\right]$

then,

$$u(t) = u(t)|_{k(t)=0} = \frac{1}{v_o + v_D}(v_o - v_g + v_D + R_{ON}i_{L,ref}).$$

B. Stability Analysis

This section provides an analysis of the closed-loop stability under assumptions of the Theorem 1. First, Lemma 1 asserts that the proposed controller (6) establishes the control objective (3) by showing that a positive-definite function with respect to the tracking error $e_1(t)$ decreases monotonically.

Lemma 1: Suppose that all assumptions of the Theorem 1 hold. The proposed control law (6) ensures the achievement of control objective (3) while satisfying the input constraint (4).

Proof: The proposed control law (6) obviously satisfies input constraint (4) through the Theorem 1, causing the inductor current error dynamics (5) to be satisfied as

$$L\dot{e}_1(t) = -(R_{ON} + k(t))e_1(t),\ \forall t. \tag{15}$$

Using the closed-loop error dynamics (15), the positive-definite function $V(e_1(t))$ designed as

$$V(e_1(t)) := \frac{L}{2}e_1^2(t),\ \forall t, \tag{16}$$

satisfies

$$\begin{aligned} \dot{V}(e_1(t)) &= -(R_{ON} + k(t))e_1^2(t) \\ &\leq -R_{ON}e_1^2(t) < 0,\ \forall t, \end{aligned} \tag{17}$$

because $k(t) \geq 0$, $\forall t$ (see(7)). These Equations imply that

$$\lim_{t\to\infty} i_L(t) = i_{L,ref}. \tag{18}$$

Although the fact that the proposed control law (6)

asymptotically stabilizes the inductor current tracking error dynamics under the input constraints have been verified, whether the entire closed-loop system including the output voltage dynamics (2) is stable remains unknown. Theorem 2 governs the closed-loop stability analysis.

Theorem 2: Suppose that all assumptions of the Theorem 1 hold, and let v_o be the equilibrium point of the output voltage $v_o(t)$ corresponding to the equilibrium point $i_{L,ref}$ of the inductor current $i_L(t)$. The equilibrium point $(i_L(t), v_o(t)) = (i_{L,ref}, v_o^*)$ of the closed-loop system comprising (1), (2), and (6) is locally and asymptotically stable.

Proof: The proposed control law (6) forces the output voltage dynamics (2) to be governed by

$$\begin{aligned} C\dot{v}_o(t) &= -\frac{1}{R_L}v_o(t) - u(t)i_L(t) + i_L(t) \\ &= -\frac{1}{R_L}v_o(t) + \left(-1 + \frac{k(t)}{v_o(t)+v_D}e_1(t) + \frac{v_g - R_{ON}i_{L,ref}}{v_o(t)+v_D}\right)i_L(t) \\ &\quad + i_L(t),\ \forall t, \end{aligned} \tag{19}$$

where (9) can be linearized at the equilibrium point $(i_L(t), v_o(t)) = (i_{L,ref}, v_o^*)$ as

$$\begin{aligned} C\dot{e}_2(t) &= \left(\frac{k(t) + v_g - R_{ON}i_{L,ref}}{v_o^* + v_D}\right)e_1(t) \\ &\quad - \left(\frac{1}{R_L} + \frac{(v_g - R_{ON}i_{L,ref})i_{L,ref}}{(v_o^* + v_D)^2}\right)e_2(t) \\ &=: c_1(t)e_1(t) - c_2e_2(t),\ \forall t, \end{aligned} \tag{20}$$

where $e_2(t)$ represents the output voltage tracking error defined as $e_2(t) := v_o(t) - v_o^*$, $\forall t$, and $c_1(t)$ and c_2 are defined as

$$\begin{aligned} c_1(t) &= \frac{k(t) + v_g - R_{ON}i_{L,ref}}{v_o^* + v_D},\ \forall t, \\ c_2 &:= \frac{1}{R_L} + \frac{\left(v_g - R_{ON}i_{L,ref}\right)i_{L,ref}}{\left(v_o^* + v_D\right)^2}. \end{aligned} \tag{21}$$

Note that $c_1(t)$ is bounded by the unknown constant $\bar{c}_1$ as

$$|c_1(t)| \le \bar{c}_1 := \frac{k + v_g}{v_o^* + v_D},\ \forall t. \tag{22}$$

Furthermore, $c_2 > 0$ because inequality (9) is assumed to hold. Consider the positive function defined as

$$V_{cl}(\mathrm{e}(t)) := \gamma V(e_1(t)) + \frac{C}{2}e_2^2(t),\ \forall t, \tag{23}$$

where $e(t) := [e_1(t)\ \ e_2(t)]^T$, $\forall t$, γ denotes a positive constant to be determined later. Using inequality (17) in Lemma 1, its time derivative along the trajectory of the system (15) and (20) is given by

$$\begin{aligned} \dot{V}_{cl}(\mathrm{e}(t)) &\le -\gamma R_{ON}e_1^2(t) + e_2(t)\left(c_1(t)e_1(t) - c_2e_2(t)\right) \\ &= -\gamma R_{ON}e_1^2(t) + e_2(t)\left(c_1(t)e_1(t) - c_2e_2(t)\right),\ \forall t. \end{aligned} \tag{24}$$

Applying Young's inequality,

$$xy \le \frac{\varepsilon}{2}x^2 + \frac{1}{2\varepsilon}y^2,\ \forall x, y \in \mathbb{R},\ \forall \varepsilon > 0, \tag{25}$$

and thus, it follows that

$$\dot{V}_{cl}(\mathrm{e}(t)) \le -\eta e_1^2(t) - \frac{c_2}{2}e_2^2(t) < 0,\ \forall t, \tag{26}$$

by setting the positive constant γ as

$$\gamma := \frac{\bar{c}_1^2}{2R_{ON}c_2} + \eta,\ \forall \eta > 0, \tag{27}$$

which implies local asymptotic stability of the closed-loop system.

The theorem 1 shows that the proposed control law (6) satisfies the input constraints (4) under assumption (8). However, proving that the proposed control law (6) satisfies the input constraints (4) for all tracking error trajectories starting from the set of initial conditions is possible by showing the existence of the set of initial conditions that guarantees inequality in assumption (8). For details, see Theorem 3.

Theorem 3: For any tracking error trajectory $\mathrm{e}(t)$ initiated from the set Ω defined as

$$\Omega := \left\{ \begin{array}{l} \mathrm{e}(0) \in \mathbb{R}^2 \left| \sqrt{\frac{2}{\min\{\gamma L, C\}}V_{cl}(e(0))} \right. \\ \left. \le v_o^* - v_g + v_D + R_{ON}i_{L,ref} \right. \end{array} \right\}, \tag{28}$$

the proposed control law (6) fulfills the input constraints (4). That is,

$$\forall \mathrm{e}(0) \in \Omega,\ u(t) \in [0,1],\ \forall t \ge 0. \tag{29}$$

Proof: From integrating inequality (26), it follows that

$$V_{cl}(\mathrm{e}(t)) \le V_{cl}(\mathrm{e}(0)),\ \forall t \ge 0, \tag{30}$$

which gives the inequality,

$$\frac{\min\{\gamma L, C\}}{2}\|\mathrm{e}(t)\|^2 \le V_{cl}(\mathrm{e}(0)),\ \forall t \ge 0. \tag{31}$$

Thus, because $|e_2(t)| \le \|\mathrm{e}(t)\|$, $\forall t$, inequality (31) implies that

$$|e_2(t)| \le \sqrt{\frac{2}{\min\{\gamma L, C\}}V_{cl}(\mathrm{e}(0))},\ \forall t \ge 0, \tag{32}$$

which means the following chain implications hold:

$$\begin{aligned} &\left[\forall \mathrm{e}(0) \in \Omega\right] \\ &\Rightarrow \left[|e_2(t)| \le v_o^* - v_g + v_D + R_{ON}i_{L,ref},\ \forall t \ge 0.\right] \\ &\Rightarrow \left[-(v_o^* - v_g + v_D + R_{ON}i_{L,ref}) \le v_o(t) - v_o^*,\ \forall t \ge 0.\right] \\ &\Leftrightarrow \left[v_g - v_D - R_{ON}i_{L,ref}) \le v_o(t),\ \forall t \ge 0.\right] \end{aligned} \tag{33}$$

Therefore, because inequality (33) implies assumption (8), statement (29) holds true by Theorem 1.

Remark 4: The results of the analysis show that the

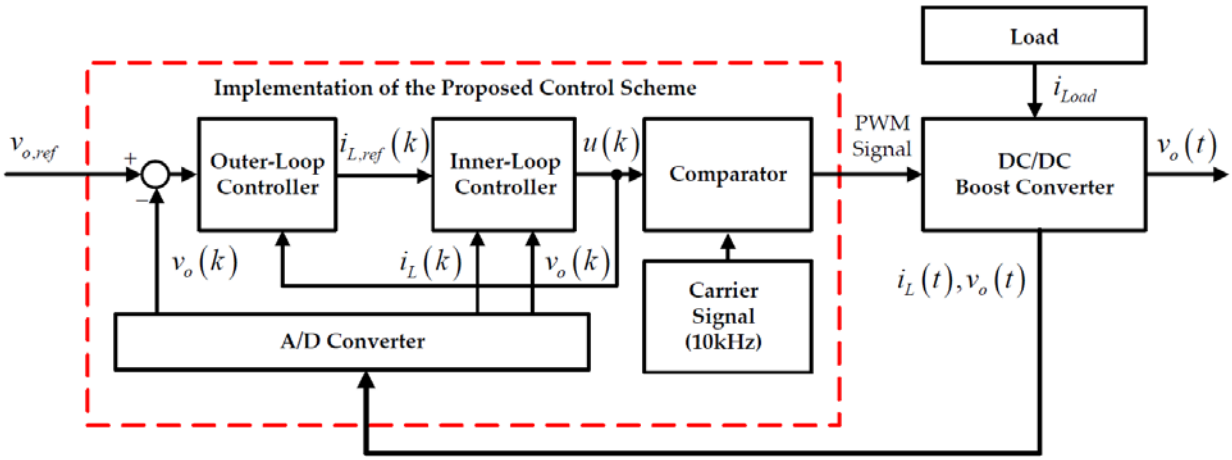

Fig. 3. Implementation of the closed-loop system.

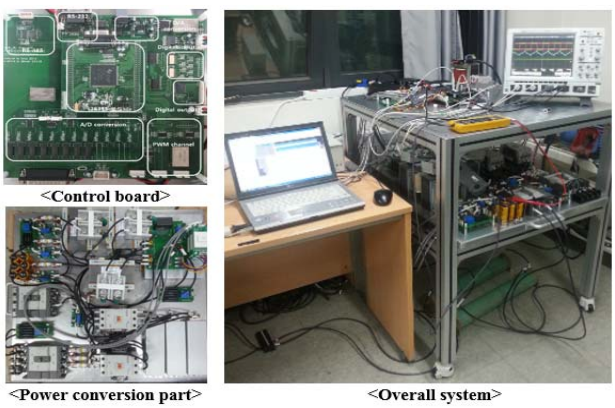

Fig. 4. Experimental setup.

proposed method guarantees the closed-loop stability in the presence of input constraints. These results are in sharp contrast to the classical PI method in the control theoretical point of view.

IV. Experiments and Results

This section describes the experimental evaluation of the closed-loop performance and its comparison with the classical PI scheme.

An experimental 20kW boost converter system is developed to demonstrate the performance of the proposed control scheme. The experimental setup of Fig. 4 consists of two sections: power and measurement, and control. The power section includes the main power switching device and other components. The proposed control algorithm and other software features are implemented by using a TMS320F028335.

A 20-kW DC/DC boost converter with parameters listed in Table I was used. Resistance R_L=40Ω was used as converter load. Fig. 3 shows the implemented closed-loop system using DSP28335. The sampling and PWM periods were both set to 100μs.

TABLE I
Experiment Parameters

Input Voltages (v_g)	Low Condition	80V
	High Condition	220V
Output Voltages (v_o)	Low Condition	150V
	High Condition	400V
Rated Power		20 kW
Input Voltage Side Inductance (L)		130 μH
Output Capacitance (C)		1500 μF
Switching Frequency		10 kHz
Switch ON Resistance (R_{ON})		0.1 Ω
Diode Voltage (v_D)		0.707V

The first experiment was performed to demonstrate the inductor current tracking performance for the inductor current reference $i_{L,ref} = 20\text{A}$ and the input source voltage $v_g = 100\text{V}$. The damping gain was chosen to be $k = 5$, and the initial conditions of the inductor and output voltage were set to

$$i_L(0) = 7\,\text{A},\ v_o(0) = 150\text{V},$$

where $\mathrm{e}(0) \in \Omega$ to ensure that the control law is satisfied for all time (Theorem 3). The resulting inductor current tracking performance, output voltage, and corresponding control input (duty) behaviors are depicted in Fig. 5, where $u(t)\big|_{k(t)=k}$ denotes the unconstrained control defined in (7).

These experiments confirm that the proposed control law provides an acceptable inductor current tracking performance while efficiently constraining the control input (duty) to the The second experiment was conducted to compare the output voltage tracking performance with that of the classical cascade PI method, where the output voltage tracking performance was evaluated by replacing the inner-loop PI controller with the proposed controller. The inner- and

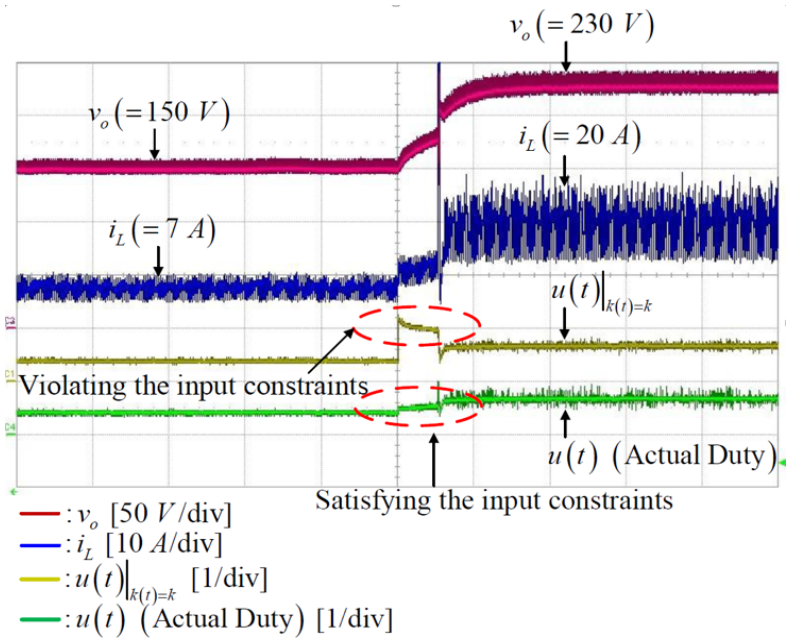

Fig. 5. Current tracking performance of the proposed method.

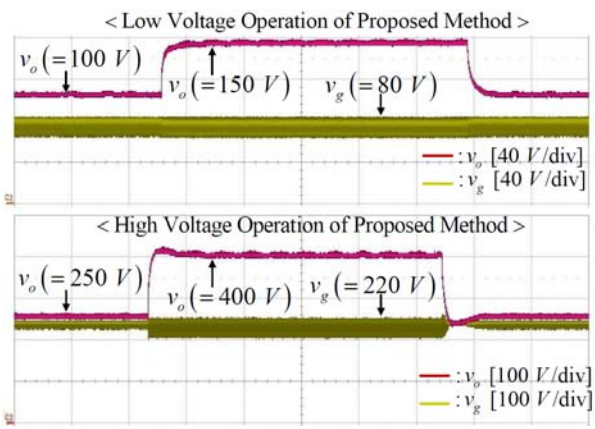

Fig. 6. Output voltage tracking performance of the proposed method in the low- and high-voltage operation modes.

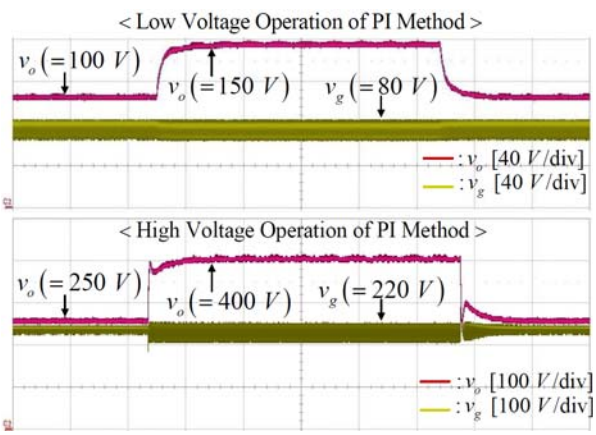

Fig. 8. Output voltage tracking performance of the PI method in the low- and high-voltage operation modes.

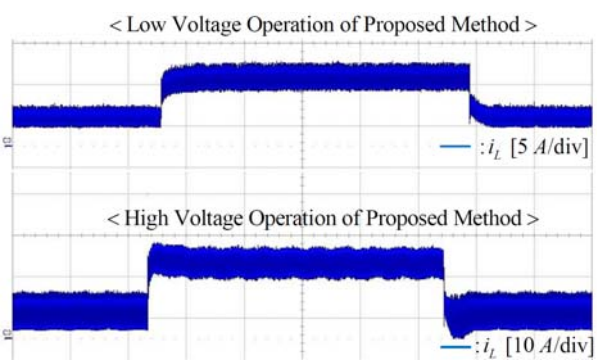

Fig. 7. Inductor current response of the proposed method in the low- and high-voltage operation modes.

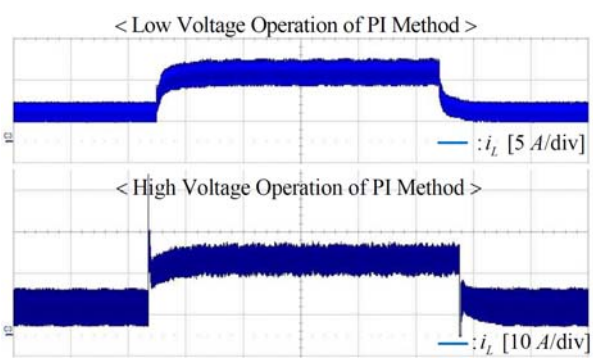

Fig. 9. Inductor current response of the PI method in the low- and high-voltage operation modes.

admissible interval [0; 1] for all time. This step is the main advantage of this proposed method.
outer-loop PI gains were tuned as

$$k_{P,inner} = 0.01,\ k_{I,inner} = 1,\ k_{P,outer} = 0.1,\ k_{I,outer} = 1,$$

for the best inductor current and output voltage tracking performance with tolerable overshoot. The same damping gain as that in the first experiment was chosen for the proposed method. The two operating modes were considered in this experiment.

1) Low-voltage operating mode

$v_g = 80\text{V},\ v_o(0) = 100\text{V},\ i_L(0) = 3\text{A},\ v_{o,ref} = 150\text{V}$

($v_{o,ref}$ is the output voltage reference)

2) High-voltage operating mode

$v_g = 220\text{V},\ v_o(0) = 250\text{V},\ i_L(0) = 6\text{A},\ v_{o,ref} = 400\text{V}$

Figs. 6 and 7 show the closed-loop performance of the proposed method in the low- and high-voltage operation modes, while Fig. 8 and 9 show the closed-loop performance of the PI method in the same operating modes.

Figs. 6 and 9 show that the PI method suffers from severe closed-loop performance degradation, whereas the proposed method succeeds in preserving similar closed-loop performance as in the low-voltage operation case. However, the closed-loop performance can be recovered by using other PI gains, which is an expected result, because the closed-loop poles of the inner-loop PI control system, depend on the output voltage.

These experimental verifications show that the proposed method can be used efficiently for solar power generation applications as an alternative solution to the classical PI method because unlike the classical PI method, the proposed method will provide the desired closed-loop performance over a wide operating region.

V. CONCLUSIONS

This paper presented a simple input-constrained current controller for a DC/DC boost converter by considering the nonlinearity of the converter model. The proposed control law includes nonlinear cancellation terms and a tracking error damping term to stabilize the inductor current tracking error dynamics. The input constraints of the converter are treated by assigning the damping gain appropriately while the closed-loop current tracking error dynamics is stable. The closed-loop stability, which includes the internal dynamics, is analyzed rigorously. Finally, using realistic simulations and experiments, the proposed method is verified to be an effective solution to the output voltage tracking problem of the DC/DC boost converter.

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Woo Jin Choi received his B.S. degree in Electrical Engineering from Semyung University, Jecheon, South Korea in 2012. He received his M.S. in Electrical and Computer Engineering degree from Ajou University, Suwon, South Korea in 2014. He is currently working toward his Ph.D. degree at Ajou University. His research interests include grid-connected system, machine drives, and DC-DC converter.

Seok-Kyoon Kim received his B.S. degree from the Seoul National University of Science and Technology, Seoul, South Korea in 2004, and his Ph.D. degree in electrical engineering from the Korea University, Seoul, South Korea in 2014. He has worked for the Vehicle Component Technology Center, LG Electronics as a Senior Research Engineer since 2015. His research interests include passivity-based control, nonlinear adaptive control, power system stabilization problems of power electronic applications such as power converters and motor drive.

Juyong Kim received his M.S. and Ph.D. degrees in Electrical and Electronic Engineering degrees from the Kyungpook National University, Daegu, South Korea in 1994 and 2007, respectively. He joined the Korea Electric Power Research Institute, KEPCO in 1994. His current research interests include design and control of DC distribution system.

Kyo-Beum Lee received his B.S. and M.S. in Electrical and Electronic Engineering degrees from Ajou University, Suwon, South Korea in 1997 and 1999, respectively. He received his Ph.D. in Electrical Engineering degree from Korea University, Seoul, South Korea in 2003. He was a part of the Institute of Energy Technology, Aalborg University, in Aalborg, Denmark from 2003 to 2006. He was a part of the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea from 2006 to 2007. He joined the Department of Electrical and Computer Engineering, Ajou University, Suwon, South Korea in 2007. His current research interests include electric machine drives, electric vehicles applications, and renewable power generation. He is an associate editor of the IEEE Transactions on Power Electronics, the Journal of Power Electronics, and the Journal of Electrical Engineering & Technology.