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Novel High Step-Up DC/DC Converter Structure Using a Coupled Inductor with Minimal Voltage Stress on the Main Switch

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Abstract

A high-step-up DC/DC converter for renewable energy systems is proposed. The proposed structure provides high voltage gain by using a coupled inductor without the need for high duty cycles and high turn ratios. The voltage gain is increased through capacitor-charging techniques. In the proposed converter, the energy of the leakage inductors of the coupled inductor is reused. This feature reduces the stress on the switch. Therefore, a switch with low ON-state resistance can be used in the proposed converter to reduce losses and increase efficiency. The main switch is placed in series with the source. Therefore, the converter can control the energy flow from the source to the load. The operating principle is discussed in detail, and a steady state analysis of the proposed converter is conducted. The performance of the proposed converter is verified by experimental results.

Key words: Coupled inductor, High step-up DC–DC converter, Low voltage stress, Renewable energy systems

I. INTRODUCTION

Nowadays, DC/DC converters with high step-up gains are widely utilized for many applications, such as high-intensity discharge lamp ballasts for automobile headlamps, accelerators, modulators, X-ray generators, and solar-cell energy converters [1]. Photovoltaic (PV) sources have become increasingly popular in the last 10 years, and estimations show that a significant portion of renewable energy in the future will be produced by PV sources because PV systems do not create pollution and are highly reliable [2], [3]. The output voltage of a PV panel is low (about 15 V to 40 V) [4]. Therefore, several panels must be connected in series to produce high voltage. However, when the number of panels is increased, the partial shading effects on PV sources become difficult to avoid [5]-[7]. High-gain DC/DC converters must be used to increase the output voltage and efficiency, especially in grid-connected applications [8].

Theoretically, the common boost converter can provide high output voltage with an extremely high duty cycle [9], [10]. However, this converter is limited because of the effect of power switches, diodes, and equivalent series resistance (ESR) of the inductors and capacitors. Moreover, the voltage stress on the main switch is equal to the output voltage, and the converter's control and stability at high duty cycles are extremely complex [11]. A solution is to utilize high-turn-ratio transformers, such as flyback converters. However, these transformers are expensive, large, and heavy, and the voltage stress on the main switch and the leakage losses are high [12]. Using active clamp and snubber circuits can address these problems, but driver circuits are inconvenient because of the high-power switch [13]. The characteristics of non-ideal elements deteriorate in high-voltage transformers with extremely high turn ratios. Consequently, the leakage inductance of the transformers causes adverse voltage spikes [14]. In addition, the distribution capacitors of transformers cause current spikes and a slow rise time in the output. These two non-ideal features increase the switching losses and decrease the efficiency and reliability of the converter [15].

Several converters have been presented to achieve high

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step-up voltage gain [16]-[32]. Coupled inductors are used to obtain high step-up voltage gain in non-isolated converters [16]-[18]. The main drawback of these converters is the leakage inductance of the coupled inductor, which increases the voltage stress on switches [19]. Active clamping can result in high voltage spikes and reduce switching losses [26]. A high-step-up DC/DC converter that employs a coupled inductor and a capacitor was presented in [27]. A passive clamped circuit was used to clamp the voltage level of the main switch and recycle the energy of the leakage inductor in [27]. In [20], [21], switching capacitor techniques were recommended to achieve high step-up voltage gain. In these cases, the switch is forced to tolerate high current, which increases conduction losses. A combination of conventional boost and switch capacitor converters was presented in [22]. However, the output voltage was limited by the rating of the switching component. The switching loss in a resonant converter can be reduced by using a resonant tank [23], [28], [29]. However, using such a tank increases control complexity and the stress on the switching devices. In [30], a new structure was presented for high-voltage applications. Negative voltage gain is the main disadvantage of these types of DC/DC converters.

According to the preceding discussion, an appropriate structure that achieves high voltage gain needs to be established. In this paper, a new DC/DC converter with high voltage gain and high efficiency is presented. The paper is organized as follows. First, the operating principles of the proposed converter in continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) are presented. Second, detailed steady-state analyses of the proposed converter in CCM, DCM, and boundary-conduction mode are conducted. The voltage and current stresses on active components are also discussed. Lastly, the experimental results are presented.

II. Operating Principles of the Proposed Converter

Fig. 1 shows the circuit configuration of the proposed converter. The converter is composed of coupled inductor T_1, switch S_1, diodes, and capacitors. D_1 and D_2 are clamp diodes. C_1 and C_2 are clamp capacitors of the clamp circuit of the proposed converter. The leakage inductor energy of primary winding N_1 is stored in capacitors C_1 and C_2 through diodes D_1 and D_2. Secondary winding N_2 is connected to capacitors C_3 and C_4 through diodes D_3 and D_4, respectively. The energy of the leakage inductor of secondary winding N_2 is stored in capacitors C_3 and C_4 through diodes D_3 and D_4, respectively. Output capacitor C_5 and load R_L are connected to the mentioned part through rectifier diode D_5.

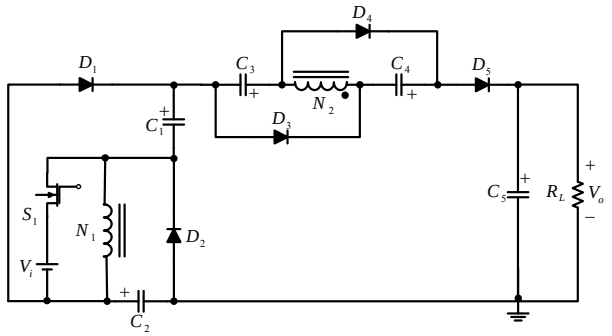


Fig. 1. Proposed converter.

The proposed converter provides high voltage gain at the output by using capacitor-charging techniques. The capacitors are charged in parallel and discharged in series to increase the output voltage. The leakage inductance of the coupled inductor can increase the voltage stress on the main switch. A passive-clamp circuit was used to eliminate this problem. The proposed structure possesses the following main features.

1) The proposed converter provides high voltage gain by using a coupled inductor and capacitor-charging techniques.
2) The energy of the leakage inductors of the coupled inductor is recycled. This feature reduces the losses and prevents a voltage spike from occurring in the main switch.
3) The voltage stress on the main switch is very low. Therefore, a low-voltage switch and low ON-state resistance (R_{DS-ON}) can be used in the converter.
4) The main switch is placed in series with the source. The switch controls the energy flow from the source to the load.
5) Voltage spikes in the main switch are prevented by using a passive-clamp circuit.

The number of components in the proposed converter is higher than that in several other converters, such as the conventional boost converter. In addition, the input current is discontinuous. The high voltage gain achieved and the relatively low voltage stress compensate for this condition.

To simplify the analysis of the proposed converter, the following assumptions are considered.

1) All components, except for the coupled inductor, are considered ideal. The ON-state resistance of the switch, the forward voltage drop of the diodes, and the ESR of the coupled inductor and capacitors are ignored.
2) The turn ratio of the coupled inductor is equal to $n = N_2 / N_1$.
3) All capacitors are sufficiently large. Therefore, the voltages across these capacitors are constant during one period.

The operating principles in CCM and DCM are presented in detail below.

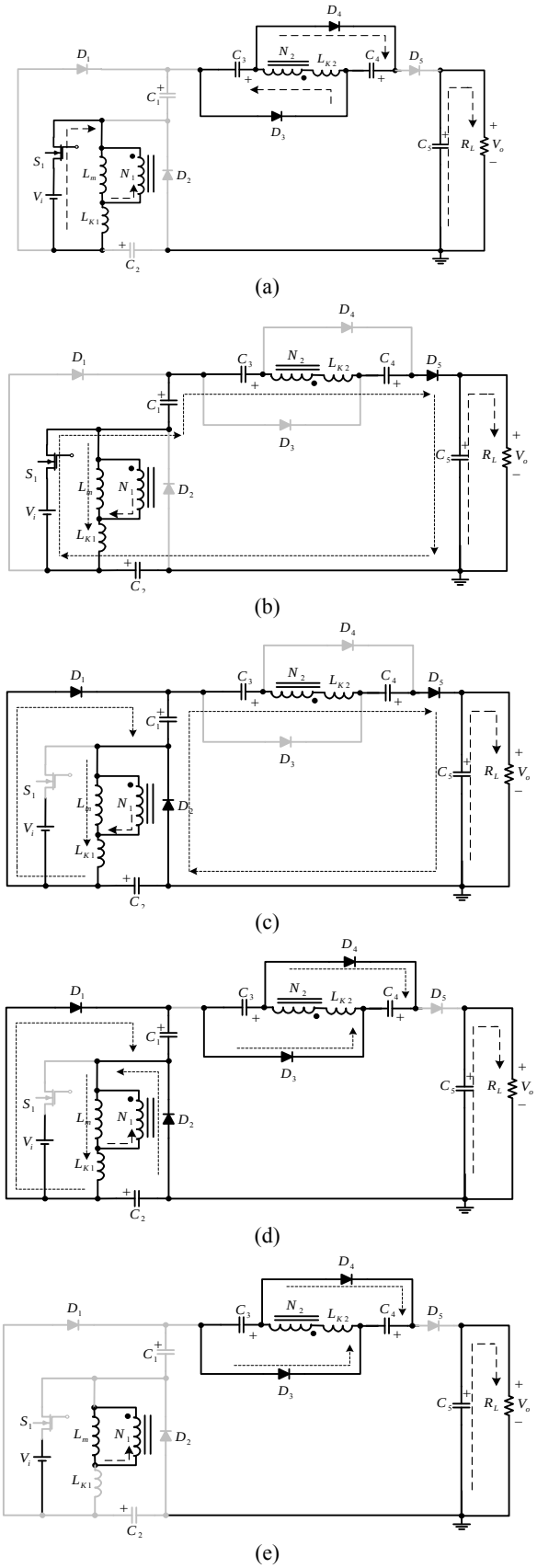


Fig. 2. Equivalent circuits of different operating modes during one switching period in CCM. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

A. CCM Operation

In CCM, the proposed converter operates in five modes. The equivalent circuits of the proposed converter in different operating modes are shown in Fig. 2. Coupled inductor T_1 is replaced by ideal primary and secondary windings (N_1, N_2), magnetizing inductor (L_m), and primary and secondary leakage inductances (L_{K1}, L_{K2}).

Mode I $(0 < t < t_1)$

Switch S_1 and diodes D_3 and D_4 are turned on, as shown in Fig. 2(a). Source V_i is across L_m and L_{K1} through S_1. Secondary leakage inductance L_{K2} continually discharges its energy into capacitors C_3 and C_4. Current i_{Lm} decreases because inductor L_m discharges its energy into the secondary winding, and the energy is reduced by charging capacitors C_3 and C_4. Therefore, currents i_{D3} and i_{D4} decrease. Current i_{LK2} also decreases according to i_{Lm}/n. The first mode ends when current i_{LK1} is equal to i_{Lm} at $t = t_1$. In this mode, the following equations apply.

$$\frac{di_{Lm}^{I}(t)}{dt} = \frac{v_{Lm}}{L_m}, \tag{1}$$

$$\frac{di_{LK1}^{I}(t)}{dt} = \frac{V_i - v_{Lm}}{L_{k1}}, \tag{2}$$

$$i_{LK2}^{I}(t) = \frac{i_{Lm}^{I}(t) - i_{LK1}^{I}(t)}{n}, \tag{3}$$

where n, v_{Lm}, i_{Lm}^{I}, i_{LK1}^{I}, and i_{LK2}^{I} are the turn ratio of coupled inductor T_1, magnetizing inductor voltage, magnetizing inductor current, and primary and secondary leakage inductor currents in mode I, respectively.

Mode II $(t_1 \le t < t_2)$

In this operating mode, switch S_1 and diode D_5 are turned on. Voltage source V_i is connected in series with capacitors C_1, C_2, $\cdots$, C_4 and secondary winding N_2 and supply output capacitor C_5 and load R_L. Magnetizing inductor L_m and primary leakage inductor L_{K1} also receive energy from source V_i. Currents i_{Lm}, i_{LK1}, and i_{D5} are increased. This mode ends when the main switch is turned off. The following equations apply in this operating mode.

$$i_{Lm}^{II}(t) = i_{LK1}^{II}(t) - n i_{LK2}^{II}(t), \tag{4}$$

$$i_{i}^{II}(t) = i_{DS}^{II}(t) = i_{Lm}^{II}(t) + (1+n) i_{LK2}^{II}(t), \tag{5}$$

$$\frac{di_{LK2}^{II}(t)}{dt} = \frac{di_{D5}^{II}}{dt} = \frac{n v_{Lm} + V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_i - V_o}{L_{K2}}, \tag{6}$$

where i_{D5}^{II}, v_{N2}, V_o, V_{C1}, V_{C2}, V_{C3}, and V_{C4} are diode D_5 current, secondary winding voltage, output voltage, and

the voltages of capacitors C_1, C_2, $\cdots$, and C_4 in the second mode, respectively.

Mode III $(t_2 \le t < t_3)$

During this period, secondary leakage inductance L_{K2} continues charging capacitor C_5 while switch S_1 is turned off. The energy stored in the primary leakage inductance flows through diodes D_1 and D_2 into capacitors C_1 and C_2, respectively. Simultaneously, L_{K2} maintains the previous mode current and is in series with capacitors C_2, C_3, and C_4 supplying output capacitor C_5 and load R_L. Currents i_{LK1} and i_{LK2} rapidly decrease because they are discharged into capacitors C_1, C_2, and C_5. However, current i_{Lm} increases because L_m receives energy from L_{K2} through T_1. This mode ends when current i_{LK2} becomes zero. For this mode, the following equations apply.

$$i_{Lm}^{III}(t) = i_{LK1}^{III}(t) - n i_{LK2}^{III}(t), \tag{7}$$

$$\frac{di_{LK1}^{III}(t)}{dt} = 2\frac{di_{D1}^{III}(t)}{dt} = \frac{-V_{C1} - v_{Lm}}{L_{K1}}, \tag{8}$$

$$\frac{di_{LK1}^{III}(t)}{dt} = 2\frac{di_{D2}^{III}(t)}{dt} = \frac{-V_{C2} - v_{Lm}}{L_{K1}}, \tag{9}$$

$$\frac{di_{LK2}^{III}(t)}{dt} = \frac{nv_{Lm} + V_{C2} + V_{C3} + V_{C4} - V_o}{L_{K2}}, \tag{10}$$

Substituting Equation (8) into Equation (9) results in

$$V_{C1} = V_{C2}. \tag{11}$$

As shown in Equation (11), capacitors C_1 and C_2 have the same voltage amplitude. Thus, their capacity should be equal.

Mode IV $(t_3 \le t < t_4)$

Diodes D_1, D_2, D_3, and D_4 are turned on during this period. The energy stored in L_m is discharged into capacitors C_1, C_2, C_3, and C_4. Currents i_{LK1}, i_{D1}, and i_{D2} decrease because L_{K1} releases its energy into capacitors C_1 and C_2 through diodes D_1 and D_2. The energy stored in capacitor C_5 is discharged into load R_L. This mode ends when inductor L_{K1} becomes completely discharged and its current i_{LK1} is zero. For this mode, the following equations are obtained.

$$\frac{di_{LK2}^{IV}(t)}{dt} = 2\frac{di_{D3}^{IV}(t)}{dt} = \frac{nv_{Lm} + V_{C3}}{L_{K2}}, \tag{12}$$

$$\frac{di_{LK2}^{IV}(t)}{dt} = 2\frac{di_{D4}^{IV}(t)}{dt} = \frac{nv_{Lm} + V_{C4}}{L_{K2}}, \tag{13}$$

Substituting Equation (12) into Equation (13) yields

$$V_{C3} = V_{C4}, \tag{14}$$

As shown in Equation (14), capacitors C_3 and C_4 have the same voltage amplitude. Thus, their capacity should be equal.

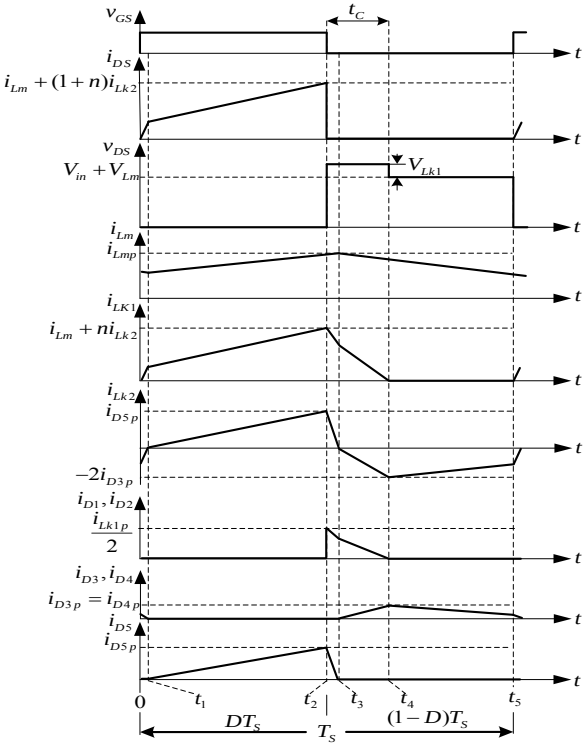


Fig. 3. Key waveforms of the proposed converter in CCM.

Mode V $(t_4 \le t < t_5)$

During this period, L_m discharges its energy into capacitors C_3 and C_4. Diodes D_3 and D_4 are turned on. Current i_{Lm} decreases because L_m discharges its energy into capacitors C_3 and C_4 through secondary winding and diodes D_3 and D_4. The energy stored in capacitor C_5 is discharged into load R_L. This mode ends when switch S_1 is turned on. The equations associated with mode V are as follows:

$$\frac{di_{Lm}^{V}(t)}{dt} = \frac{v_{Lm}}{L_m}, \tag{15}$$

$$i_{LK1}^{V} = 0, \tag{16}$$

$$\frac{di_{LK2}^{V}(t)}{dt} = 2\frac{di_{D3}^{V}(t)}{dt} = \frac{nv_{Lm} + V_{C3}}{L_{K2}}. \tag{17}$$

The proposed converter's key waveforms in one switching period based on the above equations in CCM are shown in Fig. 3. The input current ($i_i = i_{DS}$) is discontinuous because of the series connection of the main switch and the source. In several applications, such as PV source, additional filtering in the form of capacitors or several other types of LC filters is needed. This condition can increase the reliability of the converter because the energy flow from the source to the load is controlled.

B. DCM Operation

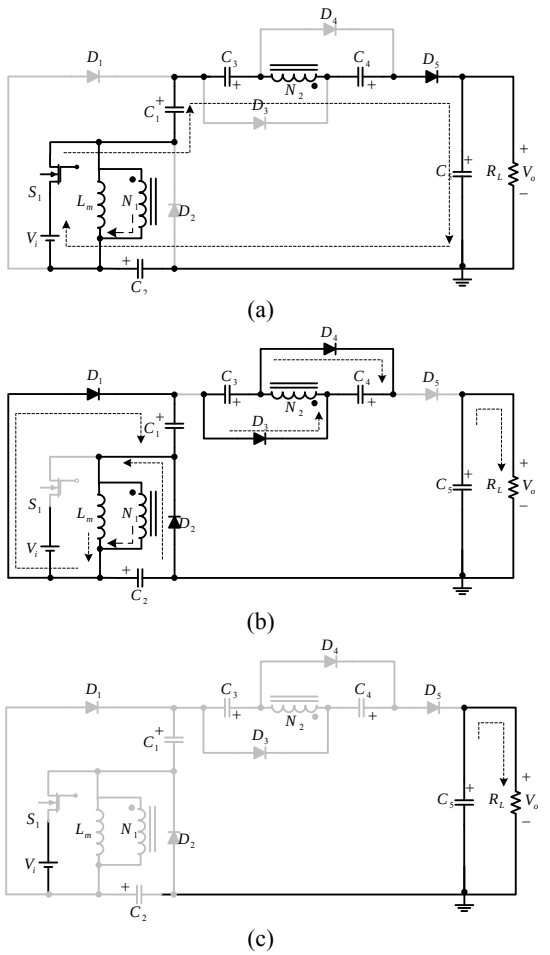


Fig. 4. Equivalent circuits of different operating modes during one switching period in DCM. (a) Mode I, (b) mode II, and (c) mode III.

In DCM, the primary and secondary inductors (L_{K1}, L_{K2}) are disregarded to simplify the analysis. Therefore, the proposed converter has three operating modes in DCM (Fig. 4).

Mode I $(0 < t < t_1)$

According to Fig. 4(a), input source V_i is in series with capacitors C_1, C_2, ⋯, C_4 and the secondary windings and feeds output capacitor C_5 and load R_L. Current i_{Lm} increases because L_m receives energy from source V_i. This mode ends when the main switch is turned off. The following equations are true for this mode.

$$i_i^I(t) = i_{Lm}^I(t) + n i_{N2}^I(t), \tag{18}$$

$$\frac{di_{Lm}^I(t)}{dt} = \frac{V_i}{L_m}, \tag{19}$$

where i_{N2}^I is the secondary winding current in mode I.

Mode II $(t_1 \le t < t_2)$

During this period, inductor L_m releases its energy into capacitors C_1, C_2, ⋯, and C_4. Thus, currents i_{D1}, i_{D2}, ⋯, and i_{D4} decrease. The energy saved in capacitor C_o is discharged into load R_L. This mode ends when current i_{Lm} becomes zero. For this mode, the following equations are true.

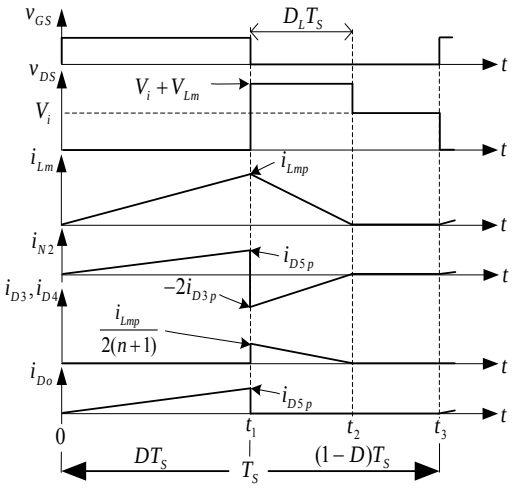


Fig. 5. Key waveforms of the proposed converter in DCM.

$$i_i^{II}(t) = i_{DS}^{II}(t) = 0, \tag{20}$$

$$\frac{di_{Lm}^{II}(t)}{dt} = 2\frac{di_{D1}^{II}(t)}{dt} = \frac{-V_{C1}}{L_m}. \tag{21}$$

Mode III $(t_2 \le t < t_3)$

During this period, switch S_1 is turned off while L_m is completely out of energy and capacitor C_5 is discharging its energy into load R_L. This mode ends when switch S_1 is turned on. For this mode, the following equations are obtained.

$$i_i^{III}(t) = i_{DS}^{III}(t) = 0 \tag{22}$$

$$i_{Lm}^{III}(t) = i_{N2}^{III}(t) = 0 \tag{23}$$

The key waveforms of the proposed converter during a switching period in DCM are shown in Fig. 5 according to Equations (18) to (23).

III. Steady State Analysis of the Proposed Converter

A. CCM Operation

During CCM operation, compared with one switching period, the time durations of modes I and III are very short and can be ignored. Thus, only modes II, IV, and V are considered. The secondary leakage inductance (L_{K2}) of the coupled inductor is transferred to its primary side. Fig. 6 shows the relationship between the clamp capacitor's charge and discharge currents under the assumption that magnetizing current i_{Lm} does not contain ripples. t_C is the fourth time duration mode, and D_C is its corresponding duty cycle by

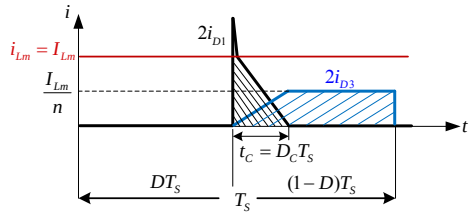


Fig. 6. Relationship of the clamp capacitor's charge and discharge currents in the proposed converter.

ignoring modes I and III. The stored energy in equivalent primary leakage inductance L_K at time interval t_C is discharged into clamp capacitors C_1 and C_2. The average values of I_{D1}, I_{D2}, ⋯, and I_{D5} are equal to the average value of I_o because average capacitor currents I_{C1}, I_{C2}, ⋯, and I_{C5} are zero in steady state. By obtaining the charging energy equal to the discharging energy, the following relationships can be established.

$$L_K = L_{K1} + n^2 L_{K2} \tag{24}$$

$$D_C = \frac{t_C}{T_S} = \frac{2(1-D)}{1+n} \tag{25}$$

The coupling coefficient of coupled inductor K is equal to $L_m/(L_m+L_K)$. The following equations are established based on Fig. 2(b).

$$v_{LK}^{II} = \frac{L_k}{L_m + L_K} V_{in} = (1-K)V_i \tag{26}$$

$$v_{Lm}^{II} = \frac{L_m}{L_m + L_k} V_i = KV_i \tag{27}$$

$$v_{N2}^{II} = n v_{Lm}^{II} = nKV_i \tag{28}$$

$$V_o = V_i + V_{C1} + V_{C2} + V_{C3} + V_{C4} + v_{N2} \tag{29}$$

By using Equations (24) to (29) and considering the voltage second balance principle of inductance, voltages $v^{IV}{}_{LK}$, $v^{IV}{}_{Lm}$, and $v^{IV}{}_{N2}$ can be derived as follows:

$$V_{LK}^{IV} = \frac{-D(1+n)(1-K)}{2(1-D)} V_i, \tag{30}$$

$$V_{Lm}^{IV} = \frac{-DK}{(1-D)} V_i, \tag{31}$$

$$V_{N2}^{IV} = \frac{-nDK}{(1-D)} V_i. \tag{32}$$

Capacitors C_1, C_2, C_3, and C_4 are charged in mode IV. Considering Equations (30) to (32), the voltages across capacitors C_1, C_2, C_3, and C_4 are obtained as follows:

$$V_{C1}^{IV} = V_{C2}^{IV} = -V_{Lm}^{IV} - V_{LK}^{IV} = \frac{D}{2}\left[\frac{(1+K)+n(1-K)}{(1-D)}\right] V_i, \tag{33}$$

$$V_{C3}^{IV} = V_{C4}^{IV} = -V_{N2}^{IV} = \frac{nDK}{(1-D)} V_i. \tag{34}$$

By substituting Equations (28), (33), and (34) into Equation (29), the voltage gain is obtained as follows:

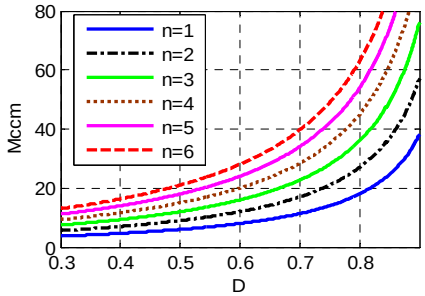


Fig. 7. Voltage gain (M_{CCM}) as a function of duty ratio (D) considering various turn ratios.

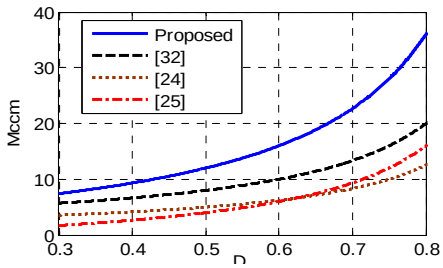


Fig. 8. Voltage gain (M_{CCM}) versus duty cycle (D) of the proposed converter compared with that of the presented converters in [24], [25], and [32] in CCM operation under $n=3$ and $K=1$.

$$M_{CCM} = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{1+DK+nD+nK}{(1-D)}. \tag{35}$$

At $K=1$, the ideal voltage gain can be written as

$$M_{CCM} = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{(1+n)(1+D)}{1-D}. \tag{36}$$

Fig. 7 shows the variation in voltage gain M_{CCM} as a function of duty cycle D and various turn ratios. In Fig. 8, the variation in voltage gain (M_{CCM}) versus duty cycle D of the proposed converter is compared with that of the converters presented in [24], [25], and [32] in CCM operation under $n=3$ and $K=1$. The proposed converter has the highest voltage gain among the compared converters, and this value is much larger than the other voltage gain values for all duty cycles.

B. DCM Operation

On the basis of Fig. 4(a), the following equations are established.

$$v_{N2}^{I} = nV_i \tag{37}$$

$$V_o = V_i + V_{C1} + V_{C2} + V_{C3} + V_{C4} + v_{NS}^{I} \tag{38}$$

The peak magnetizing inductor current (i_{Lmp}) is given as

$$i_{Lmp} = \frac{DT_S}{L_m} V_i. \tag{39}$$

The following equations are derived from Fig. 4(b).

$$v_{Lm}^{II} = -V_{C1} = -V_{C2} \tag{40}$$

$$v_{NS}^{II} = -V_{C3} = -V_{C4} \tag{41}$$

The following equation is based on Fig. 4(c).

$$v_{Lm}^{III} = v_{N2}^{III} = 0 \tag{42}$$

By applying the voltage second balance principle of inductance and by using Equations (37) to (42), the voltages across capacitors C_1, C_2, $\cdots$, and C_4 are achieved as follows:

$$V_{C1} = V_{C2} = \frac{D}{D_L} V_i, \tag{43}$$

$$V_{C3} = V_{C4} = n\frac{D}{D_L} V_i. \tag{44}$$

By substituting Equations (37), (43), and (44) into Equation (38), the output voltage equation is obtained as follows:

$$V_o = \frac{(1+n)(D_L+2D)}{D_L} V_i. \tag{45}$$

From Equation (45), the equation of D_L is derived as

$$D_L = \frac{2D(1+n)V_i}{V_o - (1+n)V_i}. \tag{46}$$

In addition, the following relationship is derived between output voltages and currents.

$$V_o = R_L I_o \tag{47}$$

The average values of the currents of diodes D_3 and D_4 are given by

$$I_{D3} = I_{D4} = \frac{I_{Lm} - 2I_{D3}}{2n}. \tag{48}$$

By using Equation (48) and knowing that the average current values of diodes are equal to the average value of I_o, the peak current of diodes D_3 and D_4 in DCM can be obtained as follows:

$$i_{D3p} = i_{D4p} = \frac{i_{Lmp}}{2(n+1)}. \tag{49}$$

On the basis of Equation (49) and Fig. 5, the following equation is derived.

$$\frac{1}{2} D_L \frac{i_{Lmp}}{2(n+1)} = I_o \tag{50}$$

Substituting Equations (39), (45), and (47) into Equation (50) yields

$$\frac{D^2 V_i^2 T_S}{2L_m \left[V_o - (1+n)V_i\right]} = \frac{V_o}{R_L}. \tag{51}$$

The normalized time constant of the magnetizing inductor (τ_{Lm}) is given by

$$\tau_{Lm} = \frac{L_m}{R_L T_s}. \tag{52}$$

By substituting Equation (52) into Equation (51), the output voltage gain in DCM (M_{DCM}) is obtained as follows:

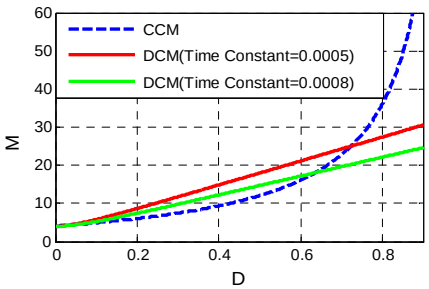


Fig. 9. DCM voltage gain curve versus duty cycle at different time constants under $n = 3$.

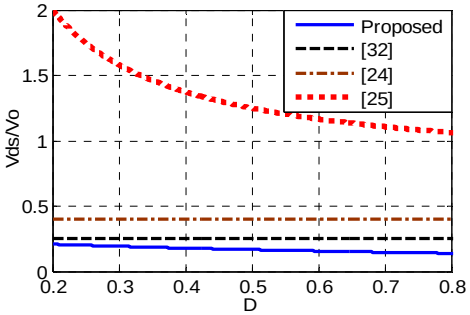


Fig. 10. Comparison of voltage stress on the main switch of the proposed converter with that for the presented converters in [24], [25], and [32] in CCM operation under $n = 3$.

$$M_{DCM} = \frac{V_o}{V_i} = \frac{n+1}{2} + \sqrt{\left(\frac{n+1}{2}\right)^2 + \frac{D^2}{2\tau_{Lm}}}. \tag{53}$$

The curve of DCM voltage gain versus duty cycle at different time constants under $n = 3$ is shown in Fig. 9.

C. Calculation of Voltage Stress on Active Devices

The stresses on the active devices, such as switches and diodes, were calculated. The leakage inductances of the primary and secondary sides were ignored, and $K = 1$ was considered. In CCM, the voltage stress on switch S_1 and diodes D_1, D_2, $\cdots$ and D_5 is obtained as follows:

$$V_{DS} = V_{D1} = V_{D2} = \frac{V_i}{1-D} = \frac{V_o}{(1+n)(1+D)}, \tag{54}$$

$$V_{D3} = V_{D4} = \frac{nV_i}{1-D} = \frac{nV_o}{(1+n)(1+D)}, \tag{55}$$

$$V_{D5} = V_o - V_{C1} - V_{C3} = \frac{V_o}{1+D}. \tag{56}$$

Fig. 10 shows a comparison of the voltage stress on the main switch of the proposed converter and that for the presented converters in [24], [25], and [32] in CCM operation under $n = 3$. Evidently, the proposed converter has the least voltage in all duty cycles.

IV. Experimental Results

A. Proposed Structure Design Considerations

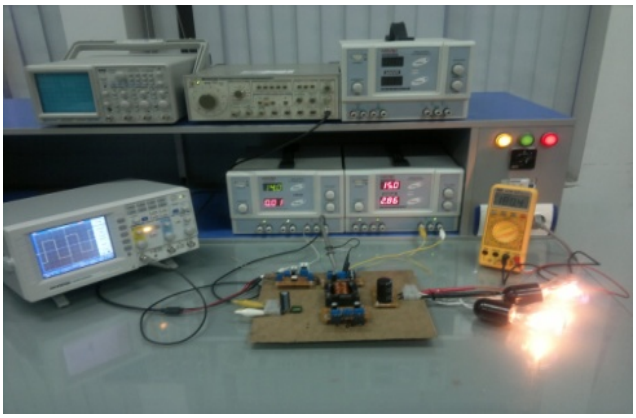


Fig. 11. Experimental prototype of the proposed converter.

Several voltage and current waveforms of the proposed converter were established to confirm the correctness of the proposed structure. The specifications of the built prototype shown in Fig. 11 are summarized in Table I.

In the experimental setup, a signal generator was used to produce the switching pulse for the main switch. IC TPL 250 was utilized to derive the switch, and an adjustable DC source was used as the input voltage source.

Electrolytic capacitors in power electronics are often eliminated because they possess relatively low reliability and a short lifetime. The capacitances of C_1, C_2, $\cdots$ and C_4 used in the proposed converter do not need to be high because the switching frequency of the proposed converter is quite high (25 kHz). Thus, film capacitors, which are used in light-emitting diode drivers, can be used in the proposed converter.

The experimental and calculated waveforms of the proposed converter, such as the input current, primary and secondary leakage inductor currents, and D_1 and D_2 currents, are shown in Fig. 12.

The experimental figures shown in Fig. 12(a) reveal the validity of the steady state analyses shown in Fig. 12(b). All experimental current waveforms were measured by measuring the voltage across the resistance of 0.1 Ω. The calculated and measured waveforms are shown in one figure to validate properly the operational waveform equations derived. The amplitudes of the waveforms shown in Fig. 12(b) were calculated by using the specifications presented in Table I and Equations (1) to (17). The experimental current waveform of the secondary winding of the coupled inductor is shown in Fig. 12(a). As illustrated previously, the positive half cycle waveform constitutes the current waveform of diode D_5, and the negative half cycle waveform constitutes the current waveforms of diodes D_3 and D_4. The current waveforms of the primary leakage inductor and diodes D_1 and D_2 are shown in Fig. 12(a). The peak value of the currents of diodes D_1 and D_2 is equal to half of the peak value of the primary leakage inductor current, which proves the accuracy of Equations (11) and (12). Waveforms i_{LK1}, i_{D1}, and i_{D2} show that the energy of primary leakage inductance (L_{K1}) is discharged into capacitors C_1 and C_2 through diodes D_1 and D_2.

TABLE I

SPECIFICATIONS OF THE PROTOTYPE OF THE PROPOSED CONVERTER

Symbol	Quantity	Magnitude (Unit)
f_S	switching frequency	$25kHz$
D	duty cycle	50%
V_i	input voltage	$15V$
V_o	output voltage	$180V$
P_o	output power	$40W$
L_m	magnetizing inductor	$0.5mH$
L_K	leakage inductor	$1.68\mu H$
C_1, C_2	clamp circuit capacitors	$47\mu F$
C_3, C_4	parallel charged capacitors	$22\mu F$
C_5	output capacitors	$220\mu F$
n	turn ratio	3

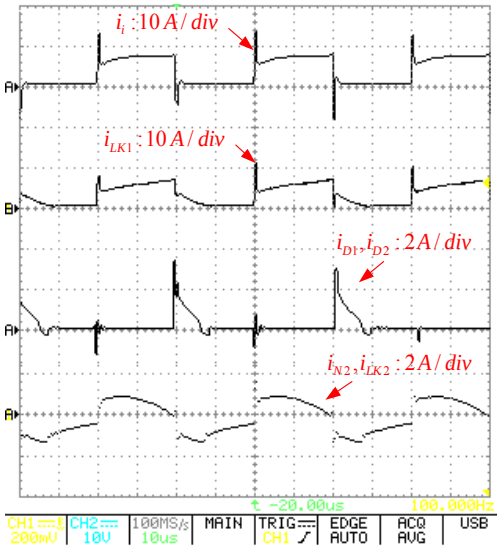
The experimental and calculated voltage waveforms of the switch and diodes as well as the input and output voltage waveforms are shown in Fig. 13. According to the waveform of V_{DS} shown in Fig. 13(a), the voltage stress on switch S_1 is clamped. The accuracy of Equation (54) is verified by $V_{DS} = 30V$. To reduce losses in the proposed converter, a switch with a low voltage rate and low ON-state resistance can be used.

The waveforms of diodes D_3, D_4, and D_5 shown in Fig. 15(a) confirm the accuracy of Equations (55) and (56). As shown in Fig. 13(a), the amplitude of input and output voltages are approximately 15 and 180 V, respectively. A high voltage gain $(M_{CCM} = 12)$ is achieved by the proposed converter.

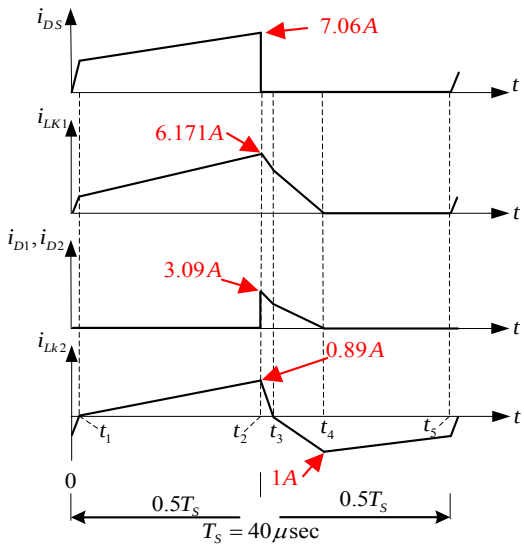
Different means, such as reducing the switching frequency and duty cycle, can be applied to make the converter operate in DCM mode.

The experimental voltage waveforms of the switch and primary winding in DCM are shown in Fig. 14. The duty cycle was reduced for the proposed converter to operate in DCM. In addition, the coupled inductor is out of energy in approximately two-thirds of a cycle. Thus, its voltage is zero.

The difference between the experimental efficiencies of the proposed converter and the converters presented in [32], [24], [33], and [34] for different output powers is shown in Fig. 15. The proposed converter operates at nominal power with an efficiency of about 94.2%.

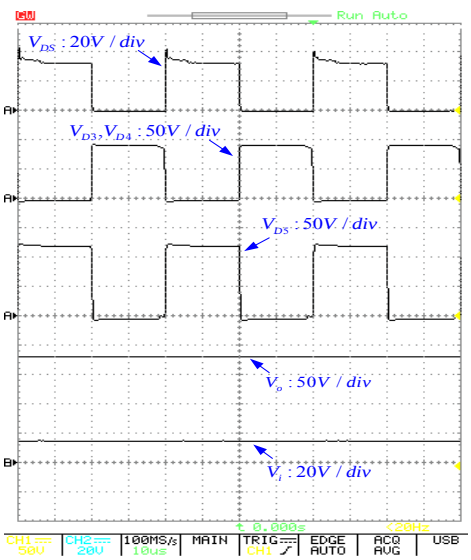


(a)

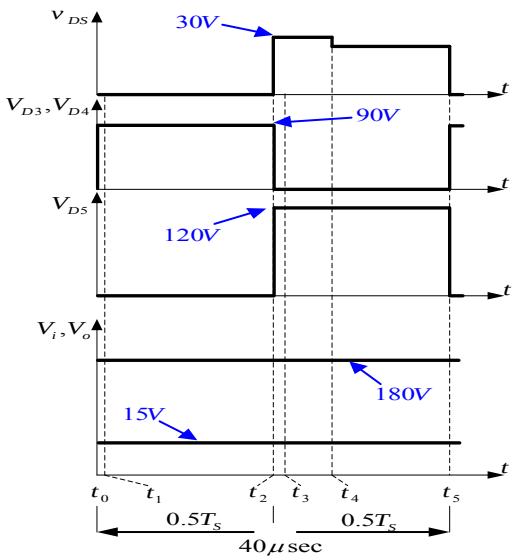


(b)

Fig. 12. Proposed converter's output current waveforms for $V_i = 15$, $D = 0.5$, $n = 3$ in CCM. (a) Experimental results (time/div: 10μ sec/ div) and (b) typical waveforms.



(a)



(b)

Fig. 13. Voltage waveforms of the proposed converter for $V_i = 15$, $D = 0.5$, $n = 3$ in CCM. (a) Experimental results (time/div: 10μ sec/ div) and (b) typical waveforms.

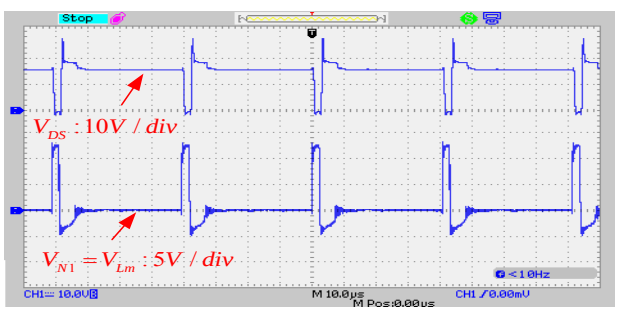


Fig. 14. Experimental voltage waveforms of the proposed converter for $V_i = 15$, $D = 0.05$, $n = 3$ in DCM (time/div: 10μ sec/ div).

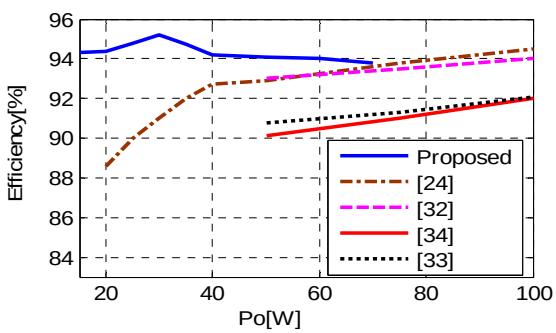


Fig. 15. Measured efficiency of the proposed converter compared with that of converters presented in [32], [24], [33], and [34].

VI. CONCLUSIONS

A novel structure of a DC/DC boost converter with high step-up gain was proposed. Compared with converters presented in other studies, the proposed structure achieved a higher voltage gain with low duty cycles by using capacitor-charging techniques. The proposed converter uses a clamp circuit to reduce the voltage stress on the main switch. Thus, a switch with low ON-state resistance can be used. In addition, the leakage inductance energy recycling in the proposed structure reduces losses. Given the series connection of the main switch to the source, the energy flowing from the source to the load is easily controlled. The experimental results were presented with $V_i = 15$, $D = 0.5$, and $n = 3$ to confirm the accuracy of the analyses. The proposed converter's efficiency at nominal power is about 94.2%.

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