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무변압기형 태양광 시스템에서 누설전류를 제거하기 위한 3레벨 인버터의 단순 SVPWM

A Simplified SVPWM for Three Level Inverters to Eliminate Leakage Currents in Transformeless Photovoltaic Systems

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(Arsalan Ansari · Hee-Jun Kim)

Abstract - This paper proposes a simplified SVPWM for three level inverters in transformerless photovoltaic (PV) systems. With the proposed SVPWM the three level space vector (SV) diagram is divided into only six sectors as in conventional two level SV diagram in such a way that only seven SVs are used among all the available SVs of three level inverter. The main features of the proposed SVPWM are that it is simple to implement, less switching losses as compared to conventional SVPWM and most importantly it eliminates the leakage currents in transformerless PV systems. Detailed theoretical analysis of the proposed SVPWM are presented and verified by numerical simulations and experimental results.

Key Words : SVPWM, Three level inverter, Leakage currents, Transformerless PV systems.

1. Introduction

The renewable energies such as PV modules, fuel cells and wind turbines are of particular interest due to their tremendous advantages over conventional sources of energy. The PV systems are particularly more attractive due to their relative small size, noiseless operation, simple installation and the possibility to install them closer to the user[1]. However, the output voltages of PV modules have a low dc amplitude value. In order to connect to the grid the multistage conversion systems (dc-dc converter & inverter) employing a high frequency transformer are used. The multistage conversion systems decrease the efficiency of the system and transformer makes it complicated[2]. For these reasons the transformerless grid-connected PV inverters are manifested to offer the benefits of lower cost, higher efficiency, smaller size, and weight. However, a galvanic connection exists between the power grid and the PV module due to the exclusion of the transformer. The main disadvantage of transformerless PV inverter system is that a common mode (CM) voltage variation between the PV panels and ground inject an additional leakage current[2, 3] and results in harmonics and losses in the PV system, electromagnetic interference and even electrical safety problems[4].

The mitigation of the leakage currents can be achieved by the modification of the inverter topology and also by modulation methods[5-8]. The modulation methods are most widely used because there is no need of topological modification or extra hardware. In most cases SVPWM methods are used to solve leakage current problems, because three level inverter has an inherent capability to produce the constant CM voltage by using particular SVs and thereby eliminating the leakage currents in the system. A SVPWM approach is proposed in[9] to solve the problem of leakage current and neutral point voltage variations simultaneously. However the leakage currents have some higher values due to the fact that the SVs used in any switching period do not maintain the constant CM voltage. In[10] different SVPWM techniques are presented to eliminate leakage currents in transformerless PV systems. The proposed techniques however, maintains the constant CM voltage to eliminate leakage currents but the detailed implementation steps are not provided for these modulation techniques. In this paper a simplified SVPWM is proposed to solve the problem of leakage currents in transformerless grid-connected PV inverter systems. The proposed SVPWM

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is simplified in such a way that it only uses seven SVs (six medium and a zero SV) among a total of twenty seven SVs available for three level inverter.

This paper is structured as follows. Next section describe briefly the three level inverter and conventional SVPWM. Section 3 provides detailed theoretical analysis of the proposed method. Section 4 analyses some important features of the proposed SVPWM. Simulations are provided in section 5 and section 6 concludes the paper.

2. Three level Inverter and Conventional SVPWM

A three phase three level transformerless grid-connected inverter is shown in Fig. 1. In grid-connected transformerless PV system, there exist a conduction path between PV panel and grid ground through C_{pv} and R_g. The C_{pv} and R_g represents the PV array stray capacitance and resistance from PV panel to ground respectively in Fig. 1.

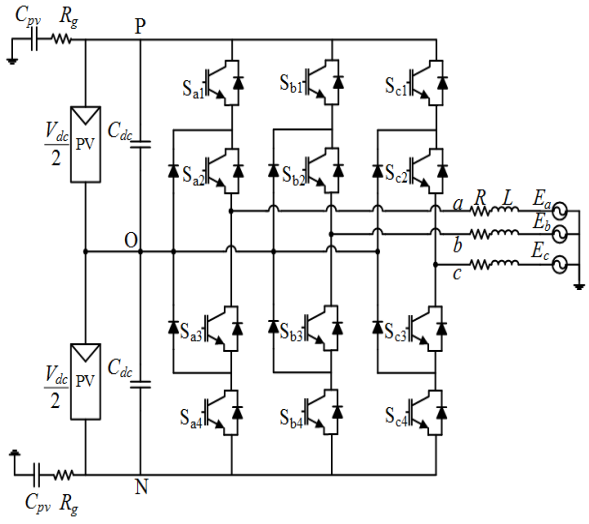


Fig. 1 Transformerless grid-connected PV system

In three phase three level inverter, each inverter leg can be connected to three output states P ($\frac{V_{dc}}{2}$), O (0) or N ($-\frac{V_{dc}}{2}$), by particularly switching on or off the appropriate switches of the inverter leg as given by Table 1. Where S_{xi} (x=(a,b,c) and i=1~4) represents the switches of the three level inverter. A total of 3^3=27 output sates can be achieved from a three phase three level inverter. Each state corresponds to a voltage vector or switching state vector in the SV diagram of the three level inverter as shown in Fig.

Table 1 Switching state definition

Switching State	Switching device status				Output Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P	On	On	Off	Off	$\frac{V_{dc}}{2}$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-\frac{V_{dc}}{2}$

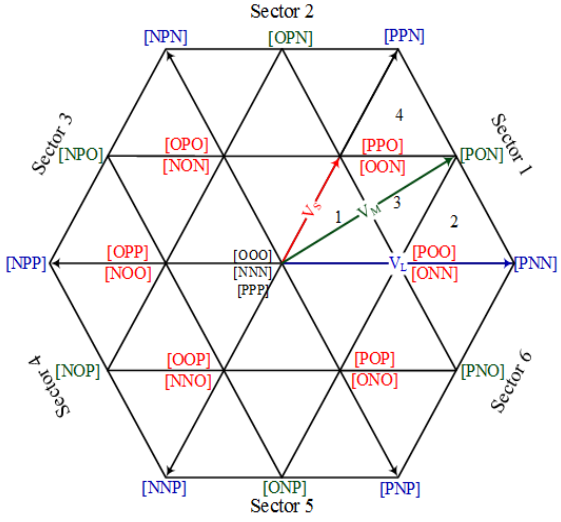


Fig. 2 SV diagram of conventional three level SVPWM

2. The SV diagram of three level inverter can be divided into six sectors, further each sector can be divided into four small triangular regions. Depending upon the location of reference voltage vector, the SVPWM works on the principle of synthesizing reference voltage vector by adjacent three voltage vectors. The implementation process of the conventional SVPWM involves the following steps.

1. Sector determination according to the location of the reference voltage vector.
2. Small triangular regions identification.
3. Selection of voltage vector depending upon the sector number and the triangular region.
4. Dwell time calculation for the selected voltage vectors.
5. Finally, designing the switching sequence.

Since SV diagram of a three level inverter is divided into six sectors and four small triangular regions, there is a complexity in identifying the small triangular regions and in the calculation of duty cycles for each switching state. In the proposed method the three level inverter SV diagram is

simplified to a two level SV diagram so that the computational burden is reduced.

3. Proposed Method

In the proposed simplified SVPWM for three level inverters the hexagon is formed by joining the vertices of the medium voltage vectors as shown in Fig. 3. The implementation of the proposed method then follows the same steps as mentioned for the conventional SVPWM (except 2).

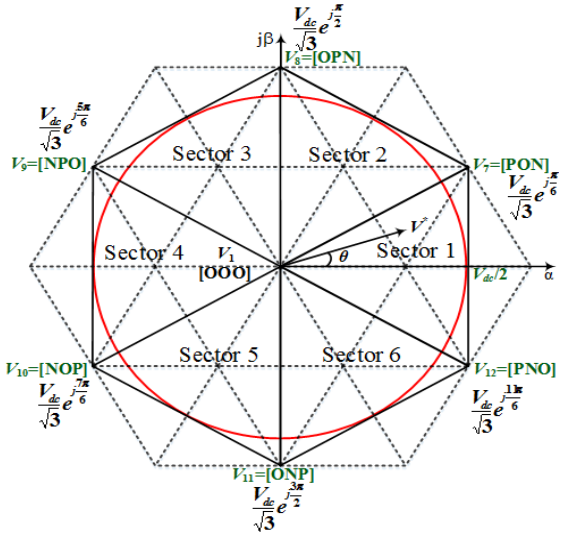


Fig. 3 SV diagram of proposed SVPWM division of sectors

3.1 Determination of sectors

According to the location of the reference voltage vector V^*, the sectors are determined as

Sector 1: If $-\frac{\pi}{6} \le \theta < \frac{\pi}{6}$

Sector 2: If $\frac{\pi}{6} \le \theta < \frac{\pi}{2}$

Sector 3: If $\frac{\pi}{2} \le \theta < \frac{5\pi}{6}$

Sector 4: If $\frac{5\pi}{6} \le \theta < \frac{7\pi}{6}$

Sector 5: If $\frac{7\pi}{6} \le \theta < \frac{3\pi}{6}$

Sector 6: If $\frac{3\pi}{2} \le \theta < \frac{11\pi}{6}$

where θ is the angle between the reference voltage vector V^* and α-axis of the SV diagram as shown in Fig. 3. The SV diagram of the proposed method is just same as that of two level inverter except that each sector is shifted by 30°.

3.2 Dwell times calculation

To calculate the switch on times, the volt-sec balance principle is used, that is the product of the reference voltage V^* and sampling time T_s equals the sum of the voltage multiplied by the time interval of chosen SVs. For example if the reference voltage vector falls into the first sector of Fig. 3, the vectors V_1, V_7 and V_{12} can be used to synthesize V^* as shown in Fig. 4. The volt-sec balance principle is given as

$$V^*.T_s = V_1 T_1 + V_{12} T_{12} + V_7 T_7 \tag{1}$$

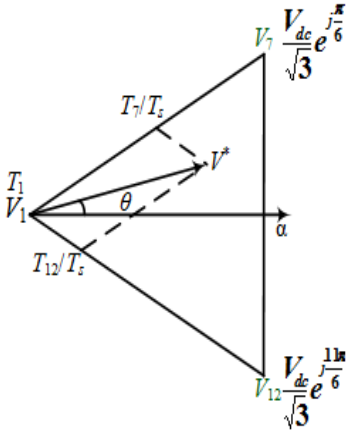


Fig. 4 Dwell times calculations

The magnitude of zero vector V_1 is zero and the magnitude of all medium vectors is $\frac{V_{dc}}{\sqrt{3}}$. The angle of the corresponding medium vectors V_{12} and V_7 in sector 1 is $\frac{-\pi}{6}$ and $\frac{\pi}{6}$ respectively, as shown in Fig. 4. Then (1) can be written in polar form and is given as

By solving (2) and separating the real and imaginary parts one can get

$$|V^*|e^{j\theta}.T_s = 0T_1 + \frac{1}{\sqrt{3}} V_{dc} e^{j\frac{11\pi}{6}} T_{12} + \frac{1}{\sqrt{3}} V_{dc} e^{j\frac{\pi}{6}} T_7 \tag{2}$$

$$|V^*|.T_s.\cos\theta = \frac{V_{dc}}{2} T_{12} + \frac{V_{dc}}{2} T_7 \tag{3}$$

$$|V^*|.T_s.\sin\theta = -\frac{V_{dc}}{2\sqrt{3}} T_{12} + \frac{V_{dc}}{2\sqrt{3}} T_7 \tag{4}$$

Also the sampling time T_s should be equal to

$$T_s = T_1 + T_{12} + T_7 \quad (5)$$

By solving equations (3), (4) and (5) simultaneously T_7 and T_{12} can be obtained as

$$T_7 = \frac{|V^*|.T_s}{V_{dc}}(\sqrt{3}\sin\theta + \cos\theta) \quad (6)$$

$$T_{12} = \frac{|V^*|.T_s}{V_{dc}}(\cos\theta - \sqrt{3}\sin\theta) \quad (7)$$

where $-\frac{\pi}{6} \le \theta < \frac{\pi}{6}$ and $m_i = 2 \times \frac{|V^*|}{V_{dc}}$ is the modulation index. Equations 6 and 7 illustrate the time of application of voltage vectors V_7 and V_{12}, respectively in sector 1. Let's suppose the reference voltage vector lies on the vertex of V_{12} in sector 1, then the angle (θ) with respect to α-axis is $-\frac{\pi}{6}$, putting $\theta = -\frac{\pi}{6}$ in (6), T_7 becomes equal to zero that means at this particular instant only T_{12} is used to synthesize the reference voltage vector. As reference voltage vector (V^*) rotates towards the voltage vector V_7, the time T_{12} starts decreasing and time T_7 starts increasing from its zero value.

The switch on times for other sector can be determined similarly by the principle of volt-sec balance principle and are given in Table 2.

Table 2 Dwell times in all sectors

Sector	Switching times	θ
1	$T_7 = \frac{m_i}{2}.T_s(\sqrt{3}\sin\theta + \cos\theta)$ $T_{12} = \frac{m_i}{2}.T_s(\cos\theta - \sqrt{3}\sin\theta)$ $T_1 = T_s - T_{12} - T_7$	$-\frac{\pi}{6} \le \theta < \frac{\pi}{6}$
2	$T_7 = m_i.T_s\cos\theta$ $T_8 = \frac{m_i}{2}.T_s(\sqrt{3}\sin\theta - \cos\theta)$ $T_1 = T_s - T_8 - T_7$	$\frac{\pi}{6} \le \theta < \frac{\pi}{2}$
3	$T_8 = \frac{m_i}{2}.T_s(\sqrt{3}\sin\theta + \cos\theta)$ $T_9 = -m_i.T_s\cos\theta$ $T_1 = T_s - T_8 - T_9$	$\frac{\pi}{2} \le \theta < \frac{5\pi}{6}$
4	$T_9 = \frac{m_i}{2}.T_s(\sqrt{3}\sin\theta - \cos\theta)$ $T_{10} = -m_i.T_s(\sqrt{3}\sin\theta + \cos\theta)$ $T_1 = T_s - T_9 - T_{10}$	$\frac{5\pi}{6} \le \theta < \frac{7\pi}{6}$
5	$T_{10} = -m_i.T_s\cos\theta$ $T_{11} = \frac{m_i}{2}.T_s(\cos\theta - \sqrt{3}\sin\theta)$ $T_1 = T_s - T_{10} - T_{11}$	$\frac{7\pi}{6} \le \theta < \frac{3\pi}{6}$
6	$T_{11} = -m_i.T_s(\sqrt{3}\sin\theta + \cos\theta)$ $T_{12} = 2.m_i.T_s\cos\theta$ $T_1 = T_s - T_{11} - T_{12}$	$\frac{3\pi}{2} \le \theta < \frac{11\pi}{6}$

3.3 Switching Sequence Design

With the voltage vectors selected and the dwell times calculated the next step is to arrange switching sequence. If the reference voltage vector is in sector 1 as shown in Fig. 3, the voltage vector V_1, V_7, V_{12} are selected with their respective dwell times T_1, T_7, T_{12} to synthesize the reference voltage vector V^*. Then the switching sequence is shown in Fig. 5. The zero vector V_1 [OOO] is applied at the start and at the end with dwell time $T_1/2$ at both ends. In the middle the medium voltage vectors V_7 [PON] and V_{12} [PNO] are applied for total dwell time of T_7 and T_{12} respectively. From Fig. 5 it can be realized that the transition from one switching state to another switching state requires inverter's any two legs to change their state. This may cause the implementation difficulties however; this problem may be solved by properly controlling the commutation of the inverter.

The switching sequence for other sectors is obtained similarly and is tabulated in Table 3.

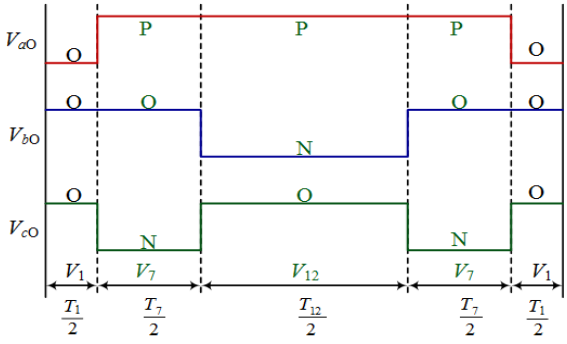


Fig. 5 Switching sequence and dwell times in sector 1

Table 3 Switching sequence in all sectors

Sectors	Switching Sequence
1	V_1,V_7,V_{12},V_7,V_1
2	V_1,V_8,V_7,V_8,V_1
3	V_1,V_9,V_8,V_9,V_1
4	$V_1,V_{10},V_9,V_{10},V_1$
5	$V_1,V_{11},V_{10},V_{11},V_1$
6	$V_1,V_{12},V_{11},V_{12},V_1$

4. Characteristics of Proposed SVPWM

Some of the main features of the proposed SVPWM are discussed in this section.

4.1 Voltage Gain

Fig. 3 also illustrates the maximum output voltage of the proposed SVPWM in the linear range of modulation. The peak value of the output voltage is given as

$$V_P = \frac{V_{dc}}{2} \tag{8}$$

It should be noted that since the large voltage vectors are not employed in the proposed SVPWM, the maximum modulation index in the linear modulation range is given by (9) which is

$$m_{i(\max)} = 2 \times \frac{|V^*|}{V_{dc}} = 1 \tag{9}$$

which is 86.67% of the modulation index of conventional SVPWM in the linear modulation range. The linear modulation range of the proposed SVPWM is less than the conventional SVPWM however, the proposed SVPWM eliminates the leakage currents and its unavoidable effects in grid connected inverter systems.

4.2 The Switching frequency

The number of commutation per a sampling period of the proposed SVPWM are eight and can be carefully observed by looking at Fig. 5 and Table. 1. Since there are 12 switches in three level inverter the effective switching frequency can be calculated as

$$f_{sw} = \frac{8/T_s}{12} = \frac{2}{3} f_{samp} \tag{9}$$

where f_{samp} is the sampling frequency. It is obvious from (9), that the switching frequency and therefore the switching losses with the proposed SVPWM are reduced by 1/3rd to the conventional SVPWM.

4.3 Constant common mode voltage

As shown in Fig. 5, the proposed SVPWM only employs medium voltage vectors and only zero vector [OOO]. All these voltage vector keep the common mode voltage constant and thus the proposed SVPWM is helpful in mitigation of leakage currents in the transformerless PV systems.

5. Simulations

To verify the effectiveness of the proposed method for three phase three level transformerless grid-connected PV inverter system shown in Fig. 1, simulations are carried out with the circuit parameters as shown in Table 4. The inverter control parameters are: modulation index m_i=0.86, Inverter angle: 10^o. The simulation results are shown in the following figures. Fig. 6 to Fig. 8 shows the simulation results when conventional SVPWM is used, and figures from Fig. 9 to Fig. 11 are the simulation results for the proposed SVPWM.

Table 4 Simulation Parameters

Parameters	Values
V_{dc}	800 V
L	400 μH
R	0.1 Ω
E_{ab}	380 V rms
C_{pv}	10 nF
R_g	5 Ω
C_{dc}	1100 μF
T_s	100 μsec

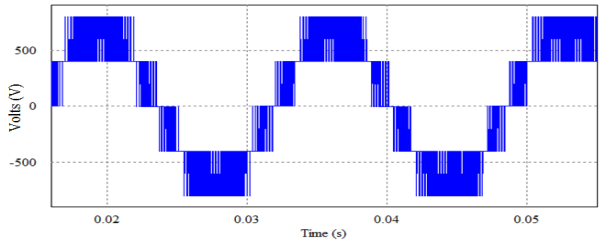


Fig. 6 Line-to-line voltage when conventional SVPWM is used

Fig. 6 shows the line to line voltage V_{ab} when the conventional SVPWM is used. It should be noted that in the first quarter V_{ab} first varies between 0 and V_{dc}/2, and then between V_{dc}/2 and V_{dc}.

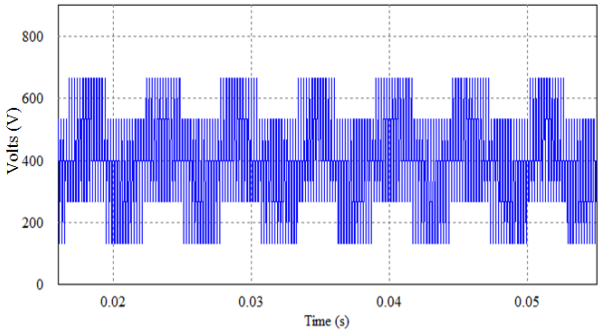
Fig. 7 shows the common mode voltage when the conventional SVPWM is used. Fig. 7(a) clearly depicts that the common mode voltage is not constant for conventional

SVPWM. Fig. 7(b) shows the zoom-in-view of common mode voltage with conventional SVPWM. It can be observed that the common mode voltage varies from its minimum $V_{dc}/6$ to maximum $5V_{dc}/6$ in steps of $V_{dc}/6$. These variations in the common mode voltages result in higher leakage currents when using conventional SVPWM.

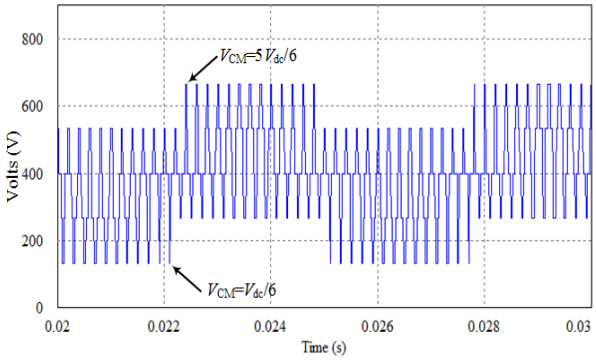
Fig. 8 shows the leakage current when the conventional SVPWM is used. The peak value of the leakage current can be seen as 580 mA with the conventional SVPWM which is unavoidable in PV systems and may cause harmonics, losses and electromagnetic interference problems.

Fig. 9 shows the three phase currents of the system, when the proposed SVPWM is applied. One can see that the peak value of the phase current is 461 A.

Fig. 10 shows the output voltages of three level inverter such as pole voltage V_{aO} and line-to-line voltage. Fig. 10(a) depicts the pole voltage V_{aO} while Fig. 10(b) describes the line-to-line voltage V_{ab}. The line-to-line voltages obtained



(a) V_{CM}



(b) Zoom-in-view of V_{CM}

Fig. 7 Common mode voltage VCM when conventional SVPWM is used

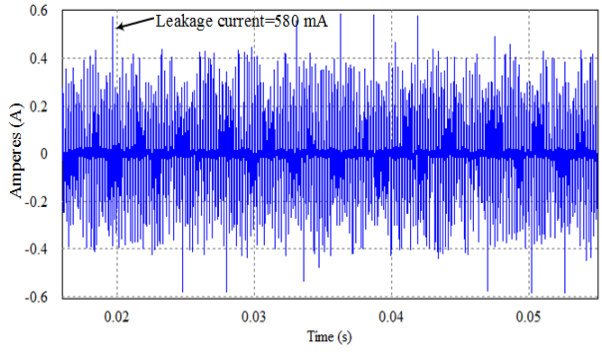


Fig. 8 Leakage current when conventional SVPWM is used

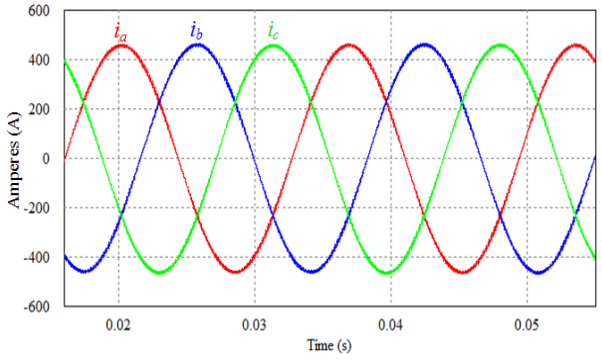
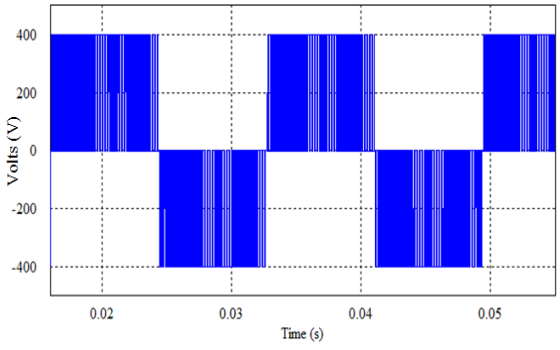
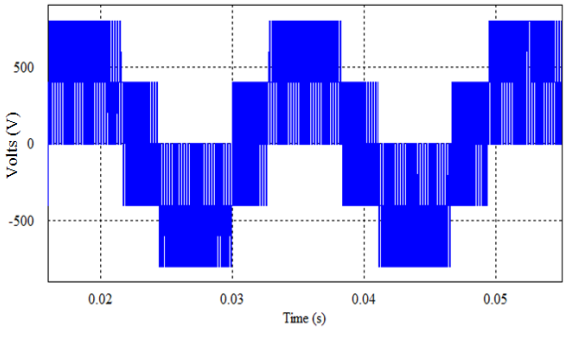


Fig. 9 Three phase output currents when proposed SVPWM is used



(a) Pole voltage V_{aO}



(b) Line-to-line voltage V_{ab}

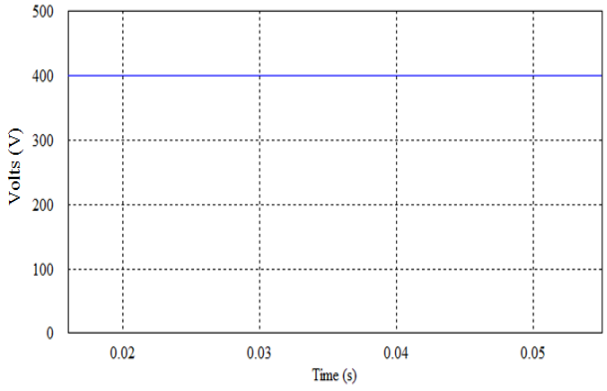
Fig. 10 Outputs of three level inverter when proposed SVPWM is applied

from the proposed SVPWM consists of five voltage levels same as in conventional SVPWM, however with the proposed SVPWM the line-to-line voltages always vary from zero voltage level to other voltage levels that is not the case for conventional SVPWM as shown in Fig. 6.

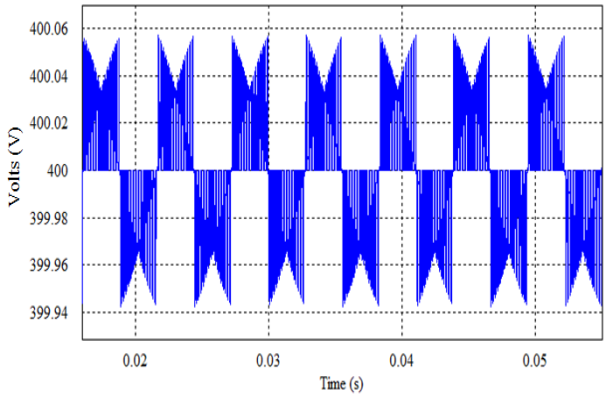
Fig. 11(a) shows the common mode voltage V_{CM} and Fig. 11(b) shows the zoom-in view of V_{CM} with the proposed SVPWM applied to the inverter system. It can be seen that the V_{CM} is almost constant and equals to $V_{dc}/2$ by using only seven voltage vectors among all the available voltage vectors of the conventional three level SVPWM. Since V_{CM} is almost constant the leakage current with the proposed method is very small almost negligible.

Fig. 12 shows the leakage current of the system when the proposed SVPWM is used. Since the proposed SVPWM produces almost constant CM voltage as discussed for Fig. 11 above, the constant CM voltage helps in mitigation of the leakage current. The peak value of leakage current shown in Fig. 12 is 0.25 mA.

Fig. 13 shows the voltage vectors applied in the corresponding sectors. As discussed in section 3.3 and Fig. 5, for sector 1 the voltage vectors used are V_1, V_7 and V_{12}, that is also true for simulation results shown in Fig. 13.



(a) V_{CM}



(b) Zoom-in-view of V_{CM}

Fig. 11 Common mode voltage VCM when proposed SVPWM is applied

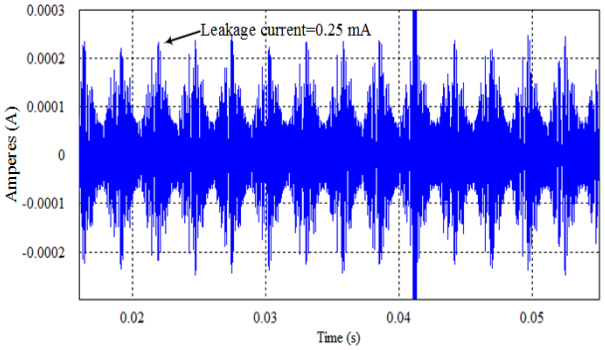


Fig. 12 Leakage current when proposed SVPWM is used

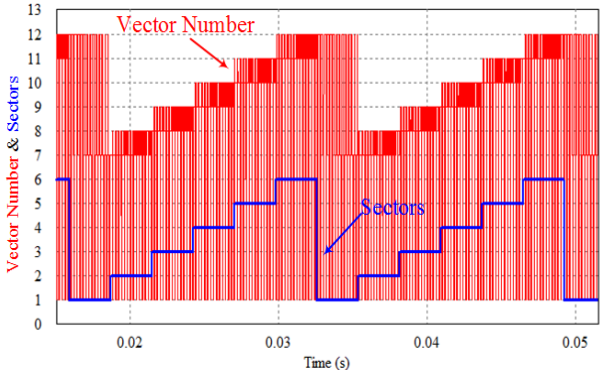


Fig. 13 Voltage vectors used in each sector

6. Experimental results

Experiments were carried out for the system shown in Fig. 1 and the experimental parameters are same as simulation parameters which are given by Table 4. Experimental setup is shown in Fig. 14. The experimental results are presented in figures from Fig. 15 to Fig. 17.

Fig. 15 shows the three phase output currents of the transformerless grid connected inverter system. The peak value of the phase currents is 416 A.

Fig. 16 shows the output voltages of the system. Fig. 16(a) shows the pole voltage V_{aO} and Fig. 16(b) shows the line-to-line voltage V_{ab} of the three level inverter. The results for are well matched with the simulations and consists of five voltage levels. Each time the line voltage varies between one of five levels of the and zero as also described for the simulation result of Fig. 10(b).

1 NPC inverter
2 NPC input & output
3 Oscilloscope
4 AC filter capacitor
5 Power stack
6 Interfaced reactor

Fig. 14 Experimental setup

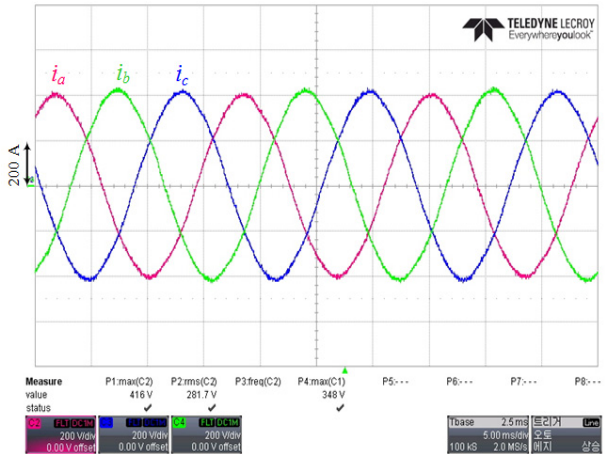
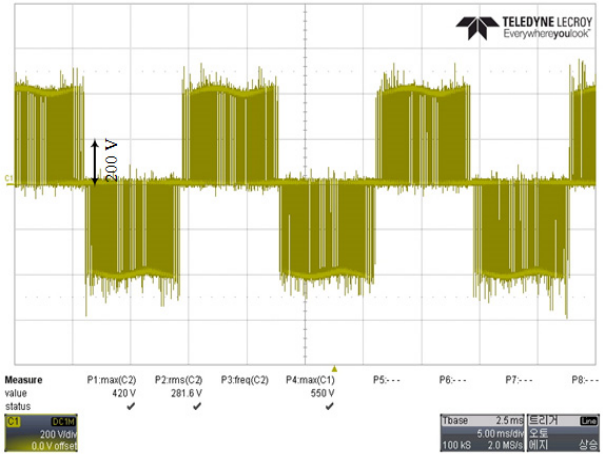
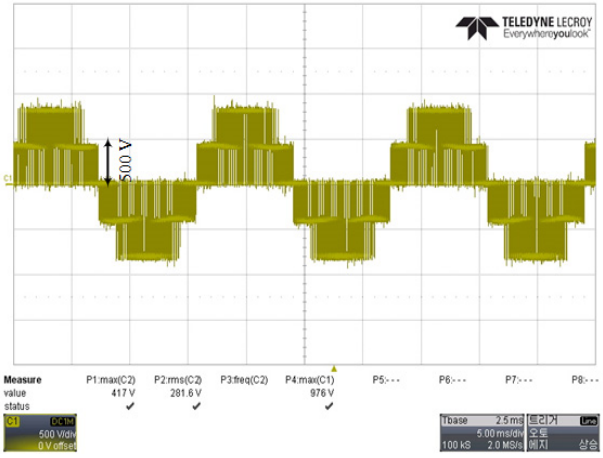


Fig. 15 Three phase output currents when proposed SVPWM is applied



(a) Pole voltage VaO



(b) line-to-line voltage V_{ab}

Fig. 16 Output voltage of three level inverter when proposed SVPWM is used

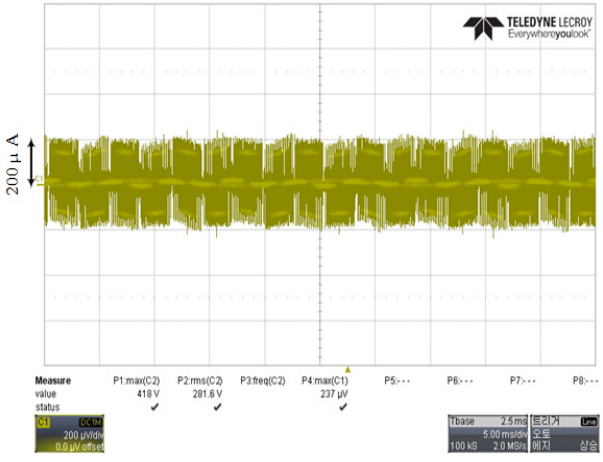


Fig. 17 Leakage current when proposed SVPWM is applied

Fig. 17 shows the leakage current of the transformerless grid connected inverter system. It can be seen that the leakage current with the proposed method is very small and equals to 0.237 mA.

7. Conclusion

In this paper a simplified SVPWM for three level inverter is proposed by which the three level SV diagram is simplified into a two level SV diagram thus reducing the computational effort required to obtain the on time calculations for all the voltage vectors available in conventional three level SVPWM. Also with the proposed

method the common mode voltage of three level inverter is kept constant by using only medium vectors and a zero vector only. Keeping the common mode voltages of three level inverter constant helps in eliminating the leakage currents, which can be troublesome in transformer less PV grid connected power systems.

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