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Temperature Dependence of Electrical Parameters of Silicon-on-Insulator Triple Gate n-Channel Fin Field Effect Transistor

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In this work, the temperature dependence of electrical parameters of nanoscale SOI (silicon-on-insulator) TG (triple gate) n-FinFET (n-channel Fin field effect transistor) was investigated. Numerical device simulator ATLAS™ was used to construct, examine, and simulate the structure in three dimensions with different models. The drain current, transconductance, threshold voltage, subthreshold swing, leakage current, drain induced barrier lowering, and on/off current ratio were studied in various biasing configurations. The temperature dependence of the main electrical parameters of a SOI TG n-FinFET was analyzed and discussed. Increased temperature led to degraded performance of some basic parameters such as subthreshold swing, transconductance, on-current, and leakage current. These results might be useful for further development of devises to strongly down-scale the manufacturing process.

Keywords: Nanotechnology, Device scaling, FinFET, Leakage current, Gate length, Silvaco software

1. INTRODUCTION

As semiconductor devices are steadily shrinking recently, high leakage currents and SCEs (short channel effects) such as DIBL (drain induced barrier lowering) and threshold voltage (V_{th}) roll-off are becoming so important that they are of major concerns to integrated circuit designers. Many recent works have been focused on novel device designs in order to tackle this problem. FinFET (Fin field-effect transistor) has been introduced as a novel device structure for all production companies such as TSMC, Intel, and Samsung to obtain a high performance of microprocessors beyond the barrier of 14 nm [1,2]. Compared to conventional MOSFET (metal oxide semiconductor field effect transistor), the FinFET provides a better electrical control over the channel, thus leading to significant improvements of device performance [1-3]. For FinFET, the body thickness T_{Fin} should be

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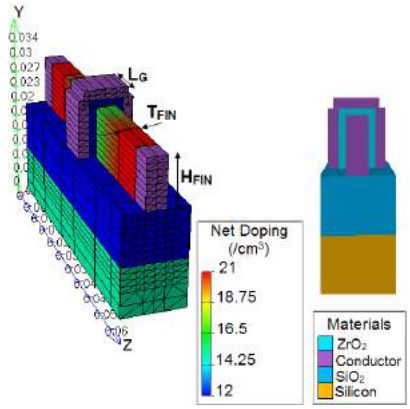

Fig. 1. Illustration of the SOI TG n-FinFET structure.

approximately half of the gate length L_G to provide better control of short channel effects. When the L_G/T_{FIN} ratio is smaller than 1.5, the drain induced barrier lowering, subthreshold swing, and leakage current are increased sensibly [2-8].

SOI (Silicon-on-insulator) wafers are typically used for FinFET fabrication [9]. The use of SOI substrate in manufacturing microprocessors has been introduced by major semiconductor companies with the aim to minimize parasitic capacitances and improve current drive, circuit speed, and power consumption [1].

Increased power consumption and degraded device performance are observed when SiO_2 is used as gate insulator [10]. Therefore, high-k dielectric materials (Al_2O_3, La_2O_3, and ZrO_2) are considered as promising solution to improve gate control on the channel region and increase electrical performance [11]. The region between the source and the drain of the considered device is covered by zirconium dioxide (ZrO_2, κ = 25) as high-κ gate dielectric materials to allow further miniaturization of electronic components [12,13].

In this paper, we determined the performance of FinFET device using semiconductor TCAD tools. In the simulation, Lombardi CVT (constant voltage and temperature), SRH (Shockley-Read-Hall), and AUGER (Auger) models were considered. The main results of these simulations were extracted and compared to the results presented in recent papers. Results of the present analysis, will help improve the performance of FinFET device. This study was performed with various electrical characteristics, such as V_{th}, SS (subthreshold swing), transconductance (g_m), DIBL, on-current (I_{on}), leakage current (I_{off}), and on/off current ratio. Their temperature (T) dependence was analyzed.

2. DEVICE STRUCTURE

The 3D schematic view of the simulated TG (triple gate) FinFET structure is shown in Fig. 1. The device dimensions L_G, H_{FIN}, T_{FIN}, and t_{ox} are gate length, height of silicon fin, thickness of silicon fin, and thickness of gate oxide, respectively.

The thin ZrO_2 layer was used to replace conventional SiO_2 gate dielectric material for a good gate control of SCE. In the TG FinFET under analysis, as depicted in Fig. 1, the gate oxide thickness was equal in all three sides of the fin region. It was fixed at 1.5 nm. The height of silicon fin (H_{FIN} = 10 nm) was defined as the distance between the top gate and bottom gate oxides. The thickness of silicon fin (T_{FIN} = 4 nm) was defined as the distance between front gate and back gate oxides [14].

The channel region was formed by a slightly doped volume with doping concentration of 10^{16} cm^{-3} (p-type). The doping concentrations of the source/drain regions were assumed to be uniform and equal to 10^{21} cm^{-3} (n-type). The value of the gate work function was 4.53 eV.

3. DEVICE SIMULATION USING SILVACO-ATLAS

Numerical device simulator ATLAS™ was used to simulate the structure of the proposed SOI TG n-FinFET device. A numerical simulation in SILVACO consisted of two main steps: structure creation and numerical resolution. Structure creation included the definition of the mesh, the different regions of the device, electrodes, and doping. Numerical resolution included the definition of the gate work function, the choice of physical models, and the mathematical methods used by the simulator [14]. The choice of the physical models is important to improve the accuracy of the numerical simulation results. In our simulation, the inversion-layer Lombardi CVT (constant voltage and temperature) mobility model were considered. Auger model was invoked to deal with the minority carrier recombination. SRH (Shockley-Read-Hall) generation and recombination model were also used. Two numerical methods (Gummel and Newton) were employed to achieve the results [14].

The threshold voltage in case of a MuGFET (multiple gate field-effect transistor) can be expressed in the following equation [1]:

$$V_{Th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (1)$$

where Q_{ss} represents the charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents the metal-semiconductor work function difference between the gate electrode and the semiconductor, and Φ_f is the Fermi potential for p-type silicon that is given by the following equation:

$$\Phi_f = \frac{KT}{q} \ln \frac{N_A}{n_i} \quad (2)$$

where K is the Boltzmann constant, T is the temperature, q is the electron charge, N_A is the acceptor concentration in the p-substrate, and n_i is the intrinsic carrier concentration.

When a dielectric material is inserted, the capacitance is increased by the relative dielectric constant value κ. In this case, the capacitance is described as follows [11]:

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \quad (3)$$

where κ is the dielectric constant of the material ($\kappa = \varepsilon/\varepsilon_0$), and ε_0 is the permittivity of free space.

The critical electrical parameters such as SS (subthreshold swing) and DIBL (drain-induced barrier lowering) are defined below [4]:

$$SS(mV/dec) = \frac{d V_{GS}}{d(\log_{10} I_{DS})} \quad (4)$$

$$DIBL(mV/V) = \frac{\Delta V_{Th}}{\Delta V_{DS}} \quad (5)$$

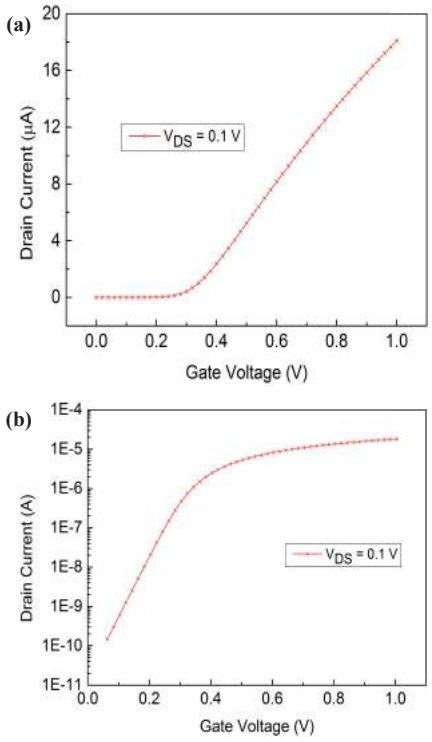

Fig. 2. Linear (a) and log scale (b) of I_{DS} versus V_{GS} for TG FinFET device at V_{DS} = 0.1 V.

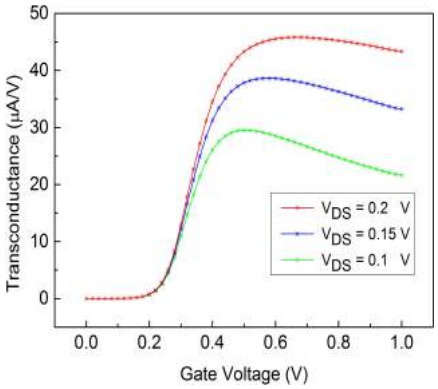

Fig. 3. Transconductance versus V_{GS} for a TG n-FinFET device at different drain-source voltage values.

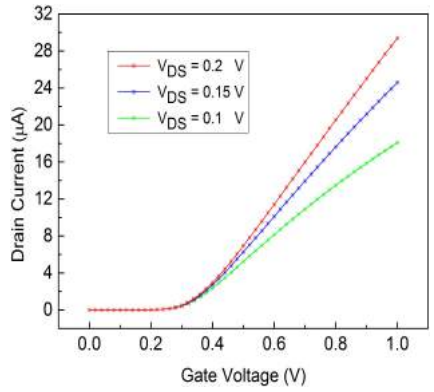

Fig. 4. I_{DS}-V_{GS} characteristics on a linear scale for an SOI n-FinFET device at different drain-source voltages.

SS is defined as the change in gate voltage that must be applied in order to create a one decade increase in the output current. The lowest theoretical limit for SS is 60 mV/decade at room temperature [15]. DIBL is defined as the ratio of the difference in threshold voltage measured at a low value to high value of the drain voltage [15].

The transconductance quantifies the drain current variation due to gate-source voltage variations while keeping the drain-source voltage constant [15]. Therefore, the value of gm is extracted by taking the derivative of the I_{DS}-V_{GS} curve.

The threshold voltage is a very important parameter for obtaining higher on-current that can improve circuit speed. I_{DS} can be calculated with the following formula as described previously [15]:

$$I_{DS}(nA) = 100\frac{W}{L}e^{\frac{q(V_{GS}-V_{Th})}{\eta KT}} \quad (6)$$

where W is the width of the channel, L is the channel length, q is the electronic charge, and η is the body factor that is proportional to the change in gate voltage with a change in channel potential [15].

The leakage current is directly related to the SS. I_{off} can be calculated with the following formula [15]:

$$I_{off}(nA) = 100\frac{W}{L}10^{\frac{-V_{Th}}{SS}} \quad (7)$$

A well-behaved I-V characteristic of an 8 nm gate length TG n-FinFET device was reported at a gate work function of 4.53 eV (Fig. 2). The gate voltage V_{GS} was swept from 0 to 1 V with a step of 0.02 V. The threshold voltage and maximum transconductance were 0.27 V and 29.54 μA/V at V_{DS} = 0.1 V, respectively, as illustrated in Fig. 2(a) and Fig. 3. The threshold voltage obtained had a very good value as compared to the one obtained by Baravelli et al. (i.e., 0.36 V) [16]. There were some modifications at the level of the work functions of the metal gates to reach the desired V_{th} value. The SS and DIBL of the considered SOI TG n-FinFET device with L_G = 8 nm, T_{FIN} = 4 nm, and H_{FIN} = 10 nm (i.e., 63.93 mV/dec and 34.87 mV/V) showed an improvement when compared to TG FinFET device with L_G = 20 nm, T_{FIN} = 8 nm, H_{FIN} = 25 nm (i.e., 71.82 mV/dec and 35.53 mV/V) or with L_G = 16 nm, T_{FIN} = 8 nm, H_{FIN} = 32 nm (i.e., 70 mV/dec and 70 mV/V) [17,18].

The transfer characteristic dependence on the drain-source voltage of the n-channel FinFET is illustrated in Fig. 4. Variations of the drain current with drain to source voltage for different gate to source voltage values are shown in Fig. 5. The leakage current is directly related to the SS. The leakage current output is 20.41 pA at V_{GS} = 0 V and V_{DD} = V_{DS} = 1 V (Fig. 6). The leakage current and the subthreshold swing of the considered device (i.e., 20.41 pA and 63.93 mV/decade) are very good when compared to the results of a recent work [19] using gate-all-around MOSFET with L_G = 20 nm, T_{FIN} = 12 nm, H_{FIN} = 24 nm (i.e., 700 pA and 86.73 mV/dec), even with a smaller physical L_G. The leakage current of the considered device (i.e., 20.41 pA) is improved if compared to results of a recent paper reporting on a 16 nm n-type FinFET (i.e., 164 pA) [20]. It is important to keep I_{off} very small in order to minimize the static power dissipation even when the device is in a standby mode. All minimum values of these device parameters are required for small sizes of the transistor. Furthermore,

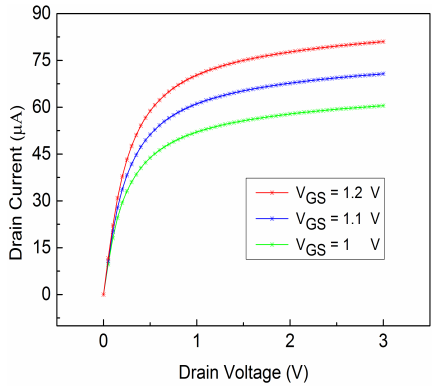

Fig. 5. I_{DS}-V_{DS} characteristics for an SOI n-FinFET at different gate voltages.

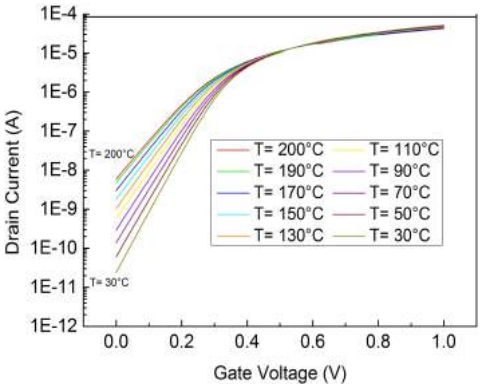

Fig. 8. Log scale of I_{DS} versus V_{GS} at different temperatures at V_{DS} of 1 V. {In this case the device is simulated at V_{DS} = 1 V}

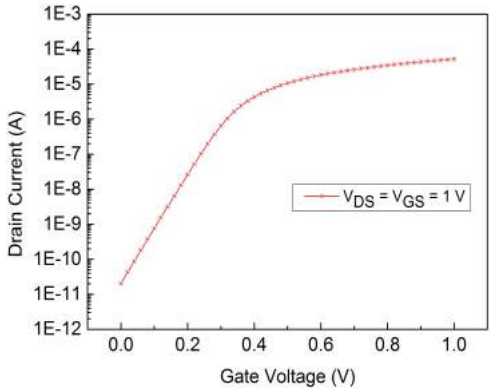

Fig. 6. I_{DS}-V_{GS} characteristics on a log scale for an SOI n-FinFET at V_{DS} of 1 V.

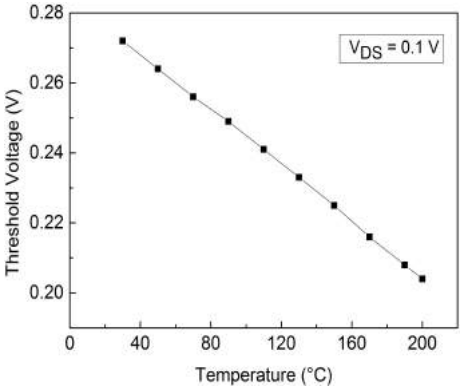

Fig. 9. Threshold voltage versus temperature with V_{DS} at 0.1 V.

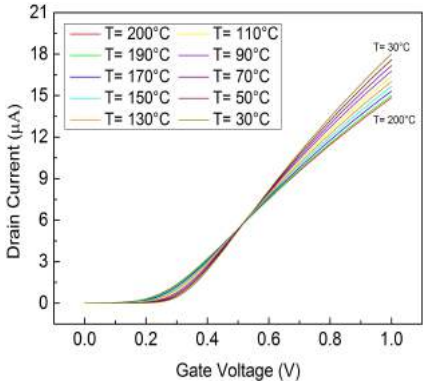

Fig. 7. Linear scale of I_{DS} versus V_{GS} at different temperatures at V_{DS} of 0.1 V.

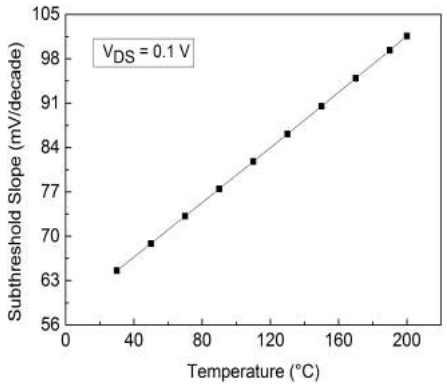

Fig. 10. Subthreshold slope versus temperature with V_{DS} at 0.1 V.

transistor dimensions are scaled to minimize parasitic capacitances to reduce power consumption and improve both current drive and circuit speed. The ratio of I_{on}/I_{off} exceeded 106 for the analyzed device with silicon channel material and ZrO_2 gate dielectric material at room temperature, indicating excellent on-state and off-state characteristics when compared to the results of a paper using a 20 nm conventional FinFET (i.e., 7.42 103) [22]. These simulations were carried out by setting the device temperature at T = 300 K and keeping the fin thickness at minimum (≈ $L_G/2$).

Linear scale of I_{DS} versus V_{GS} transfer characteristics at different temperatures with TG n-FinFET device structure at V_{DS} of 0.1 are shown in Fig. 7. Log scale of I_{DS} versus V_{GS} transfer characteristics at different temperatures with TG n-FinFET device structure at V_{DS} of 1 V are shown in Fig. 8. As T was increased from 30℃ to 200℃, the device with a T_{FIN} of 4 nm showed V_{th} decrease (from 0.27 to 0.20 V) and SS (subthreshold slope) degradation (from 64 to 101 mV/dec) as shown in Fig. 9 and Fig. 10, respectively. In a FinFET device, the decrease of threshold voltage with temperature tends to increase drain current in weak inversion while the mobility reduction causes a decrease in strong inversion [22,23]. A gate bias point exists when these opposing effects compensate each other, thus exhibiting the so-called ZTC (zero temperature coefficient) point [24,25]. The ZTC

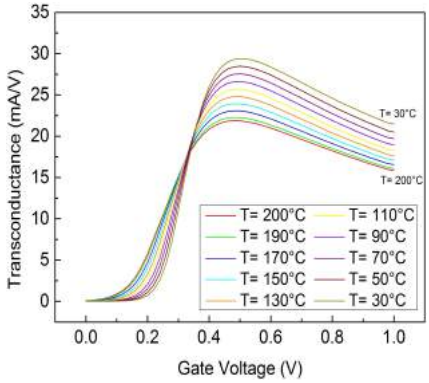

Fig. 11. Transconductance characteristics at different temperatures with V_{DS} at 0.1 V.

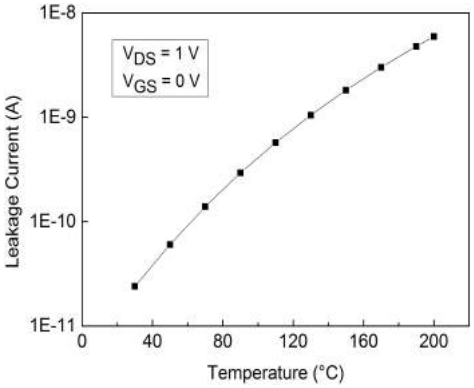

Fig. 14. Leakage current as a function of temperature with V_{DS} at 1 V and V_{GS} at 0 V.

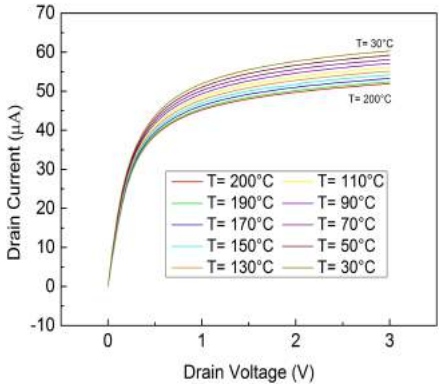

Fig. 12. Linear scale of I_{DS} versus V_{DS} at different temperatures with V_{DS} at 0.1 V.

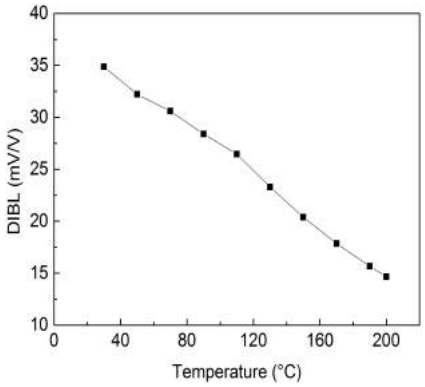

Fig. 15. DIBL as a function of temperature at V_{DS} at 0.01 V (V_{DS} low) and V_{DS} at 0.05 V (V_{DS} high).

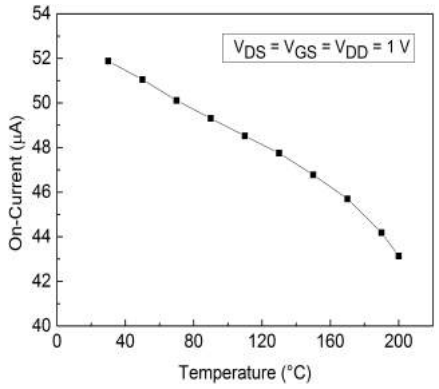

Fig. 13. On-current of TG n-FinFET as a function of temperature with V_{DS} at 1 V.

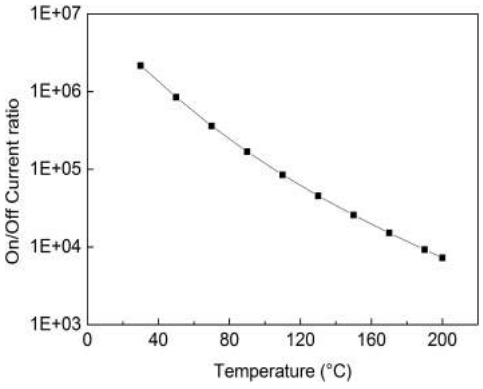

Fig. 16. On/off current ratio as a function of temperature.

point occured around VG of 0.52 V for the FinFET device under test as shown in Fig. 7. The transconductance characteristics as a function of the gate voltage at various device temperatures with W of 4 nm and L of 8 nm at V_{DS} of 0.1 V are shown in Fig. 11. The simulated transconductance exhibited roughly the same shape at different maximum values and different temperatures. In particular, the transconductance was first increased and then decreased with increasing gate voltage at V_{DS} = 0.1 V (Fig. 11). The maximum transconductance (gmmax) was degraded with increasing temperature (from 29.4 to 21.8 mA/V). The temperature dependence of Output I_{ds}-V_{ds} characteristics is shown in Fig. 12. The on-current of the TG n-FinFET device was decreased with increasing temperature (from 51.8 to 43.1 μA) as the gate bias was larger than ZTC bias (Fig. 13). This occurred because the threshold voltage was decreased more with increasing temperature while the mobility reduction was lower. The increase of temperature increased the intrinsic carrier concentration in silicon, which in turn increased the leakage current and a tendency of degrading the ratio of I_{on}/I_{off} (Fig. 16, [26,27]). The carrier mobility increased as the temperature increased, which resulted in increased leakage current with increasing temperature, as shown in Fig. 8 and Fig. 14.

The sensitivity of DIBL to temperature is shown in Fig. 15. During accurate circuit design, the first important step is to neutralize these DIBL effects related to temperature.

4. CONCLUSIONS

In this work, the performance of a tri-Gate n-channel FinFET structure was analyzed by using a TCAD simulator. The newly proposed transistor structure is compatible with current manufacturing process. It exhibited good performance characteristics down to 8 nm by using ZrO_2 as gate dielectric material. The temperature dependence of the main electrical parameters of the SOI TG n-FinFET transistor was studied in the range from 30 to 200℃. Variations of parameters such as threshold voltage, subthreshold swing, transconductance, drain induced barrier lowering, on-current, leakage current, and on/off current ratio with temperature were extracted and discussed. These results might be useful for further developing devices that can strongly downscale the manufacturing process.

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