

DC and RF Analysis of Geometrical Parameter Changes in the Current Aperture Vertical Electron Transistor

Hye Su Kang*, Jae Hwa Seo*, Young Jun Yoon*, Min Su Cho* and In Man Kang[†]

Abstract – This paper presents the electrical characteristics of the gallium nitride (GaN) current aperture vertical electron transistor (CAVET) by using two-dimensional (2-D) technology computer-aided design (TCAD) simulations. The CAVETs are considered as the alternative device due to their high breakdown voltage and high integration density in the high-power applications. The optimized design for the CAVET focused on the electrical performances according to the different gate-source length (L_{GS}) and aperture length (L_{AP}). We analyze DC and RF parameters inducing on-state current (I_{on}), threshold voltage (V_t), breakdown voltage (V_B), transconductance (g_m), gate capacitance (C_{gg}), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}).

Keywords: Gallium nitride (GaN), Current aperture vertical electron transistor (CAVET), Vertical transistor, TCAD

1. Introduction

Field-effect transistors (FETs) based on gallium nitride (GaN) have considered as the preferred choice for high power electronic devices owing to the wide band gap, high critical electric field, and high electron mobility of GaN [1-6]. AlGaIn/GaN-based high electron mobility transistor (HEMT) has the two-dimensional electron gas (2-DEG) generated by the spontaneous polarization and piezoelectric polarization that have superior properties such as high power density and high breakdown voltage, and high channel electron mobility. The 2-DEG facilitate a high drain current, low on-state resistance (R_{on}), and low gate-drain charge, which are caused by the high channel mobility, high channel density, and high breakdown electric field. These properties make the AlGaIn/GaN HEMTs extremely useful for high power applications. However, the RF output power obtained by AlGaIn/GaN HEMTs have been degraded due to the DC-RF dispersion [7-10].

However, when the vertical HEMT is applied the bias, the highest fields produced in the bulk rather than at the surface. The electric field at the surface, which results from the small potential difference between the gate and the source, is relatively small, so the surface states should not fill up with electrons. Thus, DC-RF dispersion in vertical HEMT is reduced [11]. For these reasons, the GaN-based vertical transistor has become an attractive alternative for power devices. Significant progress has been made recently in the demonstration of high power devices in the group-III nitride-based vertical field-effect transistors employing a current aperture vertical electron transistor (CAVET),

which have been developed by Mishra et al [12-14]. The devices had been successfully developed in the fabrication. Aperture length (L_{AP}) and current blocking layer (CBL) are the important design parameters of CAVET. The electrical characteristics according to various changes about the gate-source length (L_{GS}) and L_{AP} have not been studied.

In this paper, we analyze a CAVET in terms of the DC performance parameters including on-state current (I_{on}), threshold voltage (V_t), breakdown voltage (V_B), transconductance (g_m), resistance components with varying L_{AP} and L_{GS} by the device simulation. We also analyze the RF characteristics such as the gate capacitance (C_{gg}), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) by varying L_{GS} and the number of apertures (N_{AP}). The simulations were conducted by Silvaco ATLAS program [15].

2. Simulation Results and Discussions

2.1 Device structure

Fig. 1 shows a schematic cross-sectional view of the simulated CAVET structure. It consists of the 2.5 μm thick N^+ GaN (Donor of $1 \times 10^{18} \text{ cm}^{-3}$) buffer layer, the N^- GaN (Donor of $5 \times 10^{16} \text{ cm}^{-3}$) layer, and the N^- channel GaN layer of thickness is at 0.5 μm (Donor of $5 \times 10^{16} \text{ cm}^{-3}$), and the N^- channel GaN layer thickness is at 2.5 μm , 0.5 μm , and 0.05 μm , respectively. The N^- GaN aperture layer has the same doping as that of the N^- GaN layer used in the source region. The L_{AP} that is used to provide a current path in the device is an important design parameter in the CAVET. The thickness of the AlGaIn layer is 25 nm and the Al composition in AlGaIn is 24%. The polar.scal model was determined by the 2-DEG density, the gate length (L_G)

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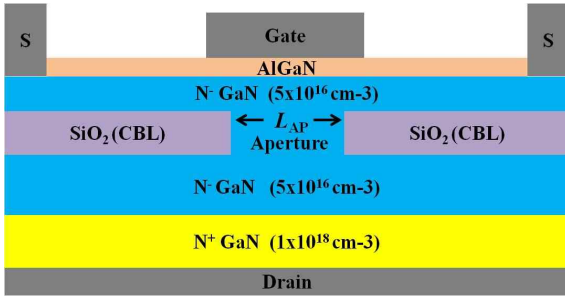


Fig. 1. Schematic cross-sectional view of the simulated CAVET structure

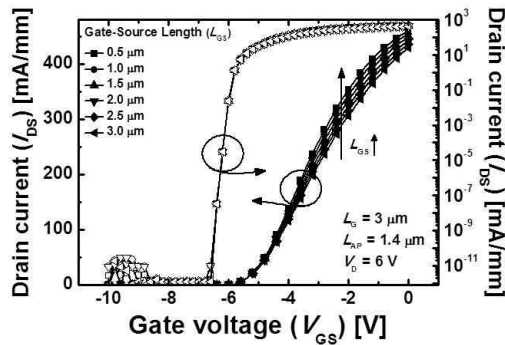


Fig. 2. Comparison of the I_{DS} - V_{GS} characteristics transfer curves of the simulated for CAVET with various gate-source length (L_{GS})

and the work function which were specified as $1.12 \times 10^{12} \text{ cm}^{-3}$, $3.0 \text{ }\mu\text{m}$, and 5.2 eV , respectively. L_{GS} was varied from $0.5 \text{ }\mu\text{m}$ to $3.0 \text{ }\mu\text{m}$ and L_{AP} values were taken to be $1.0 \text{ }\mu\text{m}$, $1.4 \text{ }\mu\text{m}$, and $1.8 \text{ }\mu\text{m}$. We have obtained the accurate simulation results by using the k.p model and the gansat model. We used the k.p band and gansat parameter model. The k.p model is to calculate the effective masses and band edge energies for wurtzite structure of GaN in drift-diffusion simulation. And the field dependent mobility in nitrogen is obtained by the gansat model. The CAVET is operated by supply voltage bias. The drain current flows through the aperture and into the drain. Thus, the aperture length that is used to provide a current path in the device is an important design parameter in the CAVET. The current blocking layer (CBL) is used to block the current falling vertically down through any other path except that from the aperture to the drain.

2.2 Results of DC characteristic

Fig. 2 shows the I_{DS} -gate voltage (V_{GS}) curves of CAVET for different values of L_{GS} varying from $0.5 \text{ }\mu\text{m}$ to $3 \text{ }\mu\text{m}$. The L_{AP} and L_G are fixed as $1.4 \text{ }\mu\text{m}$ and $3 \text{ }\mu\text{m}$, respectively. It is seen that the I_{DS} increases with a decrement in the L_{GS} owing to an increase in the resistance characteristics of L_{GS} .

The I_{on} transfer curves are investigated for different

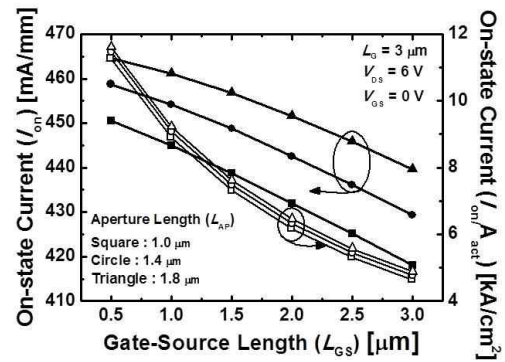


Fig. 3. Output characteristics of the simulated the CAVET of I_{on} and I_{on}/A_{act} with L_{GS} and L_{AP} ($L_G=3 \text{ }\mu\text{m}$, $V_{DS}=6 \text{ V}$ and $V_{GS}=0$)

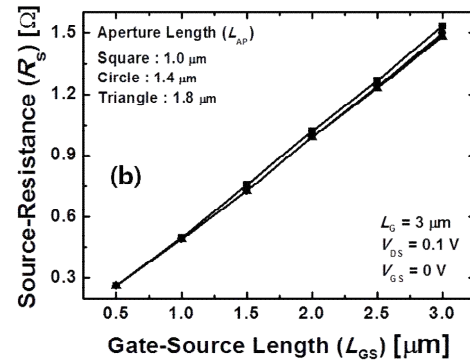
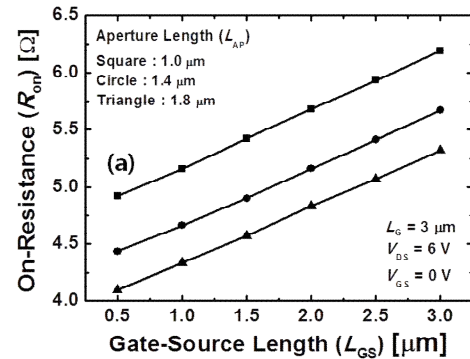


Fig. 4. Resistance components as a function of L_{GS} and L_{AP} (a) R_{on} and (b) R_s

values of L_{GS} at fixed L_{AP} values of $1.0 \text{ }\mu\text{m}$, $1.4 \text{ }\mu\text{m}$ and $1.8 \text{ }\mu\text{m}$ in Fig. 3. The I_{on} is indicating the two statements. The active area on state current (I_{on}/A_{act}) is defined as the current per unit active area (A_{act}). The A_{act} defines the transistor area between the two source electrodes of the device.

For example, the A_{act} for a device with a separation of $7 \text{ }\mu\text{m}$ between the edges of the source and an aperture width of $1 \text{ }\mu\text{m}$ at $L_{GS}=1.4 \text{ }\mu\text{m}$ is $7 \text{ }\mu\text{m} \times 1 \text{ }\mu\text{m}$. The maximum

I_{on}/A_{act} values when L_{GS} was fixed at $0.5 \text{ }\mu\text{m}$ and L_{AP} was varied as $1.0 \text{ }\mu\text{m}$, $1.4 \text{ }\mu\text{m}$, and $1.8 \text{ }\mu\text{m}$ were determined to be 11.3 kA/cm^2 , 11.5 kA/cm^2 , and 11.6 kA/cm^2 , respectively. Also, at these values of L_{GS} and L_{AP} , the I_{on} 's were 450.5

mA/mm, 458.7 mA/mm, and 464.5 mA/mm, respectively. The I_{on} varies according to the changes in L_{GS} and L_{AP} . The I_{on} increases as L_{AP} is increased because aperture is the principal current path that relates to I_{on} .

However, I_{on} decreases as L_{GS} is increased. The reason for this variation is shown in Fig. 4 (a). The R_{on} depends on L_{GS} and L_{AP} and increases with an increase in both the parameters.

Fig. 4 (b) shows the simulated the variation of R_S with L_{GS} and L_{AP} . R_S is strongly affected by a change in L_{GS} that is more influential than a change in L_{AP} . Because there is 2-DEG at the channel, the channel resistance remains almost the same when L_{AP} is increased. As a result, L_{GS} ascertains the I_{on} and is the primary design parameter.

Fig. 5 shows the variation of g_m with L_{GS} and L_{AP} . It is seen that as L_{AP} is increased, g_m increases. The main reason for this dependence is that the aperture is the primary current path. However, g_m decreases when L_{GS} is increased owing to the resistance between the gate and the source.

Fig. 6 presents the V_B at different L_{GS} and L_{AP} values, which were extracted at 233 V, 233.3 V, and 233.5 V at L_{AP} values of 1.0 μm , 1.4 μm , and 1.8 μm , respectively. In addition, we obtained these results by using the Shockley-Read-Hall (SRH) recombination model and the Selberher's impact ionization model for the off-state breakdown

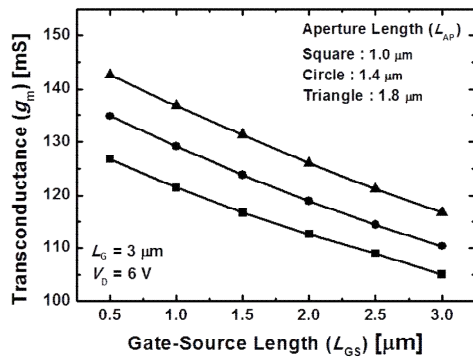


Fig. 5. Transconductance (g_m) as a function of the L_{GS} and L_{AP} .

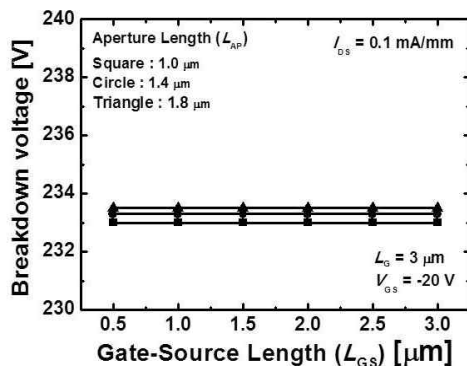


Fig. 6. Breakdown voltage (V_B) characteristics of the simulated for a CAVET according to L_{GS} and L_{AP} split ($L_G = 3 \mu\text{m}$ and $V_{DS} = -20 \text{ V}$)

characteristic [15]. V_B is constant, despite the increases in L_{GS} . In the case of a lateral device, breakdown occurs when electric field congregates at the gate edge. However, in this device the drain current flows in the vertical direction through the aperture. Therefore, breakdown is unrelated to the change in the L_{GS} .

Figs. 7 (a)-(c) show the simulated CAVET with impact generation rate for the L_{GS} split in the V_B at $L_{GS} = 1 \mu\text{m}$ and $V_{GS} = -20 \text{ V}$. Impact ionization needs a high electric field when typical non-equilibrium process. For example, an electron in the conduction band obtains its energy by external electric fields and becomes highly energetic. They were creating an electron-hole pair of come into collision an electron in the valence band and exciting it to the conduction band. In the CAVET, impact generation occurs

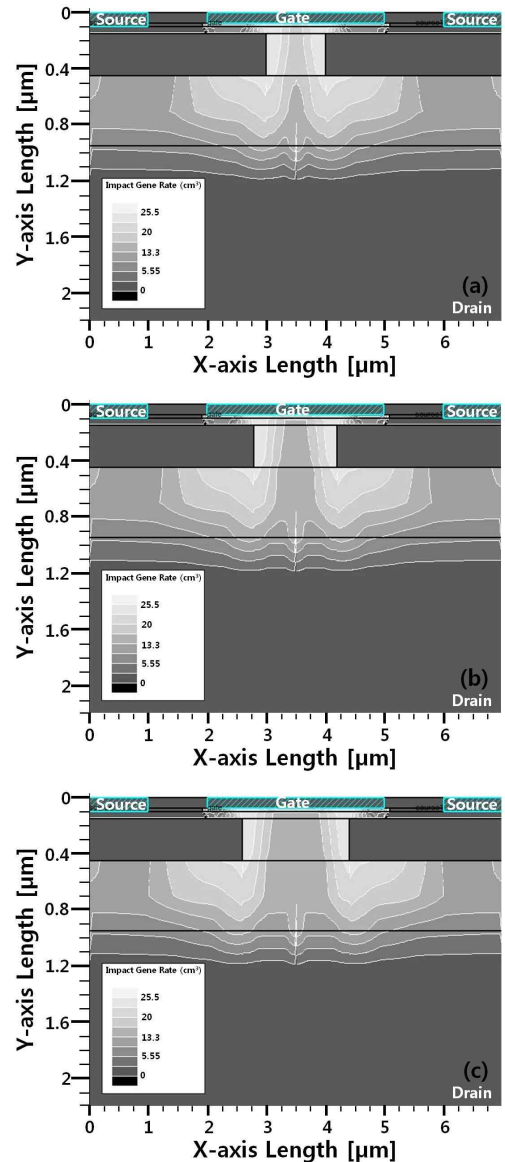


Fig. 7. Impact generation rate in the simulated V_B for CAVET with (a) L_{AP} of 1.0 μm , (b) L_{AP} of 1.4 μm , and (C) L_{AP} of 1.8 μm

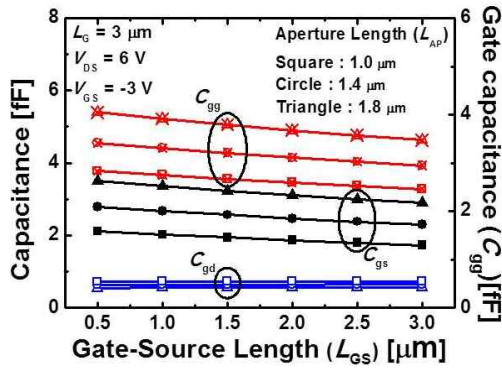


Fig. 8. Gate capacitance (C_{gs} , C_{gd} , C_{gg}) as a function of L_{GS} with different L_{AP}

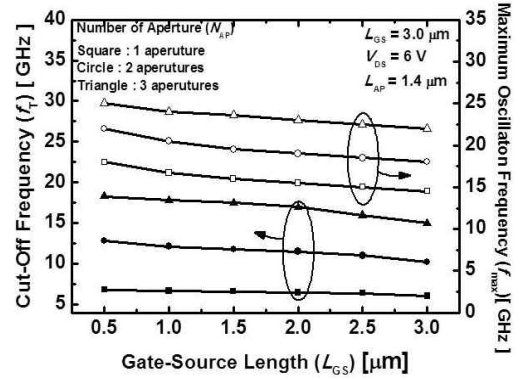


Fig. 9. f_T and f_{max} according to L_{GS} and N_{AP} split

at both ends of the aperture.

Fig. 7 (a) shows impact generation rate cross-sectional view of the simulated CAVET, which is higher than that in Figs. 7 (b) and (c), since the L_{AP} is shorter as compared to the latter. As the L_{AP} increases, impact generation rate decreases relatively. Thus, the V_B is affected strongly by L_{AP} as compared to L_{GS} .

As a result, V_B is constant, when the L_{AP} is increased from 1.0 μm to 1.4 μm , and then to 1.8 μm for varying L_{GS} .

2.3 Results of RF characteristic

In this section, the RF performance characteristics are shown. They have been extracted from the Y-parameters. Fig. 8 shows the dependence of C_{gd} , C_{gs} , and C_{gg} , on L_{GS} and L_{AP} . The values of C_{gd} , C_{gs} , and C_{gg} decrease as L_{GS} increases. The capacitance is directly proportional to the device area and in inversely proportional to the separation between the plates. In this CAVET, the total device area was fixed. Therefore, when L_{GS} increases, C_{gs} was decreased. In addition, as L_{AP} increases, capacitance charges increase owing to the increase in aperture.

Fig. 9 shows the f_T and f_{max} with a variation of N_{AP} , and L_{GS} . The f_T and f_{max} were extracted using the following Eqs. (1) and (2) [16].

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} \approx \frac{f_T}{\sqrt{4R_{g,eff}(g_{ds} + 2\pi f_T C_{gd})}} \quad (2)$$

Where, C_{gg} is the gate input capacitance, $R_{g,eff}$ is the effective gate resistance, and C_{gd} is the gate-to-drain capacitance. The g_m is directly proportional and C_{gg} is inversely proportional to f_T . Thus, g_m and C_{gg} are important design parameters. When L_{GS} increases, g_m decreases, owing to the characteristics of the resistance as shown by Fig. 4 (a). The L_{GS} is affected by not only f_T , but also f_{max} . In addition, when N_{AP} increases, I_{on} and g_m are improved because of the increased current path. It is verified that f_T

for 3-apertures is highly improved with a value of 18.0 GHz as compared to 6.67 GHz for 1-aperture device. The f_{max} is 16.5 GHz for 1-aperture device and 24 GHz for a 3-apertures device, when L_{GS} is fixed at 1.0 μm . As a result, it is seen that L_{AP} , L_{GS} and N_{AP} have a strong influence on the RF characteristics.

3. Conclusion

In this work, a CAVET was analyzed and studied by using 2-D TCAD simulations. In the DC characteristics, L_{GS} is inversely proportional to I_{on} and g_m because of R_S . Also, the V_B is affected by variation of L_{AP} , which has a much greater influence than the variation of L_{GS} . Since, the aperture is used as a current path in the device. It is an important design parameter in a CAVET. It has also been demonstrated that the RF performance can be improved by increasing N_{AP} . Consequently, the L_{AP} and N_{AP} have a stronger influence on the RF characteristics than L_{GS} . We observe that f_T and f_{max} can be improved by increasing N_{AP} in the same device area.

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References

- [1] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H.-S. Lee, F. Gao, T. Fujishima and T. Palacios, "Electrothermal

- Simulation and Thermal Performance Study of GaN Vertical and Lateral Power Transistors,” *IEEE Transactions on Electron Devices*, vol. 60, no.7, pp. 2224-2230, July 2013.
- [2] H. Yu, L. McCarthy, S. Rajan, S. Keller, S. Denbaars, J. Speck, and U. Mishra, "Ion implanted AlGaIn-GaN HEMTs with nonalloyed ohmic contacts," *IEEE Electron Device Lett.*, vol. 26, no. 5, pp. 283-285, May 2005.
- [3] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-Based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp.287-305, Feb. 2008.
- [4] M. S. P. Reddy, M.-K. Kwon, H.-S. Kang, D.-S. Kim, J.-H. Lee, V. R. Reddy, and J.-S. Jang, "Influence of Series Resistance and Interface State Density on Electrical Characteristics on Ru/Ni/n-GaN Schottky Structure," *J. Semicond. Technol. Sci.*, vol. 13, no. 5, pp. 492-498, Oct. 2013.
- [5] S. Y. Kim, J. H. Seo, Y. J. Yoon, J. S. Kim, S. Cho, J.-H. Lee and I. M. Kang, "Electrical Characteristics of Enhancement-Mode n-Channel Vertical GaN MOSFETs and the Effects of Sidewall Slope," *J. Electr. Eng. Technol.*, vol. 10, no. 3, pp. 1131-1137, May 2015.
- [6] C. B. Steven, I. Kiki, A. R. Jason, K. Walter, D. Park, B. D. Harry, D. K. Daniel, E. W. Alma, and L. H. Richard, "Trapping Effects and Microwave Power Performance in AlGaIn/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 465-471, March 2001.
- [7] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 332-343 June 2008.
- [8] K. Horio, K. Yonemoto, H. Takayanagi, and H. Nakano, "Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors," *J. Appl. Phys.*, vol. 98, no. 12, pp. 1818-1820, Dec. 2005.
- [9] X. Wang, S. Huang, Y. Zheng, K. Wei, X. Chen, H. Zhang, and X. Liu, "Effect of GaN Channel Layer Thickness on DC and RF Performance of GaN HEMTs With Composite AlGaIn/GaN Buffers." *IEEE Transactions on Electron Devices*, vol. 61, no.5, pp. 1341-1346, May 2014.
- [10] Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, and T. Palacios, "GaN-on-Si Vertical Schottky and p-n Diodes," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 618-620, June 2014.
- [11] I. Ben-Yaacov, Y.-K. Seck, U. K. Mishra, and S. P. DenBaars, "AlGaInGaIn current aperture vertical electron transistors with regrown channels," *J. Appl. Phys.*, vol. 95, no. 4, pp. 2073-2078, Feb. 2004.
- [12] Y. Gao, I. Ben-Yaacov, U. K. Mishra, and E. L. Hu, "Optimization of AlGaIn GaN current aperture vertical electron transistor (CAVET) fabricated by photoelectrochemical wet etching," *J. Appl. Phys.*, vol. 96, no. 11, pp. 1818-1820, Dec. 2004.
- [13] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on Bulk GaN Substrates Achieved With MBE-Regrown AlGaIn/GaN Layers to Suppress Dispersion," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41-43, Jan 2012.
- [14] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaIn/GaN CAVET With Mg-Ion-Implanted GaN as Current Blocking Layer," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 543-545, June 2008.
- [15] SILVACO International, ATLAS User's Manual, Apr. 2012.
- [16] Y. Tsididis, Operation and Modeling of the MOS Transistor, Oxford University Press, New York, USA, 1999, pp. 467-491, 500-504.



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