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Finite Control Set Model Predictive Current Control for a Cascaded Multilevel Inverter

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Abstract – In this paper, a Finite Control Set Model Predictive Control (FCS-MPC) for a five level cascaded multilevel inverter (CMLI) with reduced switch topology is proposed. Five switches are used here instead of conventionally used eight switches. The main contribution of this paper is to make the MPC controller work for the reduced switch topology using only 19 voltage vectors in place of conventional 61 voltage vectors for a five level CMLI. This simplifies the execution of the MPC algorithm, paving a way for the significant reduction in the computational time. The controller makes use of the excellent ability of MPC to multitask, by adding one more objective which is to reduce the average switching frequency in addition to controlling the load current. This is especially important, since switching losses and therefore switching frequency is significant for high-power applications. The trade-off of this MPC is that the current is not as smooth as the 61 vector scheme, but well within the limits of IEEE standards. The results shown prove that this MPC works well in steady state and dynamic conditions too.

Keywords: Total harmonic distortion, Multilevel inverter, Predictive current control, Switching states, Switching frequency

1. Introduction

In recent times, MLI has become popular and has attracted considerable interest. MLI include a group of power semiconductor devices and capacitors as voltage sources generating a stepped voltage waveform which has reduced harmonic distortion [1]. The various advantages of MLI are its capability of reducing voltage stress on power switches, less dv/dt ratio and common mode voltage, thus increasing the quality of the output [2]. There are number of different topologies of MLI such as Cascaded MLI (CMLI), Diode Clamped MLI (DCMLI) [3] and Flying Capacitor MLI (FCMLI) [4]. DCMLI and FCMLI requires clamping diodes and flying capacitors respectively both of which increases quadratically, if the level required is higher. Therefore three level DCMLI popularly known as Neutral Point Clamped (NPC) is explored in the literature for various applications. However in higher levels this inverter is seldom used. FCMLI on the other hand requires a complex control circuitry which needs to take care of pre-charging the capacitor. CMLI has various advantages such as modularity, flexibility, extendibility and reliability [5]. All these MLIs have same number of main switches. A three phase five level inverter has 24 main switches making the driver circuit cumbersome. Since then the researchers have started to search new family of multilevel inverters with reduced number of components.

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In this work, CMLI using N number of components for N levels is used. The new cascaded MLI uses five switches instead of eight switches per phase, for a single phase five level inverter thereby reducing the complexity of the control circuitry as well.

A promising technique for controlling this inverter is the Finite Control Set Model Predictive Control (FCS-MPC). FCS-MPC is a type of control which utilizes the discrete nature of the inverter reducing the processing time and calculation complexity. Since only finite number of switching positions are present in an inverter, the prediction is only for these states, and the one selected is that which minimizing the cost function. Moreover soft computing techniques such as neural networks and fuzzy can be combined with this predictive algorithm [6]

In this paper FCS-MPC is used to control the a five level CMLI with reduced components using only 31% voltage vectors,consequently reducing the number of calculations of cost functions for each sampling time. Therefore the computational load on the processor is reduced. The next section gives the motivation and research background. Section 4 and 5 explains the predictive control strategy. Section 5 and 6 shows the discussions on the simulation and the experimental results.

2. Motivation and Research Background

Model Predictive Control (MPC) even though developed in 1970, in process control industry has now reached its pinnacle of application in recent days [7, 8]. It's gaining

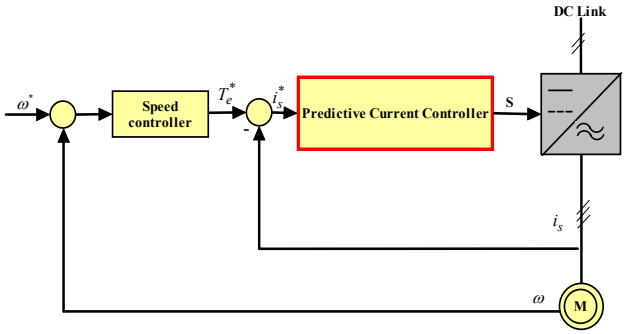


Fig. 1. Predictive current control with reference tracking for the three-phase five-level CMLI with an induction machine

popularity in power electronic and drives applications is only because of the availability of fast processor which has the ability of implementing much complex problems in fraction of seconds. The main advantage of the MPC controlled inverters are absence of modulator, utilization of variable switching frequency, possibility of online optimization, lower complexity for low level inverters and inclusion of constraints.

A FCS-MPC 's flexibility allows it to be used in various converters such as DC-DC converters [9] matrix converters, drives, active filters[10] distributed generation [11]systems, and power conditioning and in non-conventional renewable energy systems[12] uninterruptible power supplies[13]and energy storage systems[14].

Fig. 1 shows the classical cascade control scheme of an induction motor having the outer speed control loop and inner current control loop using predictive control. For the external speed control to work efficiently the inner current control has to be 100-500 times faster. Thus on the basis of its versatile application and its fast control performance, predictive current control proves to be an excellent choice to serve this purpose. The main aim of this current control loop to control the inverter such that the stator current of the induction motor is controlled.

Research of MPC controlled VSI has travelled a long road with its first publication in 2007. Here a discrete time model of the system is used to predict the future values of the load current for all the possible voltage vectors that is produced by the inverter [15]. A two level VSI has seven vectors voltage vectors. These seven voltage vectors are used in the cost function to evaluate the current error for the next sampling time.

Therefore for each sampling time there are seven predictions of the current. The work in [16] was the pioneer of the research for utilizing the MPC for the inverters. Simplified predictive control is used for a VSI for longer predictive zones is used in [17, 18]. However the sector information of the reference space vector is needed. This approach is able to decrease the computational effort considerably.

In [19, 20] FCS-MPC is applied to a five level CMLI with RL load. A five level MLI has 125 voltage vectors and calculating the current predictions for all the 125 voltage vectors for a single sampling time become cumbersome. Since, out of the 125 voltage vectors many are redundant, 61 non redundant voltage vectors are used in along with the adjacent voltage vector concept [21]. Our work proposes a new concept which reduces these 61 voltage vectors further down to 19, paving the way to reduction on computation time per sampling time and significantly reducing the calculation burden on the processor.

This paper focuses on the performance analysis of a reduced switch topology of three phase cascaded multilevel inverter controlled through predictive control algorithm. Predictive current control of a three phase five level 15 switch inverter topology involves only 19 voltage vectors. Thus using this strategy no. of calculation are less for each sampling time along with the reduction in number of switches.

3. Cascaded Multilevel Inverter with Reduced Number of Switches

A new family of CMLI is proposed with has less number of conducting devices. This family of inverter uses N+1

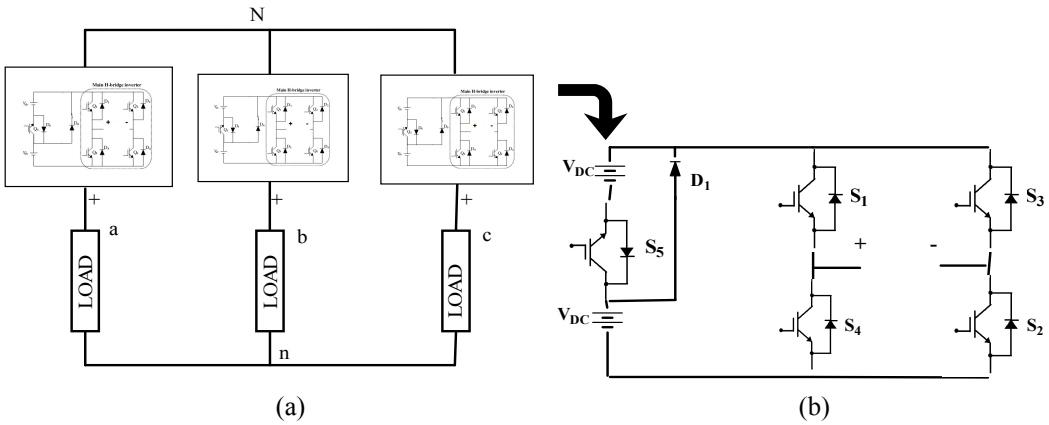


Fig. 2. (a)Three phase cascaded H bridge inverter with reduced switches; (b) internal structure of a single H bridge

Table 1. Switching states for reduced switch topology

Voltage levels	S1	S2	S3	S4	S5
+2Vdc	1	1	0	0	1
+Vdc	1	1	0	0	0
0	1	0	1	0	0
-Vdc	0	0	1	1	0
-2Vdc	0	0	1	1	1

number of switches for a N level inverter which works for effectively for all PWM technique. However, if one of the switches is replaced by a diode this inverter works just as efficiently. In this work, this inverter using N number of components for N levels thus reducing both the both circuit complexity and computational time. The new CMLI uses five switches instead of eight switches per phase, for a single phase five level inverter thereby reducing the complexity of the control circuitry as well.

For this 5-level inverter we require two voltage sources just as in conventional CMLI. The voltage sources used for the inverter have same voltage value. An extra switch and a diode is added to the normal H-bridge to form a 5-level inverter. The circuit of the 5-level inverter is shown in the Fig. 2. Therefore a single inverter consists of five switches and a diode with two voltage sources.

The inverter can be operated in five modes. All the operating modes of this inverter are given in the Table 1.

4. Predictive Current Control

Fig. 3 shows the block diagram of a FCS-MPC current controller controlling a five level inverter. It predicts the future behavior of the variables until a predefined horizon in time, and selects the switching states of the inverter which minimizes the cost function. Although the theory was developed in the 1970s, its application in power electronics is more recent due to its fast sampling times [20]. The fast microcontrollers available in last decade have triggered research in this control scheme. The main advantages of this scheme are: No modulator is required, variable switching frequency, on-line optimization is possible, low complexity for lower levels of inverter and the constraints can be included.

The basic idea present in MPC is to use a model to predict the future behavior of the current until a horizon in time, a cost function that represents the desired behavior of the system, the optimal switching states is obtained by minimizing the cost function.

4.1 System model

The inverter modelling is based on the output levels

$$V_{an}(t) = V_{aN}(t) + V_{Nn}(t) \tag{1}$$

where vaN is the inverter output voltage of phase a, and

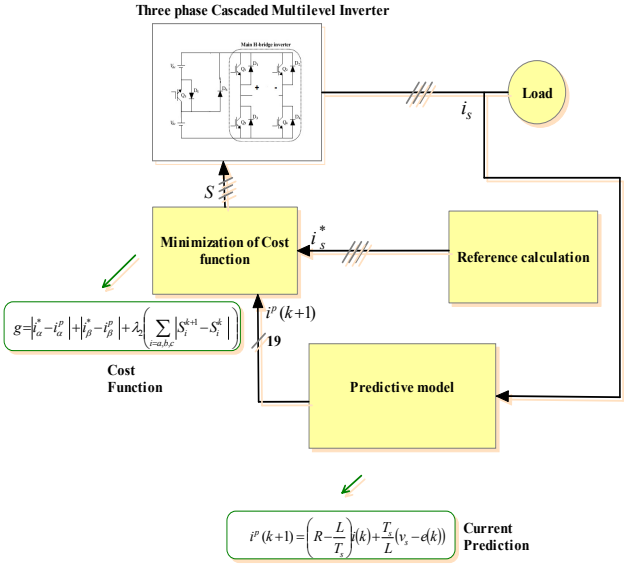


Fig. 3. An FCS-MPC block diagram for current control

vNn is the common-mode voltage, defined in terms of the inverter voltages as

$$V_{Nn}(t) = \frac{V_{aN}(t) + V_{Nn}(t) + V_{Cn}(t)}{3} \tag{2}$$

The load model is as follows

$$V_{an} = L\frac{di_a}{dt} + Ri_a \tag{3}$$

$$V_{bn} = L\frac{di_b}{dt} + Ri_b \tag{4}$$

$$V_{cn} = L\frac{di_c}{dt} + Ri_c \tag{5}$$

By applying the Laplace transform to the above equations transfer functions from voltage to current at the RL load are obtained:

$$\frac{I_a}{V_{an}} = \frac{1}{Ls + R} \tag{6}$$

$$\frac{I_b}{V_{bn}} = \frac{1}{Ls + R} \tag{7}$$

$$\frac{I_c}{V_{cn}} = \frac{1}{Ls + R} \tag{8}$$

For generating the voltage vectors we us the state space analysis in order to find the predictive value of the current.

$$a = e^{j2\pi/3} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{9}$$

$$v = \frac{2}{3}\left(v_{aN} + av_{bN} + a^2 v_{cN}\right) \tag{10}$$

$$v_{aN} = S_a * V_{dc} \quad (11)$$

$$v_{bN} = S_b * V_{dc} \quad (12)$$

$$v_{cN} = S_c * V_{dc} \quad (13)$$

Eg:- for switching state (S_a, S_b, S_c) = (0, 0, 0) generates voltage vector V_0 defined as

$$v_0 = \frac{2}{3}\left(0 + a0 + a^2 0\right) = 0 \quad (14)$$

5. Predictive Controller with Reduced Voltage Vectors

The predictive controller selects the switching states to be given to the inverter, which has the minimum cost function. While calculating this the controller has to do the process for 125 vectors. Calculating the cost function for all the 125 vectors at each sampling time is a burden for the controller. Therefore instead of the calculation being done for all the 125 vectors by removing the repeating redundant vectors, it is done only for 61 voltage vectors. Those 61 vectors are represented in the hexagon given in Fig. 4 (a). This voltage vectors are plotted in real and imaginary axis and are non- redundant or non-repeating vectors.

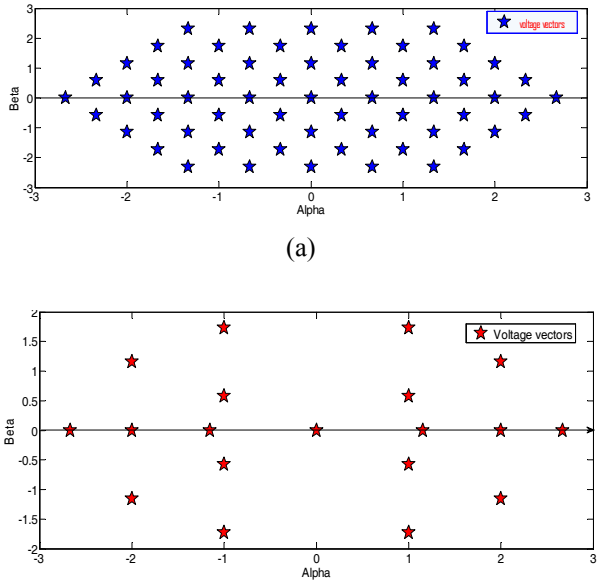
In the proposed algorithm, the 61 voltage vectors are reduced further. This is done by analyzing the voltage vectors and the switching states. Only the vectors where we get the algebraic sum of all three phase voltage levels equal to zero is chosen. For example consider a phase for 5- level inverter having voltage 2Vdc ie. $V_a=2V_{dc}$ and if the sum of the voltages of remaining two voltage levels should be equal to $-2V_{dc}$ ie. $V_b+V_c=-2V_{dc}$, those vectors are chosen. Such that voltage balance occurs which is shown in eqn (15)

$$V_a + V_b + V_c = 0 \quad (15)$$

The switching states corresponding to these voltage vectors are chosen. The inverter operates for all these 19 switching states which is proposed in this work. Fig. 4 shows both the 61 voltage vectors and 19 voltage vectors. Thus, the proposed algorithm reduces the computational burden to the system and therefore the time taken for the calculation is also reduced.

5.1 Objective function

The objective function aims at achieving the control of the inverter load current. The cost shown in the eqn. (16) includes this objective. Cost function for the current control of the inverter is given by



(a)

(b)

Fig. 4. Voltage vectors for a five level CMLI: (a) 61 vectors; (b) 19 vectors.

$$J = \left|i_\alpha^*(k+1) - i_\alpha^p(k+1)\right| + \left|i_\beta^*(k+1) - i_\beta^p(k+1)\right| \quad (16)$$

where $i_\alpha^*(k+1)$ $i_\beta^*(k+1)$ are the real and imaginary parts of the reference current vector $i_\alpha^p(k+1)$ $i_\beta^p(k+1)$) are the real and imaginary of the predicted load current vector.

$$\frac{di}{dt} = \frac{i(k+1) - i(k)}{T_s} \quad (17)$$

Therefore the predicted current is as follows

$$i^*(k+1) = \left(1 - \frac{RT_s}{L}\right) i(k) + \frac{T_s}{L}\left(v(k)\right)\hat{e}(k) \quad (18)$$

where R is the load resistance, L is the inductances is the sampling time, e ˆrepresents the back EMF. For every sampling time, the controllers calculates the values of all the 19 vectors and the switching states will be changed, such that the vector which is having minimum error and its corresponding switching state causing it will be fed as the input switching states to the inverter for that sampling.

5.1.1 Reduced switching frequency scheme

The cost shown in (16) includes only the objective of controlling current. The second objective function shown in (19) aims at achieving two objectives viz., controlling the load current and reducing the average switching frequency with above mentioned 19 vectors. The new objective function for this case is as follows:

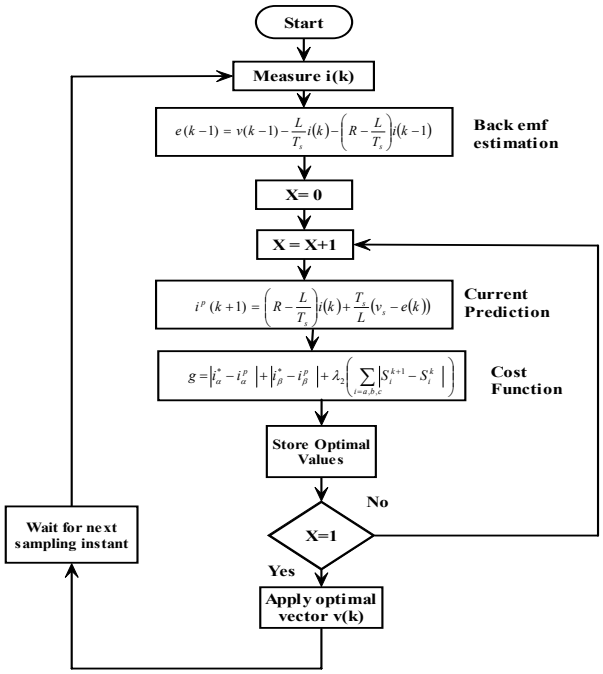


Fig. 5. Flow chart for FSMPC scheme

$$J=\left|i_{\alpha}^{*}\left(k+1\right)-i_{\alpha}^{p}\left(k+1\right)\right|+\left|i_{\beta}^{*}\left(k+1\right)-i_{\beta}^{p}\left(k+1\right)\right| +\lambda_{2}\left(\sum_{i=a,b,c}\left|S_{i}^{k+1}-S_{i}^{k}\right|\right) \quad (19)$$

S_i^k and S_i^{k+1} denote the switching state of phase i (i=a, b, c) in the current sampling time (between k^{th} and $(k+1)^{th}$ sampling instant) and the subsequent sampling time (between $(k+1)^{th}$ and $(k+2)^{th}$ sampling instant), respectively. $S_i^k = 0$ or 1, where 0 means that the top switch is off and the lower switch is on, and for 1 it is just the opposite. Fig. 5 shows the flow chart of the FCS-MPC using reducing average switching scheme.

6. Simulation results

The simulation is carried out in MATLAB/Simulink environment, to examine the FCS-MPC for the five level reduced switch cascaded MLI. This is done by comparing the control performance with the FCS-MPC utilizing 61 vectors and 19 vector scheme, for the same five level cascaded MLI under identical conditions. The effect of this controller both in steady state and transient conditions are studied and the results are benchmarked against the 61 vector scheme. The simulation parameters of R=220Ω and L=48mh at 0.98 power factor, VDC=100V and sampling time Ts is 25us is used.

6.1 Steady state control performance

In order to validate the control strategy, some perfor-

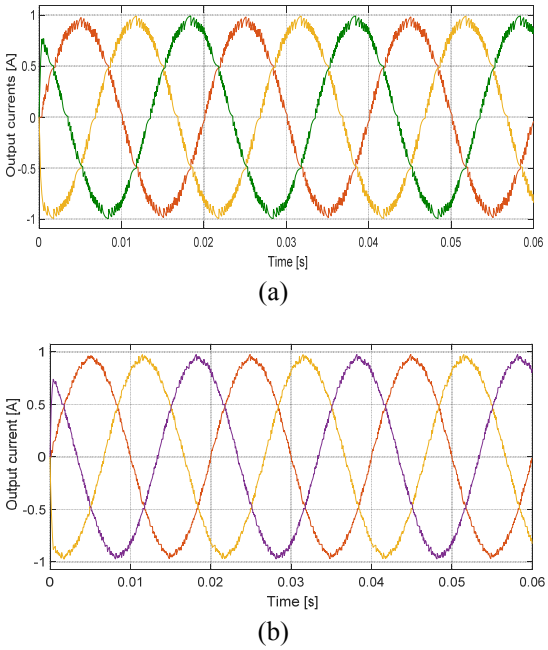


Fig. 6. (a) and (b). Three phase load current of the five level inverter

mance parameters are defined. The average switching frequency fs for a single semiconductor switch is calculated for all the 15 switches used in this topology. It is given by

$$f_s=\sum_{i=1}^{15}\frac{f_{sai}+f_{sbi}+f_{sci}}{15} \quad (20)$$

where f_{sai} is the average switching frequency of the i^{th} switch in phase A.

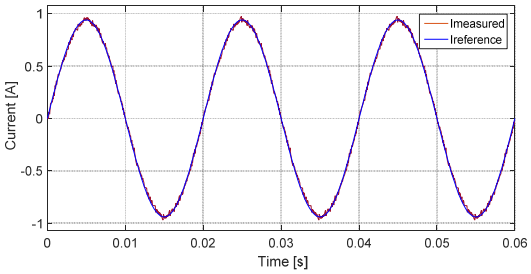
The mean absolute reference tracking error e(steady state error, SSE) is given by the difference in error in magnitude between the reference current and the measured current within m

$$e=\frac{1}{m}\sum_{k}^{m}\left|i^{*}\left(k\right)-i\ \left(k\right)\right| \quad (21)$$

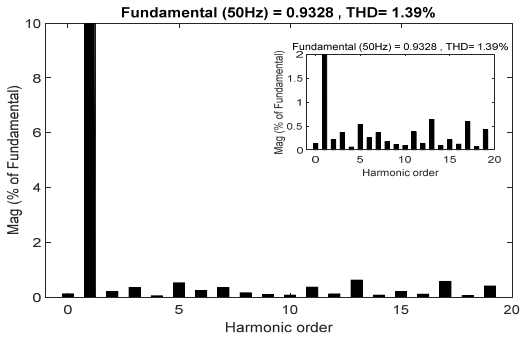
Where i*(k) is the reference current and i(k) is the measured current. Fig. 6 shows the load current of the inverter with FCS-MPC control utilizing the 61 vectors, and its corresponding Total Harmonic distortion (THD). It is found to be 2.19 % which is well below the IEEE standards. Fig. 8 shows the current in the 19 vector scheme having the THD as 1.39 %. Therefore the proposed scheme has 1% more THD than the conventional scheme. Table 2 gives the details of steady state parameters of the both FCS-MPC schemes for various sampling time. It is observed that the scheme with reduced switching frequency even though has the steady state parameters values to be approximately 50 % more, they are well within IEEE standards. It is also observed that the for the proposed

Table 2. Comparison of steady state parameters with different sampling times

	FCS-MPC with reduced switching frequency			FCS-MPC without reduced switching frequency		
Steady state parameters	25us	50us	100us	25us	50us	100us
teady state error	0.002	0.0035	0.006	0.001	0.002	0.0041
%THD	2.12	3.08	5.39	1.15	2.42	5.00
Switching frequency	5522	3388	1492	11680	5854	2221



(a)



(b)

Fig. 7. (a) Load current; (b) Harmonic spectrum of the five level inverter in 61 vector scheme

scheme the average switching frequency is reduced to 50% for all the sampling time.

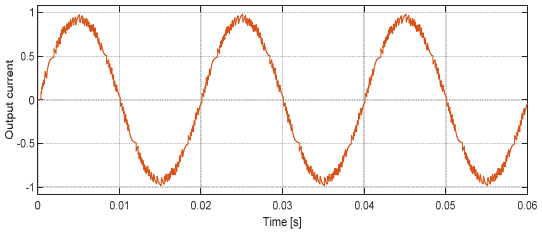
Fig. 9 Phase A load voltage the proposed FCS-MPC five level inverter with 19 voltage vector scheme. The THD is found to be 24.63% and can be further reduced by connecting a filter.

Fig. 10 and 11 shows 19 voltage vectors and 61 voltage vectors respectively. From these figures we can see that all the vectors are used in both the cases.

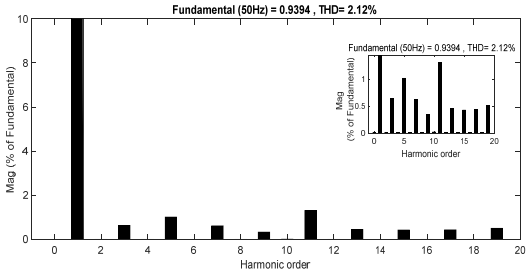
While analyzing we can see that 19 vectors scheme utilization is more effective and through.61 scheme on the other hand shows the utilization of each vectors is minimal

6.2 Dynamic control performance

The performance of the controller for a step in the amplitude of the reference current is shown in Fig. 12. This procedure is done for 61 voltage vector scheme as well as 19 voltage vector scheme. On examining both methods, it



(a)



(b)

Fig. 8. (a) Load current; (b) Harmonic spectrum of the five level inverter in 19 vector scheme

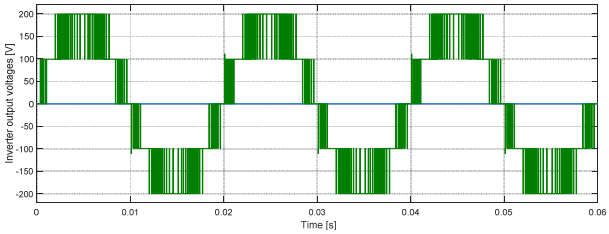


Fig. 9. Phase voltage for the FSMPC technique

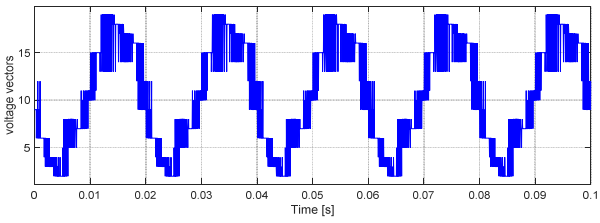


Fig. 10. 19 voltage vectors for the FSMPC technique

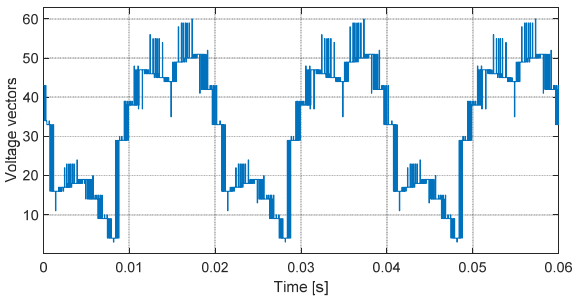
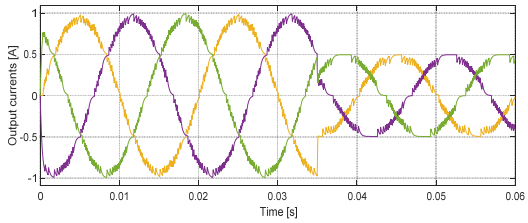
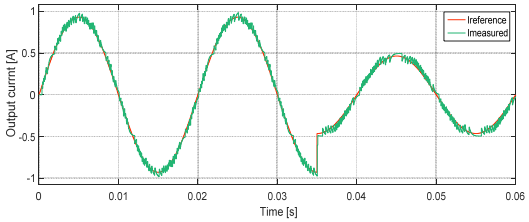


Fig. 11. 61 voltage vectors for the FSMPC technique

is seen that, both the scheme has good reference tracking. Here the reference current is decreased from 1 to 0.5A at

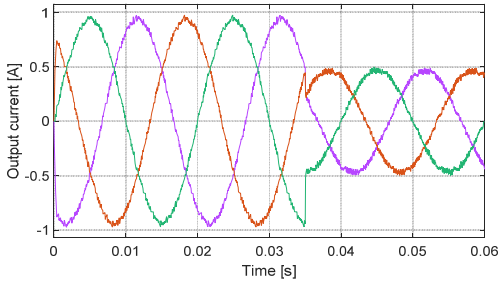


(a)

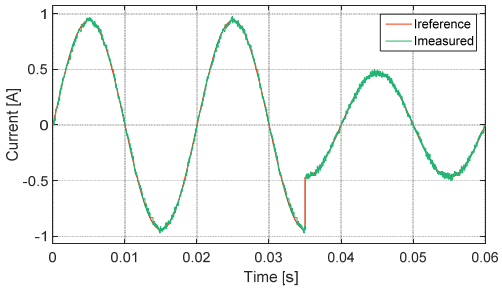


(b)

Fig. 12. (a) Three phase load current for 19 vector scheme; (b) Load current compared with reference with dynamic change at 0.035 seconds



(a)



(b)

Fig. 13. (a) Three phase load current for 19 vector scheme; (b) Load current compared with reference with dynamic change at 0.035 seconds

0.035s

Fig. 14 shows the phase voltage of the inverter for identical conditions.at 0.03s. When the magnitude of the current decreases, there is a corresponding decrease in the voltage magnitude. So, 50% of current reduction causes 50% reduction in the voltage. This result is especially shown to describe the excellent response of the inverter to the dynamic change i.e. while there is change in load current dynamically there is dynamic change in voltage as well.

Table 3. List of components required for the experimental setup

S.No	Component	Specifications
1	DC link Voltge	30V
2	MOSFET	IRF540
3	Diode	RTF20
4	Resistor	100ohm
5	Inductor	48mH
6	Opto-coupler	TLP 250
7	dSPACE	1103
8	PQ Box	PQ 200
9	Load voltage V_{RMS}	57V
10	Load current	0.420A
11	Three phase power P_{OUT}	40W

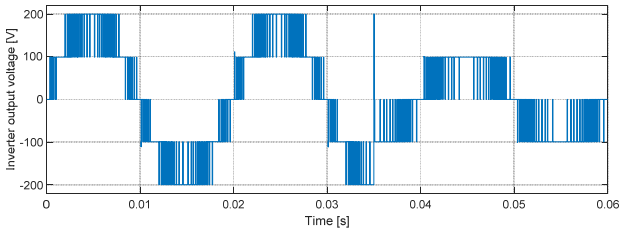


Fig. 14. Phase voltage with dynamic change at 0.035 seconds

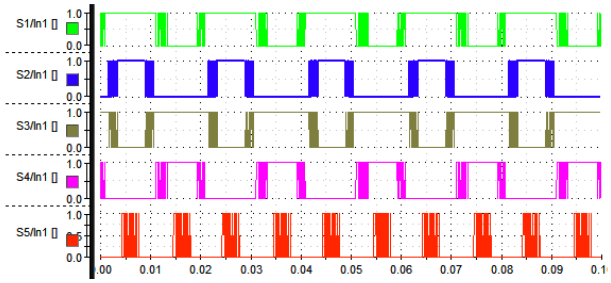


Fig. 15. Experimental results: Switching pulses to the inverter.

6.3 Experimental results

Implementation of this inverter topology is carried out using dSPACE DS1103. By interfacing MATLAB/Simulink model to the inverter circuit by using dSPACE we could generate gating signals for the inverter. The gating signals for a one phase taken from the Digital I/O ports of the dSPACE DS1103 are shown in Fig. 15. The list of components used for the experimental setup is given in Table 3.

In this test, balanced RL load is considered. The resistance and inductor values of 100Ω and 48mH is used for the power factor of 0.98 lagging.

Since the comparative analysis between 61 vector

Fig. 16. Experimental setup showing the inverter with load driven by dSPACE 1103

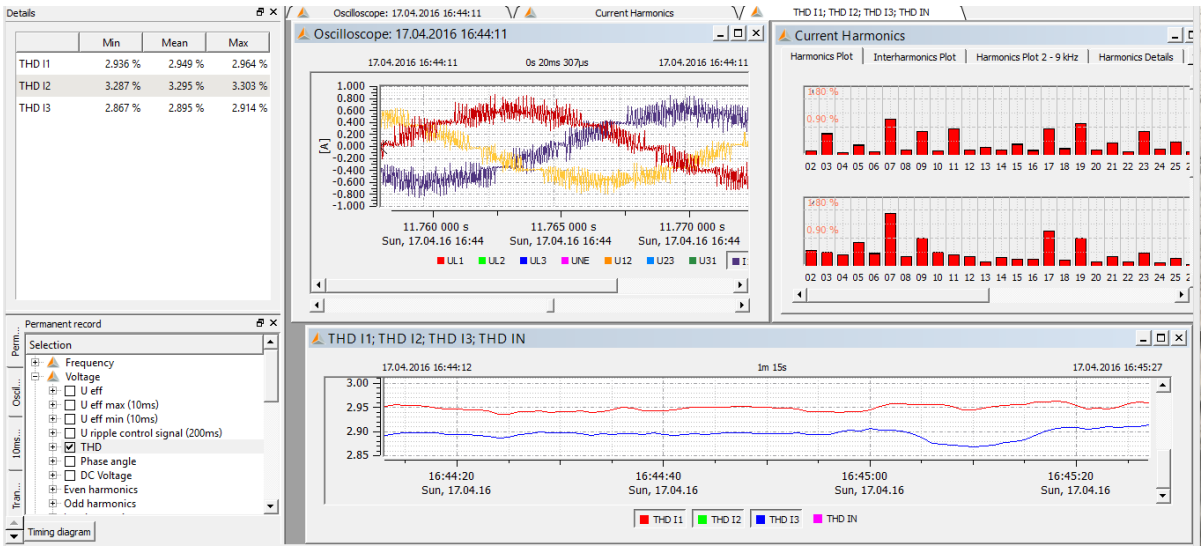


Fig. 17. Three phase load current and its THD analysis

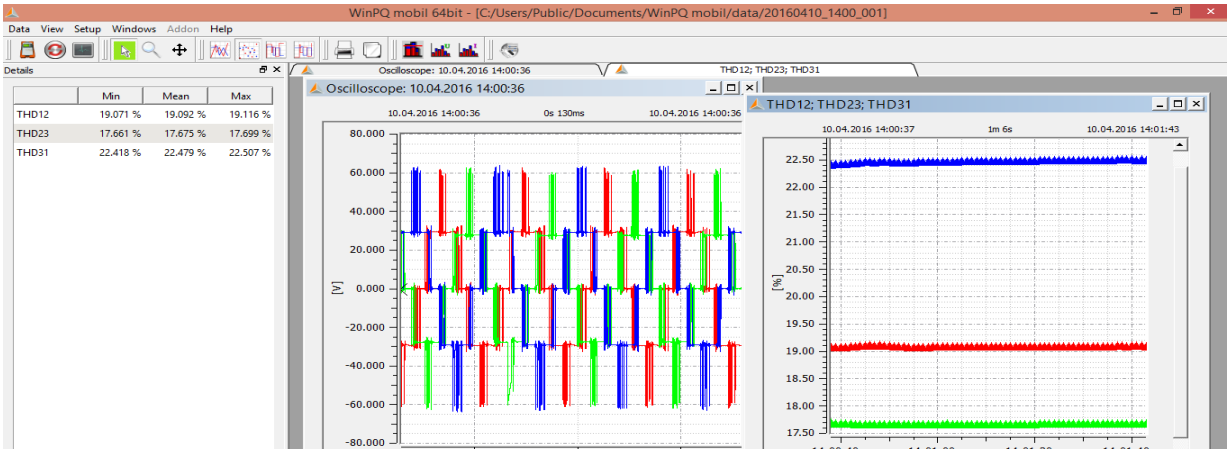


Fig. 18. Three Phase Load Voltage and its THD of the inverter

method and 19 vector method is already done in simulation, and its effectiveness already proved, the implementation is done only for 19 vectors. This FCS-MPC technique uses only 19 voltage vectors for the current control. The implementation results shows that the FCS-MPC scheme utilizing 19 voltage vector works well

Fig. 16 shows the experimental setup consisting of the Inverter, dSPACE1103, the loads and the PQ box with various voltage and current sensors. Fig. 17 shows the three phase currents and its THD.

It can be noted that the current THD for all the three phases are 3% which is 1% more than the simulation but

well within IEEE 519 standards. Fig. 18 shows the phase voltage and its THD showing approximately 22% like the simulation. It can be further reduced with filters are used in the load voltage.

7. Conclusion

In this paper, a FCS-MPC for a five level CMLI with reduced switch topology is proposed. Only five switches are used here instead of conventionally used eight switches. The main contribution of this paper is to make the MPC controller work for the reduced switch topology using only 31% of the non-redundant voltage vectors, thereby excluding 68% of other voltage vectors. This simplifies the execution of the MPC algorithm, paving a way for significant reduction in the computational time. This controller makes use of the excellent ability of MPC to multitask, by adding one more objective which is to reduce the average switching frequency in addition to controlling the load current. This is especially important, since switching losses and therefore switching frequency is significant for high-power applications. The trade-off of this MPC is that the current is distorted, but well within the limits of IEEE standards. However for this scheme the average switching frequency is reduced to 50% for all the sampling time. The results shown prove that this MPC works well in steady state and dynamic conditions too. This work will be extended in future by replacing the input DC sources by solar PV sources.

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