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Design Guidelines for a Capacitive Wireless Power Transfer System with Input/Output Matching Transformers

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Abstract – A capacitive wireless power transfer (C-WPT) system uses an electric field to transmit power through a physical isolation barrier which forms a pair of ac link capacitors between the metal plates. However, the physical dimension and low dielectric constant of the interface medium severely limit the effective link capacitance to a level comparable to the main switch output capacitance of the transmitting circuit, which thus narrows the soft-switching range in the light load condition. Moreover, by fundamental limit analysis, it can be proved that such a low link capacitance increases operating frequency and capacitor voltage stress in the full load condition. In order to handle these problems, this paper investigates optimal design of double matching transformer networks for C-WPT. Using mathematical analysis with fundamental harmonic approximation, a design guideline is presented to avoid unnecessarily high frequency operation, to suppress the voltage stress on the link capacitors, and to achieve wide ZVS range even with low link capacitance. Simulation and hardware implementation are performed on a 5-W prototype system equipped with a 256-pF link capacitance and a 200-pF switch output capacitance. Results show that the proposed scheme ensures zero-voltage-switching from full load to 10% load, and the switching frequency and the link capacitor voltage stress are kept below 250 kHz and 452 V, respectively, in the full load condition.

Keywords: Wireless power transfer, Capacitive coupling, Matching network, Zero voltage switching (ZVS)

1. Introduction

A capacitive wireless power transfer (C-WPT) system uses an electric field instead of a magnetic field for energy transmission through the isolation barrier [1]. It consists of a transmitting unit with a pair of transmitting conductors and a receiving unit with a pair of receiving conductors. A combination of conductors separated by a gap forms link capacitors whose mechanical structure is simpler than coil windings in conventional inductive wireless power transfer (I-WPT) system. Moreover, flux is confined within the volume enclosed by conductors and thus less EMI problems to nearby human body are experienced.

However, despite these advantages, the major limitations of C-WPT are usually caused by low link capacitance value. It is reported that a ¼-mm air gap provides only 3.5 pF/cm^2. Moreover, because there should be a return path, the effective link capacitance is a series connection of the two individual link capacitors, and thus it becomes much lower. With regard to it, trade-off between the available link capacitance and obtainable efficiency for a desired power have been studied in [2], especially with a MHz operating frequency.

Therefore, the circuit designer for C-WPT should consider the following challenges it presents. First, low capacitance degrades the power factor in the transmitting circuit. Secondly, low capacitance increases voltage stress and switching frequency to process a given output power. A high voltage on the link structure may cause a breakdown of the isolation barrier or shock hazard problem for users and unnecessarily high operating frequency is sometimes undesirable because of cost and technology limitation in gate drivers and power switches. Thirdly, if the effective link capacitance is as small as the main switch output capacitance, the soft switching region shrinks and the zero voltage switching (ZVS) feature of the resonant operation may be lost [3].

To tackle these problems, a series inductor is introduced to cancel out the capacitance and achieve ZVS condition [3]. However, the operating frequency becomes relatively too high and the voltage stress was not discussed fully in this literature. Another scheme adding L-C-L-type matching filters in the front-end and back-end of link capacitors increases power factor and handles more output power without increasing the operating frequency [4,5,6], but additional five resonant components – three inductors and two capacitors – should be designed, and the design procedure based on iterative process are too complex.

Among various matching scheme, double matching transformer scheme proposed by [7] is a viable solution because of its simplicity and superior performance. Its feasibility has been verified and tested in [8] and [9], but design guideline considering voltage stress, operating

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frequency, and ZVS condition has not been studied yet.

In this paper, as an effective driving method for a C-WPT system with low link capacitance, a half-bridge structure with double matching transformers is analyzed and the optimal matching condition achieving wide ZVS range, avoiding unnecessarily high frequency operation, and suppressing the voltage stress on the energy link capacitor is investigated thoroughly.

2. Design Equations

2.1 Topology overview

Fig. 1 shows a half-bridge converter with two matching transformers. While the basic operation is similar to the conventional series resonant converter, the transformers inserted into the front and rear sides of the link capacitors have dedicated functions: while the input matching transformer, TX1, widens ZVS range, the output matching transformer, TX2, increases the power factor and loosens the fundamental limit which will be further discussed later. Hence, the optimal design of matching network is critical to the overall performance of the C-WPT system. The key design equations will be derived herein.

2.2 Output voltage gain

For the analysis of operation, the normalized DC voltage gain is defined as

$$M = \frac{N_2 V_o}{N_1 V_g}(1+\gamma) \tag{1}$$

where V_o is the DC output voltage, V_g (=V_S/m) is the input voltage (m=2 for half-bridge), N_1 and N_2 are the individual turn ratios of the input and the output matching transformer, and γ (=nV_F/V_o) is the rectifier voltage drop factor (n=2 for full-wave).

The normalized operating frequency and resonant angular frequency are also defined by

$$F = \frac{\omega}{\omega_O} = \frac{f}{f_O} \tag{2}$$

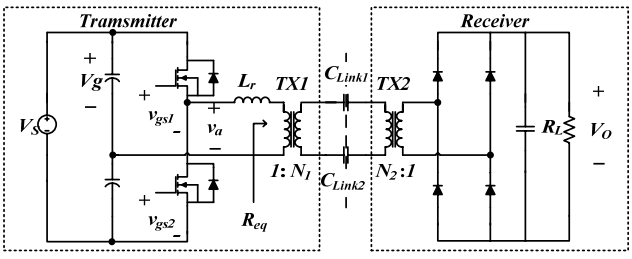


Fig. 1. C-WPT system with double matching transformers

and

$$\omega_O = \frac{1}{\sqrt{N_1^2 L_r C_e}} \tag{3}$$

where L_r is the resonant inductor and C_e is the effective capacitance given by

$$Z_o = \sqrt{\frac{L_r}{N_1^2 C_e}} \tag{4}$$

If every parameter is reflected into the switch side, the driving voltage source is a square pulse with a peak to peak value of V_S (=$2V_g$) and an operating frequency of ω (= $2\pi f$). Assuming that the resonant quality factor is sufficiently high, and that the operating frequency is always higher than the resonant frequency, the current through the resonant inductor can be regarded by a sinusoidal waveform, and a fundamental harmonic approximation (FHA) is possible [10]. If the output filter capacitance, C_o, is very large, the output voltage can be considered to be a stiff voltage source and its reflection into the switch is in phase with the current due to the diode action of the rectifier stage. If the characteristic impedance of the resonant network seen from the switch side are defined by

$$Z_o = \sqrt{\frac{L_r}{N_1^2 C_e}} \tag{5}$$

the quality factor of the resonant tank can be represented as

$$Q_e = \frac{Z_o}{R_{eq}} \tag{6}$$

where the ac equivalent load resistance reflected into the inverter, R_{eq}, is calculated as

$$R_{eq} = \left(\frac{N_2}{N_1}\right)^2 \frac{8}{\pi^2}(1+\gamma)R_L \tag{7}$$

By applying FHA to the reflected circuit, the normalized DC voltage gain relation results in

$$M = \frac{1}{\sqrt{1+Q_e^2\left(F-\frac{1}{F}\right)^2}} \tag{8}$$

With a valid range of F≥1 (above resonance operation) and 0<M≤1, F can be rearranged as follows:

$$F = \frac{1}{2Q_e}\sqrt{\frac{1}{M^2}-1} + \frac{1}{2}\sqrt{\frac{1}{Q_e^2}\left(\frac{1}{M^2}-1\right)+4} \tag{9}$$

Eq. (9) says that in order to regulate the constant output voltage by frequency control, the normalized operating frequency should be controlled to make the DC voltage gain constant. That is, F becomes minimum in the full load and maximum in the light load.

2.3 Zero voltage switching condition

The series resonant LC tank can provide a ZVS feature to the main MOSFET switches when it is driven in the above resonance region. To achieve the zero voltage turn-on of the main MOSFET switch, the charge circulated during the commutation should be large enough to clear off the charge stored in the drain-source of switching MOSFETs. In other words, the ZVS condition is

$$q_{TANK} \geq q_{SW} \tag{10}$$

where q_{TANK} denotes the circulating charge in the resonant tank, and q_{SW} is the stored charge in the switch output capacitance at the turn-on instant.

The switch output capacitance, C_{oss}, is a pn-junction depletion capacitance with a non-linear voltage dependency, and thus the equivalent linear capacitance in the full excursion of the drain to source voltage can be obtained as

$$C_{sw} = \frac{1}{V_S}\int_0^{V_S} C_{oss}(v_{DS})dv_{DS} = 2C_{oss}\big|_{v_{DS}=V_S} \tag{11}$$

Since both of the switch output capacitances are involved at the same time in half-bridge topology, the total charge is calculated by

$$q_{SW} = 2C_{sw}V_S = 4C_{sw}V_g \tag{12}$$

Subsequently, assume the fundamental component of the driving voltage, V_a, is given by

$$v_{a1}(t) = V_{am}\cos\omega t \tag{13}$$

the current through the resonant tank can be regarded as

$$i_L(t) = I_{Lm}\cos(\omega t - \varphi) \tag{14}$$

where φ is the phase angle. If we define the input impedance, $Z_i(\omega)$, looking into the resonant tank from the half-bridge switch, the phase of the input impedance is obtained by

$$\tan\varphi(\omega) = Q_e\left(F - \frac{1}{F}\right) \tag{15}$$

In this situation, the circulating charge is calculated using the timing diagram in Fig. 2. Assuming the duty

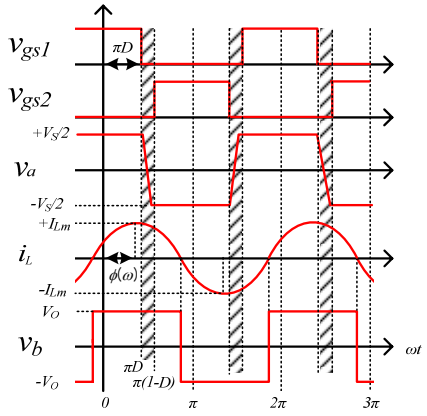


Fig. 2. Approximate waveforms for ZVS analysis

cycle of the half-bridge inverter as D, the integration of the inductor current in shaded dead-time duration represents the charge displacement to provide soft-switching. By integrating the current from the turn-off instance of one switch to the turn-on instant of the other switch, q_{TANK} is obtained as

$$q_{TANK} = \frac{1}{\omega}\int_{\pi D}^{\pi(1-D)} i_L(\theta)d\theta = \frac{1}{\omega}2I_{Lm}\sin\varphi(\omega)\cos\pi D \tag{16}$$

Therefore, the ZVS condition in (12) is then

$$N_1^2 \geq \frac{\kappa}{\kappa_{op}} \tag{17}$$

where κ is the capacitance ratio of the switch parasitic to effective link capacitance :

$$\kappa \equiv \frac{C_{sw}}{C_e} \tag{18}$$

and κ_{op} is a function of the operating point defined by

$$\kappa_{op} \equiv \frac{2}{\pi}\frac{(1-M^2)}{F^2}\cos\pi D \tag{19}$$

Eq. (17) shows that ZVS range becomes narrow with low effective capacitance value. In other words, the input matching transformer widens ZVS range by designing the turn ratio N1 larger than unity. In the design process, if M is chosen to be near unity, a high value of N1 is required to achieve ZVS function. It should also be noted that the worst case ZVS condition occurs in the light load condition where F has its maximum value.

Arranging (17), (18), and (19), the minimum turn-ratio, N1,min, determines the ZVS boundary as follows:

$$N_{1,\min} = \sqrt{\frac{\kappa}{\kappa_{op}}} \tag{20}$$

That is, ZVS is successfully achieved when N1 is designed to be larger than $N_{1,min}$, or equivalently when N2 is larger than $N_{2,min}$.

$$N_{2,\min} = N_{1\min}\frac{V_o M}{V_g(1+\gamma)} \tag{21}$$

2.4 Voltage stress in the effective link capacitor

In a capacitive energy transfer system, it is very important to consider the breakdown voltage of the isolation barrier within the link capacitors. The voltage stress on the effective capacitance, V_{Cm}, can be obtained using the law of conservation of charge. Through the voltage swing from $-V_{Cm}$ to $+V_{Cm}$, the total charge displaced by the resonant current is

$$q = C_e \cdot 2V_{Cm} \tag{22}$$

Besides, the output current is simply the rectified average value of the resonant current. Therefore, the output current is

$$I_O = N_2\frac{2}{T}\int_{half\ period}|i_{C_e}(t)|dt = N_2\frac{2q}{T} \tag{23}$$

where T is the switching period. Equating (22) and (23) to eliminate q, we obtain

$$V_{Cm} = \frac{1}{4}\frac{I_O}{N_2}\frac{T}{C_e} \tag{24}$$

and eliminating the period results in the following compact form:

$$V_{Cm} = \frac{4}{\pi}\frac{Q_e}{F}N_2 V_O \tag{25}$$

The voltage stress in the effective link capacitor is proportional to the turn-ratio, N2, of the output matching transformer and the ratio of Q_e to F. Hence, the worst case condition occurs under heavy load: the maximum Q_e and the minimum F.

2.5 Current stress in the switch

Because the output current is simply the rectified average value of the switch current reflected into the load side, the current stress is

$$I_{Lm} = \frac{\pi}{2}\frac{(1+\gamma)}{M}\frac{V_o I_o}{V_g} \tag{26}$$

This equation states that the switch current is inversely proportional to M. In order to minimize it, M should be chosen as large as possible in the design process.

3. Design Guideline

The design procedure is to find the optimal matching transformer turn ratios, N_1, and N_2 in order to achieve wide ZVS range, to avoid unnecessarily high frequency operation, and to suppress the voltage stress on the energy link capacitor. Because most of design equations are dependent on the normalized dc voltage gain, M, which is directly proportional to the ratio of N_2 to N_1, it is convenient to adopt N_2 vs. M plane as a design space.

With fixed N_2/N_1 ratio or equivalently fixed M, higher N_2 provides wider ZVS range, whereas it may cause excessive voltage stress. On the other hand, when M is approaching unity, the current stress decreases as is clear from (26), but ZVS is hard to achieve without increased voltage stress. Therefore, there are design trade-offs among ZVS condition, the capacitor voltage stress, and the current stress.

Furthermore, since it is known that a resonant quality factor larger than unity guarantees the validity of the FHA, the condition $Q_{e,min}$=1 can be regarded as another design constraint and thus $Q_{e,max}$ is calculated from the ratio of the minimum and the maximum load current.

The following summarizes the design procedure and it is graphically shown in Fig. 3.

Step 1: Assume Qe,min=1, determine Qe,max from the required load range.
Step 2: Under Qe,max, plot the voltage stress curves using (9) and (25) in the N2 vs. M plane. Choose the acceptable region using the curve.
Step 3: Plot the curve of ZVS boundary using (9) and (21) under Qe,min. The upper area of this boundary represents the ZVS region.
Step 4: Choose the intersection point as the optimal design point. This point minimizes the switch current in the valid region.

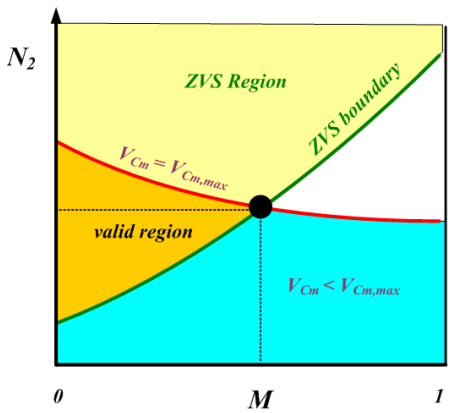


Fig. 3. Design curve in the N_2-M plane

Step 5: Calculate N1 and Lr by (1) and (5) to complete the design process.

3.2 Design example

In order to verify the analysis and the design process, a prototype design has been performed with a 5-W C-WPT system (V_s= 19V and V_o= 10V). Its load current range was from 50 mA to 500 mA.

3.2.1 Energy coupler structure

It consists of two pairs of plates having a 10 cm x 10 cm width and height, with a 0.2-mm gap filled with insulation tape (ε_r = 3). The measured capacitance values of the link capacitors were 500 pF and 526 pF, respectively, which together made the effective link capacitance Ce=256 pF.

3.2.2 Power stage design

To calculate the ZVS condition, the equivalent linear capacitance of C_{sw}=400 pF was pre-calculated by (11) using the datasheet value of the main MOSFET switch (FQPF20N60, 60 V/15 A). As was predicted in (17), the capacitance ratio, κ, is as small as 1.6 and thus appropriate design of N_1 and N_2 was important for ZVS operation.

Fig. 4 shows the design curve of N_2 vs. M plotting voltage stresses. The red broken line indicates the boundary of ZVS operation. The V_{Cm} is dependent on M, and the slope changes from steep to gentle as M increases. The curve also shows that $N_{2,min}$ increases dramatically near unity value of M, as mentioned before.

By choosing V_{Cm}=450 V, the design point (M,N_2) = (0.5,3.9) was obtained according to the design guideline.

Subsequently, N_1=9.03 and L_r=23.1 μH were calculated. The design equation predicted the maximum voltage stress on the effective capacitor as 455 V, the maximum inductor current stress as 1.82 A, and the operating frequency as 249.7 kHz under the full load condition. Under 10% of the full load, the switching frequency increased to 501.5 kHz.

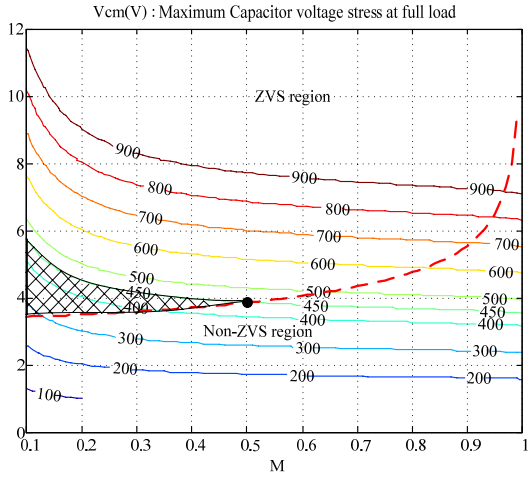


Fig. 4. Design example (V_g=9.5, V_o=10,V_F=0.5 D=0.45)

3.2.3 Resonant inductor design

L_r was designed using the area product equation,

$$A_C A_w = \frac{LI_{\max} I_{rms}}{B_{max} k_W J_{rms}} \tag{27}$$

where B_{max} is the maximum magnetic flux density, kw is the winding fill factor, and J_{rms} is the current density. Considering the core loss density below 100mW/cm^2, we selected B_{max}=0.06T. For the coil winding, typical values have been used such as k_w=0.6, J_{rms}= 500A/cm^2. For L_r=23.1 μH, and I_{rms}=1.28A with sinusoidal inductor current waveform, EI3026S (A_C=109mm^2, A_w=80mm^2) and 0.06mm/200 Litz wire were adopted and the number of turn and the air-gap were calculated as 6 and 200um, respectively.

3.2.4 Matching transformer design

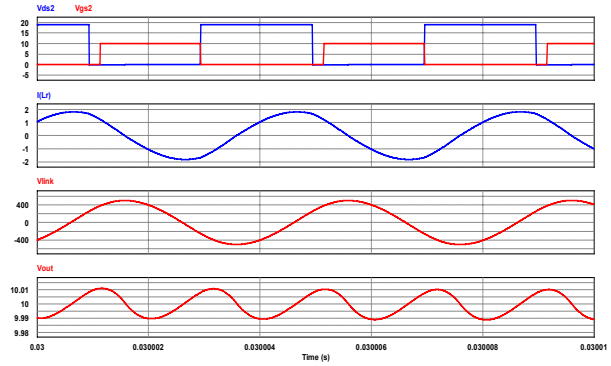
Matching transformers, TX1 and TX2 were designed using the area product equation,

$$A_C A_w = \frac{V_{p,rms} I_{p,rms} + V_{s,rms} I_{s,rms}}{4.44 B_{max} f k_W J_{rms}} \tag{28}$$

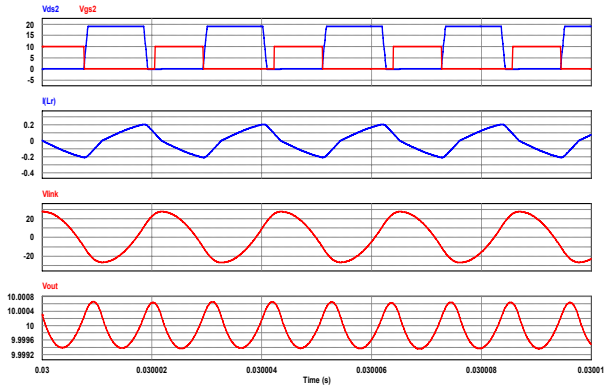
where the numerator comprises of the sum of every apparent power applied to windings of the matching transformers. For TX1 with $I_{p,rms}$ = 1.25A and $V_{p,rms}$ = 42V, EI4035S (A_C = 147mm^2, A_w=166mm^2) for magnetic core and 0.06mm/200 Litz wire for winding were adopted and the numbers of turns were selected as 14T/127T. Similarly for TX2, EE2519S (A_C = 40.4mm^2, A_w = 80.3mm^2) for magnetic core and 0.06 mm/20 Litz wire for winding were selected, respectively. The number of turns was designed to be 33T/8.5T.

3.3 Simulation

To verify the performance, the design values were put into PSIM circuit simulation software. The two power switches were modeled by an ideal MOSFET in parallel with an ideal diode and a linear equivalent switch capacitor of 400 pF. The gate driver dead-time was set to 200 nsec. Fig. 5(a) shows the simulation waveforms under the full load condition: the switching frequency is 249.3 kHz, the estimated voltage stress in the effective link capacitor is 504 V, and the maximum inductor current is 1.81 A. The drain to source voltage of the low-side switch, V_{ds2}, remains zero before the rising of the gate signal, V_{gs2}, and thus zero voltage turn-on has been successfully achieved in each switch. Fig. 5(b) shows the simulation waveforms under 10% load condition: the switching frequency is 460.7 kHz, the estimated voltage stress in the effective link



(a)



(b)

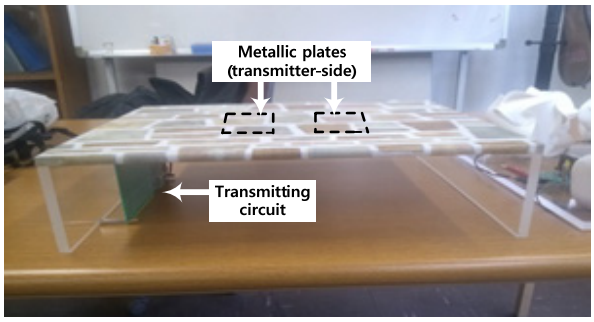
Fig. 5. Simulation waveforms: (a) full load (R_L=20 Ω); (b) 10% load (R_L=200 Ω)

capacitor is 50 V, and the maximum inductor current is 0.205 A.

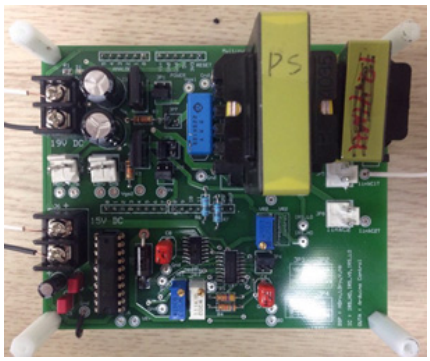
In both cases, the output voltage was regulated to 10 V. Furthermore, the drain to source voltage waveform of the low side MOSFET shows smooth transition during the dead time, and thus verifies that the ZVS operation at the instant of switch turn-on has been successfully achieved. The only discrepancy from the theoretical value was the 10% decrease in the maximum switching frequency under the light load condition. Fig. 5(b) shows that the resonant current is slightly distorted under the light load, which caused an error in the FHA adopted in the theoretical analysis.

3.4 Hardware implementation

Figure 6 is a photograph of the hardware implementation of the C-WPT system. The primary plates of the link capacitors were merged into the energizing table in Fig. 6(a) with a horizontal clearance of 4 cm. The transmitter board consisted of an inverter and an input matching transformer. A receiving unit which containing secondary plates of link capacitors, an output matching network, and a rectifier was mounted on the table covered with insulation paper of 0.2 mm in thickness.



(a)

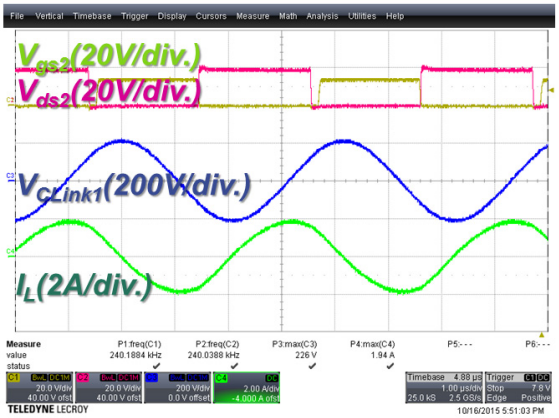


(b)

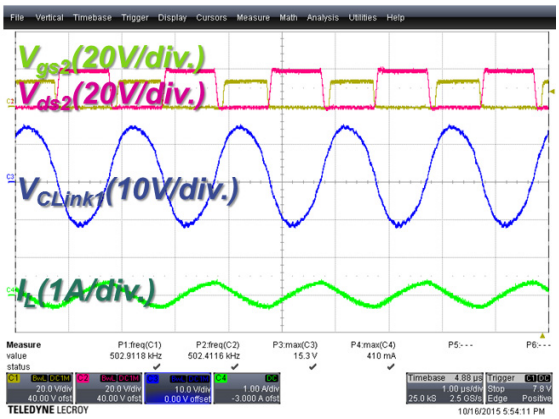
Fig. 6. Photograph of the hardware: (a) energy link capacitors; (b) transmitter circuit

In the inverter stage in Fig. 6(b), the main switches were n-channel MOSFETs and the gate driver was IRS21864 with a dead time setting of 200 nsec. In the rectifier stage, four Schottky diodes (STPS5L40, 40V/5A) implemented a full-wave rectifier, and the output capacitor was a 10-μF electrolytic capacitor. For the magnetic components, TX1 is wound on EI4035S (Samwha, PL7 ferrite) with 14T:127T, and TX2 on EE2519S with 33T:8.5T. Series inductor was constructed on EE3026 with 6T and 200um airgap, which was measured as 17.9 μH. The frequency control IC, NCP1395B, implemented the frequency control through the infrared(IR) link between the transmitter side and receiver side.

Fig. 7 shows the hardware test waveforms under the full and light load conditions. It presents the gate-to-source voltage of the high and the low side MOSFETs, the drain-to-source voltage of the low side switch, and the inductor current waveforms. In the full load, the capacitor voltage stress on each link capacitor was about 226V, or equivalently 452V for the effective capacitor. The maximum switch current was 1.94A and the overall efficiency from dc input to dc output was 73.4% (5.0W/6.8W). In 10% load condition, the switching frequency was 503 kHz, and the voltage stress on each link capacitor was 15.3V, or equivalently 31V for the effective capacitor. The efficiency was about 67.6% (0.50W/0.74W). The hardware waveforms also show that the ZVS condition has been



(a)



(b)

Fig. 7. Hardware waveforms: (a) full load (R_L=20 Ω); (b) 10% load (R_L=200 Ω)

achieved from full load to 10% load.

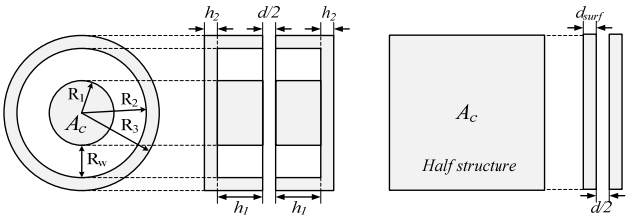
4. Further Discussions

The proposed design guideline provides the optimal design of the input/output matching transformers. For the same target specification with the same operating frequency of 250kHz, the conventional L-C-L matching network in [4,5,6] are designed and the results are compared with the proposed one in Table 1. It is clear that the proposed method reduces the size as well as the number of the resonant components.

Besides, in industrial applications with a stable gap separation distance, such as rotary joints [11,12] or rail tracers, most circuitry can be placed separately from the coupling structure and thus the required volume of the coupling structure with a given handling power is of major concern. Despite the existing duality between two different wireless power technologies, I-WPT and C-WPT, energy coupling mechanism is very different as shown in Fig. 8, and thus it is difficult to conclude the superiority of one

Table 1. Comparisons of resonant components

Topology		Conventional	Proposed
$L_1(L_r)$	A.P. (mm^4)	24402	8250
	Vol. (mm^3)	11390	6210
$L_2(TX_1)$	A.P. (mm^4)	13362	24402
	Vol. (mm^3)	6880	11390
$L_3(TX_2)$	A.P. (mm^4)	24402	3244
	Vol. (mm^3)	11390	1940
C_1	V_{max} (V)	428	N.A.
	I_{max} (A)	1.23	
C_3	V_{max} (V)	264	
	I_{max} (A)	1.8	



(a) (b)

Fig. 8. Energy link structure: (a) I-WPT; (b) C-WPT

method to the other with a hardware experiments.

Instead, it is possible to predict the limiting performance of the two methods by theoretical calculations. According to mathematical formula used in [13], the inductive handling power and the volume of the magnetic coupler structure in Fig. 8 (a) can be estimated by

$$Q_{I-WPT} = \frac{\pi f B_{\max}^2}{\mu} dA_C \tag{29}$$

$$V_{I-WPT} = \left(2h_1 + 2h_2 + \frac{d}{2}\right)\left(2A_C + \pi(R_2^2 - R_1^2)\right) \tag{30}$$

Whereas, the capacitive power and the volume of the capacitive coupler structure in Fig. 8 (b) can be given by

$$Q_{C-WPT} = \pi f \varepsilon E_{\max}^2 dA_C \tag{31}$$

$$V_{C-WPT} = (d + 4d_{surf})A_C \tag{32}$$

Assuming the maximum allowable conditions for the field quantities (B_{max}=0.2T, E_{max}=3MV/m, J_{max}=5MA/m^2) with the same energy link dimension such as the field area (A_C=10cm x 10cm), a small distance (d/2=0.1mm), and air medium. An operating frequency of 250 kHz makes $Q_{I\text{-}WPT}$=5.00x104VA/m^2 and $Q_{C\text{-}WPT}$=1.25x10^2 VA/m^2, but the coupler volumes are calculated as $V_{I\text{-}WPT}$=1.55x$10^{-3}$$m^3$ and $V_{C\text{-}WPT}$=2.43x$10^{-6}$$m^3$. This means that the capable power density of the coupler structure in C-WPT is almost 1.5 times larger. Therefore, it can be concluded that C-WPT can be more space-efficient than I-WPT. This is in accordance with the results of the comparative study in [13] : for small separation gap applications (d<1mm), C-

WPT has the higher power handling per unit volume of coupling structure, whereas I-WPT has the advantage over the C-WPT method for large gaps (d>1mm).

5. Conclusion

In this paper, as a viable circuit topology for a capacitive power transfer system with low link capacitance, double matching transformer scheme has been investigated. Design equations have been derived and its fundamental limit has been discussed. The optimal design procedure for the matching structure also has been proposed to achieve the ZVS condition with reduced capacitor voltage and operating frequency. For verification, a 5-W system equipped with an effective link capacitance of 256 pF and switch output capacitance of 200 pF has been designed. It operates in ZVS from full load to 10% load, and the switching frequency and the link capacitor voltage stress are kept below 250 kHz and 452 V in the full load condition. In the conclusion, simulation and hardware have successfully verified the analysis and the design procedure.

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