Accurate Tunable-Gain 1/*x* Circuit Using Capacitor Charging Scheme

Byung-Do Yang and Seo Weon Heo

This paper proposes an accurate tunable-gain 1/*x* circuit. The output voltage of the 1/*x* circuit is generated by using a capacitor charging time that is inversely proportional to the input voltage. The output voltage is independent of the process parameters, because the output voltage depends on the ratios of the capacitors, resistors, and current mirrors. The voltage gain of the 1/*x* circuit is tuned by a 10-bit digital code. The 1/*x* circuit was fabricated using a 0.18 μm CMOS process. Its core area is 0.011 mm^2 (144 μm × 78 μm), and it consumes 278 μW at V_{DD} = 1.8 V and f_{CLK} = 1 MHz. Its error is within 1.7% at V_{IN} = 0.05 V to 1 V.

Keywords: 1 over *x*, analog divider, process independent, capacitor charging, tunable gain.

I. Introduction

The analog 1/*x* circuit is used in analog dividers, filters, fuzzy control, neural networks, and A/D converters [1]–[6]. Several circuits for the 1/*x* function have been proposed. A voltage-mode analog divider is accurate, but it needs a highly accurate wide-range voltage controlled oscillator [1]. A current-mode 1/*x* circuit using weak-inversion MOSFETs has low accuracy due to very low reference and input currents, which are only under a few nanoamperes [2]. A voltage-mode analog divider [3], voltage-mode 1/*x* circuit [4], and current-mode analog divider [5] have good accuracy; however, their outputs significantly change due to device parameters and temperature.

In this paper, an accurate tunable-gain 1/*x* circuit is proposed. The output voltage of the 1/*x* circuit is generated by using a capacitor charging time that is inversely proportional to the input voltage. The output voltage is independent of process parameters, because all variations from active and passive devices are canceled out. In addition, the voltage gain of the 1/*x* circuit is tuned by a 10-bit digital input code.

The rest of this paper is organized as follows. Section II describes the proposed tunable-gain 1/*x* circuit. Section III shows the measurement results of the fabricated chip. Finally, conclusions are drawn in Section IV.

II. Proposed 1/*x* Circuit

The proposed 1/*x* circuit generates an output voltage (V_{OUT}) that is inversely proportional to the input voltage (V_{IN}). Figures 1 and 2 show the schematic and operation of the 1/*x* circuit, respectively. Initially, the capacitor C_{SH1} samples and holds V_{IN} by the reset signal so that the voltage of C_{SH1} (V_{SH1}) is updated to V_{IN}. The reset signal also discharges the capacitors

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Byung-Do Yang (bdyang@cbnu.ac.kr) is with the Department of Electronics Engineering, Chungbuk National University, Cheongju, Rep. of Korea.

Seo Weon Heo (corresponding author, seoweon.heo@hongik.ac.kr) is with the School of Electronic & Electrical Engineering, Hongik University, Seoul, Rep. of Korea.

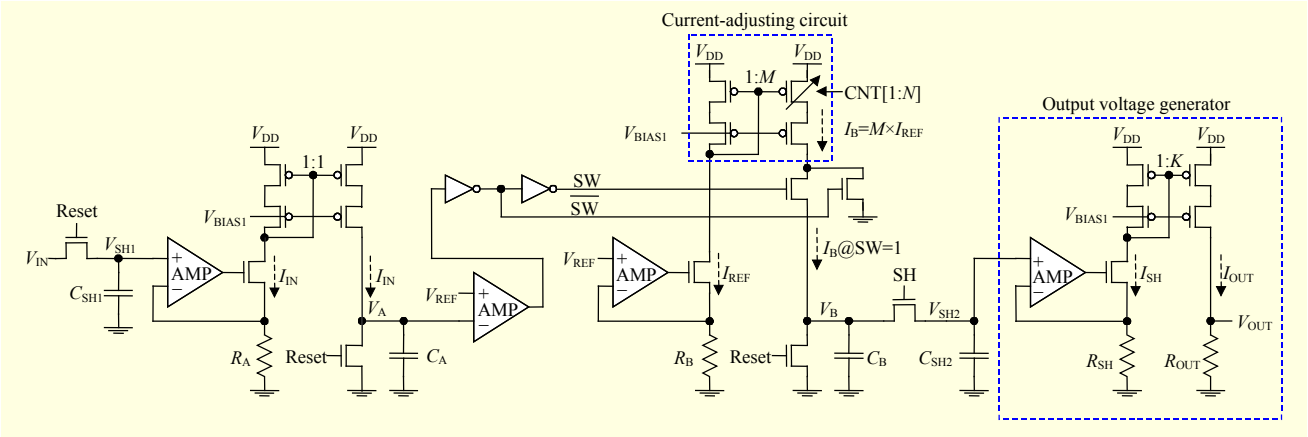

Fig. 1. Schematic of proposed 1/*x* circuit.

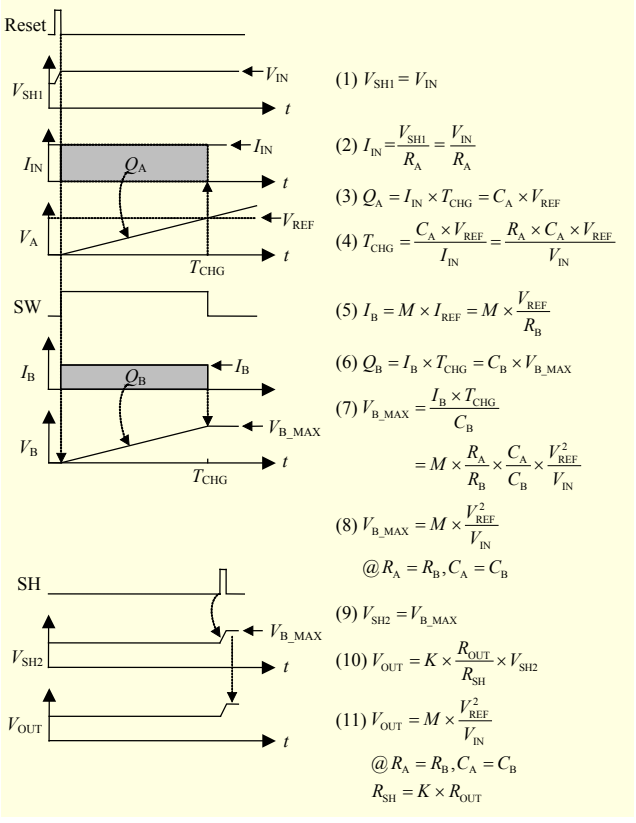

Fig. 2. Operation of proposed 1/*x* circuit.

C_A and C_B to the ground. The input voltage V_{IN} is converted to a current I_{IN} by an operational amplifier, a resistor R_A, and a current mirror. The current I_{IN} charges capacitor C_A during the capacitor charging time (T_{CHG}) until the voltage of C_A (V_A) reaches the reference voltage (V_{REF}). When $V_A = V_{REF}$, the charge stored in C_A ($Q_A = C_A \times V_{REF}$) is equal to the product of I_{IN} and T_{CHG}.

$$V_{SH1} = V_{IN}, \tag{1}$$

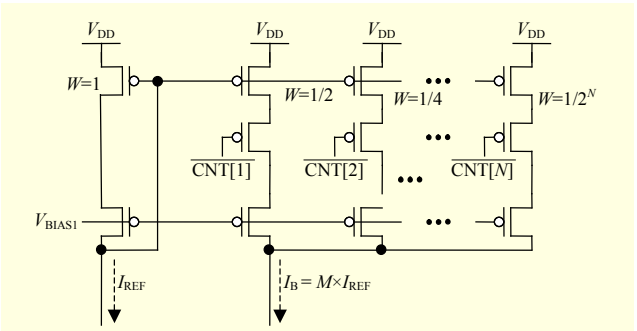

Fig. 3. Current-adjusting circuit.

$$I_{IN} = V_{SH1} / R_A = V_{IN} / R_A, \tag{2}$$

$$Q_A = C_A \times V_{REF} = I_{IN} \times T_{CHG}. \tag{3}$$

From equations (2) and (3), the capacitor charging time (T_{CHG}) is expressed as follows:

$$T_{CHG} = \frac{C_A \times V_{REF}}{I_{IN}} = \frac{R_A \times C_A \times V_{REF}}{V_{IN}}. \tag{4}$$

A reference current ($I_{REF} = V_{REF}/R_B$) is generated from the reference voltage (V_{REF}) by an operational amplifier and a resistor R_B. In the current-adjusting circuit in Fig. 3, the reference current (I_{REF}) is multiplied by M for a current I_B (= $M \times I_{REF}$) using a binary weighted current mirror and N-bit digital control code (CNT[1:N]).

$$I_B = M \times I_{REF} = M \times \frac{V_{REF}}{R_B}, \quad \text{where } M = \sum_{1}^{N} \frac{1}{2^K} \text{CNT}[K]. \tag{5}$$

During T_{CHG}, the switch (SW) turns on, and the current I_B charges capacitor C_B such that the charge stored in C_B ($Q_B = C_B \times V_{B\_MAX}$) becomes the product of I_B and T_{CHG}, where V_{B_MAX} is the maximum voltage of C_B after the capacitor charging operation.

$$Q_B = I_B \times T_{CHG} = C_B \times V_{B\_MAX}. \quad (6)$$

From equations (4), (5), and (6), V_{B_MAX} is expressed as follows:

$$V_{B\_MAX} = \frac{I_B \times T_{CHG}}{C_B} = M \times \frac{R_A}{R_B} \times \frac{C_A}{C_B} \times \frac{V_{REF}^2}{V_{IN}}, \quad (7)$$

where $R_A = R_B$ and $C_A = C_B$; V_{B_MAX} can be simplified as follows:

$$V_{B\_MAX} = M \times \frac{V_{REF}^2}{V_{IN}}. \quad (8)$$

Here, V_{B_MAX} is inversely proportional to V_{IN}, which is a function of $1/x$. The tunable-gain $1/x$ circuit is achieved by changing the value of M of the current-adjusting circuit.

Although V_{B_MAX} is inversely proportional to V_{IN}, V_B changes during the capacitor charging operation. A sampling circuit composed of a sampling switch and a capacitor is used for the continuous output voltage of the $1/x$ function. After every capacitor charging operation, the capacitor C_{SH2} samples and holds V_{B_MAX} by the SH (sample-and-hold) signal. If C_{SH2} is much smaller than C_B, then the voltage of C_{SH2} (V_{SH2}) becomes V_{B_MAX}.

$$V_{SH2} = V_{B\_MAX}. \quad (9)$$

An output-voltage generator with an operational amplifier, a current mirror, and two resistors (R_{SH} and R_{OUT}) is designed, because the minimum output voltage of the $1/x$ circuit is 0 V. The designed output-voltage generator makes 0 V easily by reducing the current going through the resistor R_{OUT}. The output current (I_{OUT}) is K-times larger than I_{SH} (= V_{SH2}/R_{SH}). The output voltage (V_{OUT}) is expressed as follows:

$$V_{OUT} = K \times \frac{R_{OUT}}{R_{SH}} \times V_{SH2}. \quad (10)$$

From equations (8), (9), and (10), V_{OUT} is simplified as follows:

$$V_{OUT} = M \times \frac{V_{REF}^2}{V_{IN}}, \quad \text{where } R_{SH} = K \times R_{OUT}. \quad (11)$$

When a resistive load is connected to the output node, V_{OUT} changes in such a way that an additional voltage buffer is required. However, in many applications, the $1/x$ circuit has a high-impedance output; thus, no voltage buffer is required, because the $1/x$ circuit drives the other circuits in the same chip.

Figure 4 shows the waveforms of the $1/x$ circuit when the input voltage (V_{IN}) changes. The current I_{IN} charging the capacitor C_A is proportional to V_{IN} such that the charging time (T_{CHG}) is inversely proportional to V_{IN} when the voltage of C_A (V_A) reaches V_{REF}. Therefore, the maximum voltage of C_B (V_{B_MAX}) is also inversely proportional to V_{IN}, because C_B is

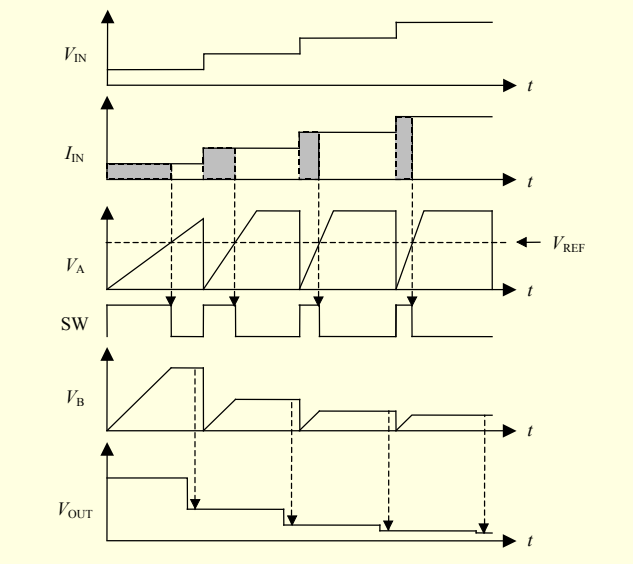

Fig. 4. Waveforms of $1/x$ circuit.

Table 1. Design and adjustable parameters of $1/x$ circuit.

Design parameters	C_A=1 pF, C_B=1 pF, C_{SH}=0.1 pF
	R_A=40 kΩ, R_B=160 kΩ
	K=5, R_{OUT}=10 kΩ, R_{SH}=50 kΩ
Adjustable parameters	M=0–1 for CNT[1:8]
	V_{REF}=0.1 V–1 V
Gain	0–1

charged with a constant current I_B during T_{CHG}. The output voltage (V_{OUT}) becomes a continuous voltage that is inversely proportional to V_{IN} by sampling V_{B_MAX} every clock cycle.

From equations (7), (9), and (10), the output voltage of the $1/x$ circuit is expressed as follows:

$$V_{OUT} = M \times K \times \frac{R_{OUT}}{R_{SH}} \times \frac{R_A}{R_B} \times \frac{C_A}{C_B} \times \frac{V_{REF}^2}{V_{IN}}. \quad (12)$$

The $1/x$ circuit was implemented with a 0.18 μm CMOS process at V_{DD} = 1.8 V. By applying the design parameters in Table 1, (12) can be simplified as follows:

$$V_{OUT} = \frac{\text{Gain}}{V_{IN}}, \quad \text{where Gain} = \frac{M}{4} \times V_{REF}^2. \quad (13)$$

The gain is controlled by the parameters M and V_{REF}. The parameter M can be changed between "0" and "1" by the 10-bit digital control code (CNT[1:10]), and the reference voltage V_{REF} can be changed between 0.1 V and 1 V. Therefore, the allowable range of the gain of the $1/x$ circuit is from "0" to "1."

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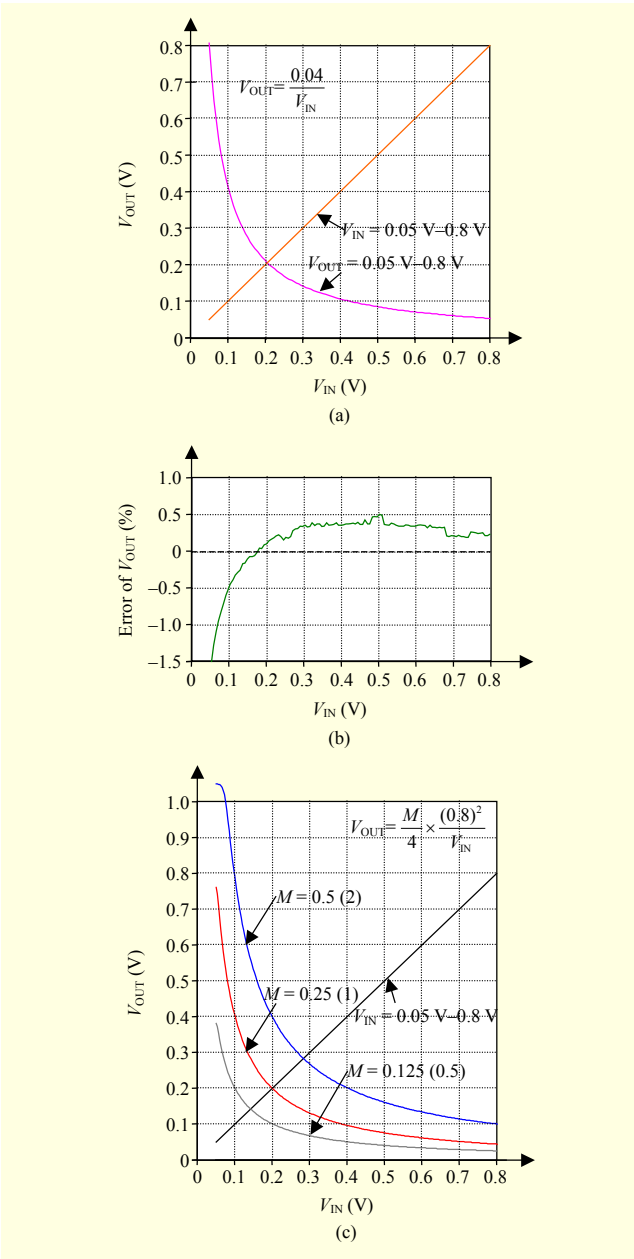

Fig. 5. Simulation results of 1/x circuit at M = 0.25 and V_{REF} = 0.8 V: (a) V_{OUT} vs. V_{IN}, (b) accuracy of V_{OUT}, and (c) V_{OUT} vs. M.

Figures 5(a) and 5(b) show the simulation results of the 1/x circuit at M = 0.25 and V_{REF} = 0.8 V. The 1/x circuit has errors less than 0.5% and 1.5% for V_{IN} = 0.1 V to 0.8 V and V_{IN} = 0.05 V to 0.8 V, respectively. The error increases when V_{IN} is under 0.1 V, because the offset voltages of the amplifiers become the more dominant factors as V_{IN} decreases. Figure 5(c) shows the gain variations of the 1/x circuit according to M at V_{REF} = 0.8 V. The simulation results in Table 2 show the high accuracy and wide input and output ranges of the 1/x circuit.

In (12), the output of the proposed 1/x circuit is independent

Table 2. Simulation results of 1/x circuit.

Process	0.18 μm CMOS
Supply voltage (V_{DD})	1.8 V
Clock frequency (f_{CLK})	1 MHz
Input voltage (V_{IN})	0.05 V–0.8 V
Output voltage (V_{OUT})	0 V–1 V
Accuracy of V_{OUT}	–0.5% < Error < 0.5% for V_{IN} = 0.1 V–0.8 V
	–1.5% < Error < 0.5% for V_{IN} = 0.05 V–0.8 V
Simulation conditions	$V_{OUT} = 0.04/V_{IN}$ @ M = 0.25, V_{REF} = 0.8 V

Table 3. Error sources of 1/x circuit.

Source	Number	Standard deviation (σ)
Offset voltage of amplifier	4	0.7% (1.4 mV @ V_{IN} = 0.2 V)
Mismatch of current mirror	3	0.18%
Resistor mismatch	2	0.07%
Capacitor mismatch	1	0.07%
Total error	N/A	1.45%

of the process parameters. However, the output is still affected by the mismatches of the devices. The main error sources are the offset voltages of amplifiers (AMPs), the mismatches of current mirrors, resistor mismatches (R_A and R_B, R_{OUT} and R_{SH}), and capacitor mismatches (C_A and C_B). In addition, the output is affected by the reference voltage (V_{REF}). The reference voltage comes from either an internal bandgap reference (BGR) circuit or an external voltage source. In this design, V_{REF} comes from an external voltage source so as to exhibit the variations of the 1/x circuit exactly. Table 3 shows the Monte Carlo simulation results of the error sources in the implemented 1/x circuit with a 0.18 μm CMOS process. The standard deviation (σ) of the total error is 1.45%. The largest error comes from the AMPs (σ = 0.7%).

The maximum clock frequency (f_{CLK}) for the voltage conversion of the 1/x circuit is determined by the capacitor charging time ($T_{CHG} = R_A \times C_A \times V_{REF}/V_{IN}$) in (4). When R_A = 40 kΩ, C_A = 1 pF, and V_{REF} = 0.8 V, the maximum capacitor charging time becomes 0.64 μs for the lowest allowable input voltage (V_{IN} = 0.05 V). In the simulations and experiments, a clock frequency of 1 MHz was used to cover the 0.64 μs capacitor charging time. A higher clock frequency can be used by reducing the maximum capacitor charging time with the parameters R_A, C_A, and V_{REF}. A lower clock frequency is recommended to save power consumption, because power consumption is proportional to the conversion frequency. The

small capacitors (C_A = 1 pF, C_B = 1 pF, and C_{SH} = 0.1 pF) are implemented to reduce power consumption and chip area, but they are weak from leakage currents and noises, which increase the error of the 1/x circuit. The larger capacitors, C_A, C_B, and C_{SH}, can improve the accuracy of the 1/x circuit.

III. Measurement Results

The proposed 1/x circuit was fabricated using a 0.18 μm CMOS process. Figure 6 shows a microphotograph of the chip. The chip occupies an area of 0.011 mm^2 (144 μm × 78 μm) and consumes 278 μW at V_{DD} = 1.8 V and f_{CLK} = 1 MHz. Figure 7 shows the measured waveforms of V_{OUT} according to V_{IN} (= 0 V to 1 V) at V_{REF} = 0.8 V and M = 0.5, 0.25, and 0.125. The function of the proposed 1/x circuit does not have any process parameters theoretically, but the output voltage of the proposed 1/x circuit is affected by process variations, such as the offset voltages of the AMPs; the switching delays of the AMPs; and the mismatches in capacitors, resistors, and current mirrors. Figure 8 shows the measured distribution of V_{OUT} for 20 untrimmed sample chips at V_{IN} = 0.2 V, M = 0.25, and V_{REF} = 0.8 V. The V_{OUT} of each chip is measured at V_{IN} = 0.2 V to show the distribution of V_{OUT} according to process variations. Theoretically, V_{OUT} = 0.2 V at V_{IN} = 0.2 V, because the function of the 1/x circuit is V_{OUT} = 0.04/V_{IN} at M = 0.25 and V_{REF} = 0.8 V. The mean (μ) and standard deviation (σ) of V_{OUT} for 20 samples were 200 mV and 3.21 mV (1.61%), respectively. The measured 20 sample chips showed a maximum and minimum V_{OUT} of 205.7 mV and 194.7 mV, respectively. Therefore, the maximum difference of V_{OUT} (ΔV_{OUT}) was 11 mV (5.48%). The change in V_{OUT} due to the process variations can be trimmed by the current-adjusting circuit. Figure 9 shows the measured accuracies of V_{OUT} for 20 trimmed sample chips at M = 0.25 and V_{REF} = 0.8 V. The 20 trimmed 1/x circuits have errors between +1.7% and –1.7% for V_{IN} = 0.05 V to 0.8 V.

Various 1/x circuit chips are compared in Table 4. The proposed 1/x circuit has a larger normalized input/output range

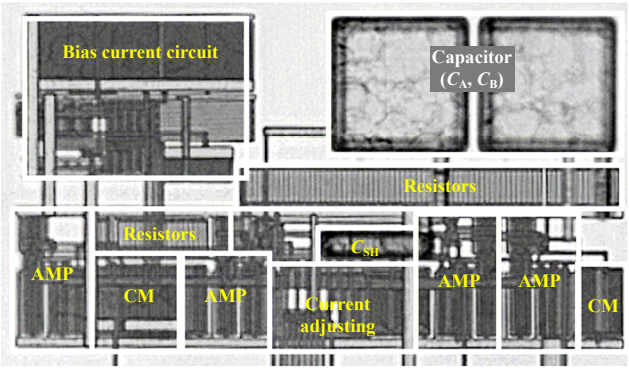

Fig. 6. Microphotograph of chip.

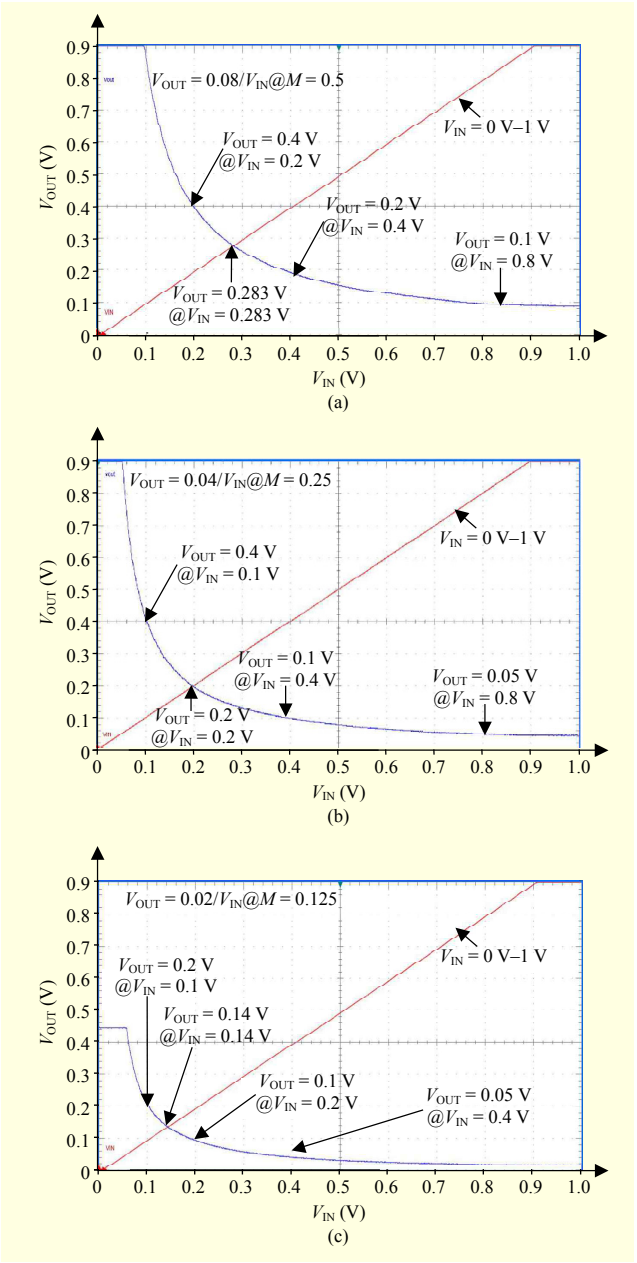

Fig. 7. Measured waveforms of V_{OUT} vs. V_{IN} (= 0 V to 1 V) at V_{REF} = 0.8 V: (a) M = 0.5, (b) M = 0.25, and (c) M = 0.125.

of 1 to 20 compared to other 1/x circuits (from 1 to 2.67 to 1 to 14). The normalized input/output range is the lowest value among the input and output ranges normalized with their minimum values. The previous 1/x circuits [3]–[5] have smaller errors of 1.7%. However, all previous 1/x circuits [3]–[6] have additional linearity errors due to PVT (process parameters, supply voltage, temperature) variations, as shown in Table 5. The additional linearity errors come from the parameters K (= $\mu C_{OX}W/L$), g_m (=$\sqrt{2KI_D}$), and V_T of the

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Table 4. Performance comparisons of various 1/x circuit chips.

	JSSC 1995 [3]	IEICE 2003 [4]	TCAS-II 2005 [5]	MWCAS 2012 [6]	This work
Process	2 μm CMOS	0.5 μm CMOS	0.5 μm CMOS	0.5 μm CMOS	0.18 μm CMOS
V_{DD} (V)	5	1.5	1.5	1.5	1.8
V_{SS} (V)	–5	–1.5	–1.5	–1.5	0
Power (μW)	N/A	240	220	80	278
Area (mm^2)	N/A	N/A	N/A	0.032	0.011
V_{IN} (V)	0.3–0.8	0.1–1.5	–	–0.4–0.4	0.05–1
V_{OUT} (V)	0.1–0.3	0.2–1.5	0.1–1.4	–0.2–0.2 (sim.)	0–0.9
I_{IN} (μA)	–	–	1–70	–	–
I_{OUT} (μA)	–	–	–	–50–50	–
Bandwidth	9 MHz (sim.)	N/A	100 MHz	175 kHz (sim.)	0.5 MHz*
Sampling frequency	–	–	–	–	1 MHz
Normalized input/output range	1–2.667	1–7.5	1–14	N/A	1–20
Number of samples	1	1	1	1	20
Linearity errors	±1% (sim.)	±1%	±0.85%	N/A	±1.7%

* Maximum bandwidth is equal to half of the sampling frequency, according to Nyquist theorem.

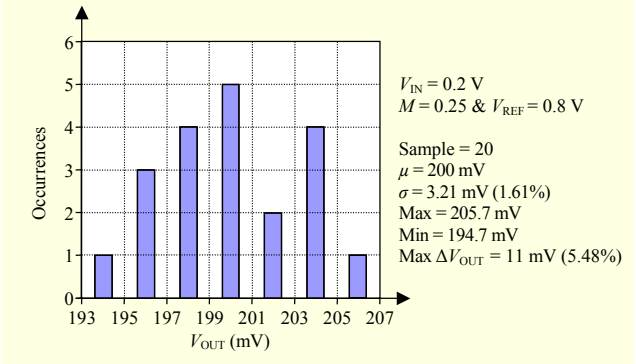

Fig. 8. Measured distribution of V_{OUT} for 20 untrimmed sample chips at V_{IN} = 0.2 V, M = 0.25, and V_{REF} = 0.8 V.

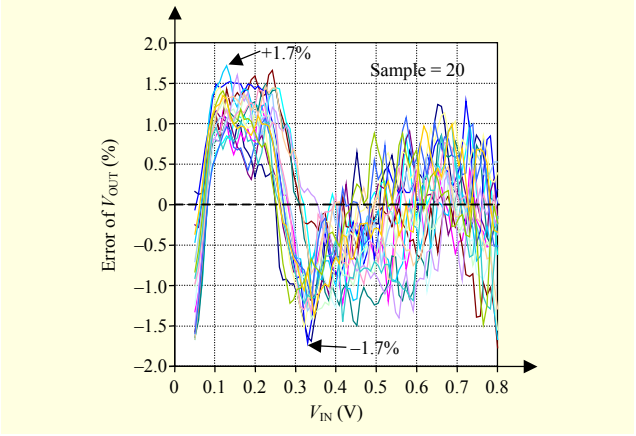

Fig. 9. Measured accuracies of V_{OUT} for 20 trimmed sample chips at M = 0.25 and V_{REF} = 0.8 V.

Table 5. Linearity error sources of PVT variations.

	Function	Measurement conditions	Linearity error sources
JSSC 1995 [3]	$V_{OUT} = \frac{g_m V_C}{4K_A V_{IN}}$	V_C = 0.5 V	K_A (21%) g_m (10%)
IEICE 2003 [4]	$V_{OUT} = \frac{I_C}{K_N V_{IN}}$	I_C = 10 μA–20 μA	K_N (21%)
TCAS-II 2005 [5]	$V_{OUT} = \frac{2K_P}{K_N}\frac{(V_{DD}-V_T)I_N}{I_{IN}}$	I_N = 0 μA–30 μA	K_P (21%) K_N (21%) V_T (20%)
MWCAS 2012 [6]	$V_{OUT} \approx \frac{\Delta V_N}{K_N \Delta V_{IN}}$	ΔV_N = 0.3	K_N (21%)
This work	$V_{OUT} = M\frac{V_{REF}^2}{V_{IN}}$	M = 0.25, V_{REF} = 0.8 V	-

* K ($=\mu C_{OX} W/L$) and g_m ($=\sqrt{2KI_D}$) are the transconductance parameters of MOSFET, and V_T is the threshold voltage of MOSFET.

MOSFET. In the 0.18 μm CMOS process, the maximum process variations of K, g_m, and V_T are 21%, 10%, and 20%, respectively. But, theoretically, the proposed 1/x circuit is not affected by the parameters (K, g_m, and V_T) because all parameters are removed from the equation of its function. Therefore, the additional linearity errors with PVT variations in [3]–[6] will be much larger than the linearity errors (±1.7%) of the proposed 1/x circuit.

The proposed 1/x circuit is slower than previous circuits [3] and [5], because its operation is based on the signal sampling

and the charge integration on capacitors. Its bandwidth (0.5 MHz) is considered to be half of the sampling frequency (1 MHz), according to Nyquist theorem. The bandwidth under 0.5 MHz is adequate for low-speed applications using the $1/x$ function. The analog dividers used in most instrumentation and control applications need a bandwidth of under 1 kHz [1]. A hearing-aid system [2] needs a bandwidth of 16 kHz.

IV. Conclusion

An accurate tunable-gain $1/x$ circuit was proposed. The output voltage of the $1/x$ circuit is generated using a capacitor charging time that is inversely proportional to the input voltage. The output voltage is independent of process parameters, because the output voltage depends on the ratios of the capacitors, resistors, and current mirrors. The $1/x$ circuit achieved low linearity errors and wide input and output voltages by using low offset amplifiers and by matching the capacitors, resistors, and current mirrors well. The voltage gain of the $1/x$ circuit is tuned by a 10-bit digital code. The $1/x$ circuit was fabricated using a 0.18 μm CMOS process. Its core area is 0.011 mm^2 (144 μm × 78 μm), and it consumes 278 μW at V_{DD} = 1.8 V and f_{CLK} = 1 MHz. Its linearity error is within 1.7% at V_{IN} = 0.05 V to 1 V.

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Byung-Do Yang received his BS, MS, and PhD degrees in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1999, 2001, and 2005, respectively. He was a senior engineer at the Memory Division, Samsung Electronics, Hwaseong, Rep. of Korea, in 2005, where he was involved in the design of DRAM. Since 2006, he has been at Chungbuk National University, Cheongju, Rep. of Korea, where he is now an associate professor. His research interests include analog circuits, memory circuits, and power IC designs.

Seo Weon Heo received his BS and MS degrees in electronic engineering from Seoul National University, Rep. of Korea, in 1990 and 1992, respectively, and his PhD degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2001. From 1992 to 1998, he was with the Digital Media Research Laboratory, LG Electronics Co., Ltd., Seoul, Rep. of Korea. From 2001 to 2006, he worked at the Telecommunication R&D Center, Samsung Electronics Co., Ltd., Hwaseong, Rep. of Korea. Since 2006, he has been an associate professor with the School of Electronic and Electrical Engineering, Hongik University, Seoul, Rep. of Korea. His current research interests include signal processing, wireless communication, and embedded system design.