250 mV Supply Voltage Digital Low-Dropout Regulator Using Fast Current Tracking Scheme

Jae-Mun Oh, Byung-Do Yang, Hyeong-Ju Kang, Yeong-Seuk Kim, Ho-Yong Choi, and Woo-Sung Jung

This paper proposes a 250 mV supply voltage digital low-dropout (LDO) regulator. The proposed LDO regulator reduces the supply voltage to 250 mV by implementing with all digital circuits in a 0.11 µm CMOS process. The fast current tracking scheme achieves the fast settling time of the output voltage by eliminating the ringing problem. The over-voltage and under-voltage detection circuits decrease the overshoot and undershoot voltages by changing the switch array current rapidly. The switch bias circuit reduces the size of the current switch array to 1/3, which applies a forward body bias voltage at low supply voltage. The fabricated LDO regulator worked at 0.25 V to 1.2 V supply voltage. It achieved 250 mV supply voltage and 220 mV output voltage with 99.5% current efficiency and 8 mV ripple voltage at 20 µA to 200 µA load current.

Keywords: Digital regulator, fast current tracking, low-dropout regulator, LDO, low voltage, subthreshold.

I. Introduction

Recently, the high demand for handheld and portable devices with a long battery-runtime has driven research into low-voltage circuits, because the low-voltage operation of very-large-scale integration (VLSI) circuits is an effective method for reducing both dynamic and leakage power dissipation. The supply voltage of the VLSI circuits was reduced to a subthreshold voltage (for example, 180 mV FFT processor [1] and 200 mV SRAM [2]).

For stable operations in such low-voltage circuits, a stable supply voltage needs to be provided. Analog low-dropout (LDO) regulators are used widely for supply voltage regulation due to their small area, low ripple voltage, and rapid transient response. The supply voltage of the analog LDO regulator was reduced to 650 mV [3]–[6]. However, the supply voltage is still higher than the threshold voltage.

Digital LDO regulators were proposed for low-voltage regulation [7]–[10]. The supply voltage was decreased to 380 mV. The digital LDO regulator supplies a current to the output load with all digital feedback control, as shown in Fig. 1. The digital LDO regulator in [7] consists of a digital clocked comparator, a shift register–based controller, and a current switch array instead of an error amplifier and a power transistor in an analog LDO regulator. However, the shift register–based controller causes a large area and slow setting time of the output voltage.

In this paper, a 250 mV supply voltage digital LDO regulator using a fast current tracking scheme is proposed. The proposed LDO regulator consists of three comparators, a digital controller, and a current switch array. A comparator is used for the feedback control of the output voltage. The other

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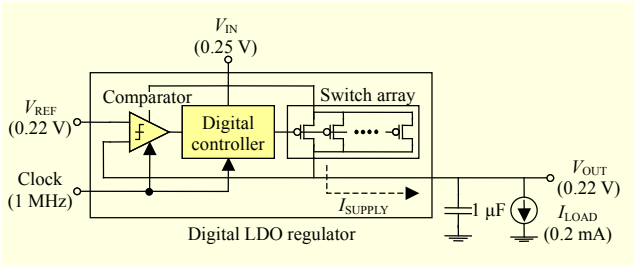

Fig. 1. Block diagram of digital LDO regulator.

comparators are used for the over-voltage and under-voltage detections to limit the overshoot (positive ripple) and undershoot (negative ripple) voltages of the output voltage. The controller with the fast current tracking scheme reduces the settling time of the output voltage by eliminating the ringing problem. The switch bias circuit in the current switch array reduces the size of the current switch array by applying a forward body bias voltage at low supply voltage. The proposed digital LDO regulator achieves a high current efficiency and low ripple voltage at 250 mV supply voltage.

The rest of this paper is organized as follows. Section II describes the architecture of the proposed digital LDO regulator. Section III shows the measurement results of the fabricated chip. Finally, conclusions are drawn in Section IV.

II. Proposed Digital LDO Regulator Architecture

1. Concept of Fast Current Tracking Scheme

Figure 1 shows a block diagram of a digital LDO regulator. The comparator compares the reference voltage (V_{REF}) and the output voltage of the digital LDO regulator (V_{OUT}). The digital controller determines the number of on-switches. The switch array supplies the current (I_{SUPPLY}) from the power supply (V_{IN}) to the output node with an external capacitor (C_{EXT}) and a load current source (I_{LOAD}).

Figure 2(a) shows the operations of the digital LDO regulator with the conventional voltage feedback control [7]. When I_{LOAD} increases from I_1 to I_2, V_{OUT} decreases due to the current difference (ΔI) between I_{LOAD} (= I_2) and I_{SUPPLY} (= I_1). The number of on-switches in the switch array continues to increase to supply more current (I_{SUPPLY}). However, when V_{OUT} = V_{REF}, I_{SUPPLY} becomes I_3 (= I_1 + 2 × ΔI) and the current difference ΔI still exists. This causes the ringing problem in V_{OUT}. In the simulation, when a variable current source is used for I_{LOAD}, a ringing exists for a long time. When a variable resistor is used instead of the current source, a larger ringing exists but its magnitude decreases.

The proposed fast current tracking scheme provides the fast

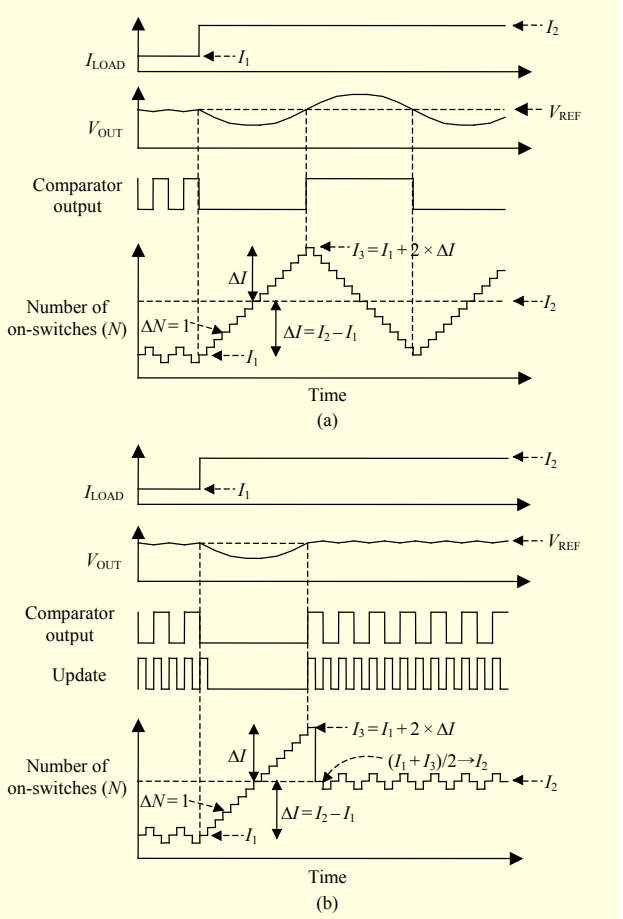

Fig. 2. Operations of digital LDO regulator with (a) voltage feedback control [7] and (b) proposed fast current tracking scheme.

settling time of V_{OUT} by eliminating the ringing problem, as shown in Fig. 2(b). In this scheme, at every voltage crossing of V_{OUT} and V_{REF}, the update signal becomes "1" and the number of on-switches becomes the mean of the two on-switch numbers at the previous two voltage crossings. For example, when two voltage crossings occur at I_1 and I_3, I_{SUPPLY} becomes I_2 by averaging I_1 and I_3. Therefore, the supply current rapidly follows the load current and the ringing of V_{OUT} can be eliminated.

The operations of the proposed digital LDO regulator are performed by the digital controller in Fig. 3. The 8-bit register #1 stores the present on-switch number. The adder/subtracter increases or decreases the on-switch number (N) by ΔN according to the comparator output (0 or 1), every clock cycle. The variable ΔN can be either "1" or "K." In Fig. 2(b), $\Delta N = 1$ because N changes one by one. In the case when $\Delta N = K$, the operations are explained in Section II-2. The 8-bit register #2 stores the on-switch number at the previous voltage crossing of V_{REF} and V_{OUT}, as shown in Fig. 2(b). When the update signal becomes "1" at a new voltage crossing of V_{REF} and V_{OUT},

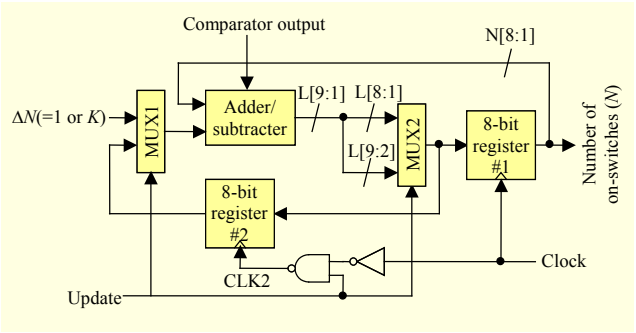

Fig. 3. Digital controller for fast current tracking scheme.

multiplexer #1 (MUX1) selects the register #2 and multiplexer #2 (MUX2) selects L[9:2] instead of L[8:1] for 1-bit-shifting the summing result of the values in the two registers. As a result, the average of the two values at the previous and new voltage crossings, which are stored in registers #1 and #2, is calculated. The update signal remains at "1" during one clock cycle. The CLK2 pulse signal for register #2 is generated by the clock signal before the update signal returns to "0." Register #2 stores the average value, which will be used at the next voltage crossing. Register #1 also stores the average value and then the adder/subtracter restarts to increase or decrease the on-switch number from the average value.

For example, when I_{LOAD} changes from I_1 to I_2 (= I_1 + ΔI) as shown in Fig. 2(b), register #2 stores the on-switch number of I_1 at the previous voltage crossing. The adder/subtracter continues to increase the on-switch number of I_{SUPPLY} in register #1 until a new voltage crossing happens when I_{SUPPLY} becomes I_3 (= I_1 + 2 × ΔI). At the new voltage crossing, the update signal becomes "1" so that the two multiplexers (MUX1 and MUX2) select their second inputs. The adder/subtracter adds two values stored in the registers #1 and #2 (I_3 and I_1) by MUX1. The summing value (I_1 + I_3) is 1-bit-shifted by MUX2 to make the average of I_1 and I_3 (= I_1 + 2 × ΔI), which is the same as I_2 (= I_1 + ΔI). Registers #1 and #2 store the on-switch number of I_2.

The digital controller has a circuit for keeping the on-switch number within a positive allowed number (0 to 255). The circuit is not shown in Fig. 3.

2. Over-Voltage and Under-Voltage Detection Scheme

In a conventional digital LDO regulator, the on-switch number (N) changes in increments of one (ΔN = 1), as shown in Fig. 4(a). Therefore, when the load current (I_{LOAD}) changes rapidly, it takes many clock cycle times when I_{SUPPLY} follows I_{LOAD}. This causes large ripple voltages (V_{R1} and V_{R2}). The ripple voltages can be reduced by using the over-voltage and under-voltage detection scheme, as shown in Fig. 4(b). In

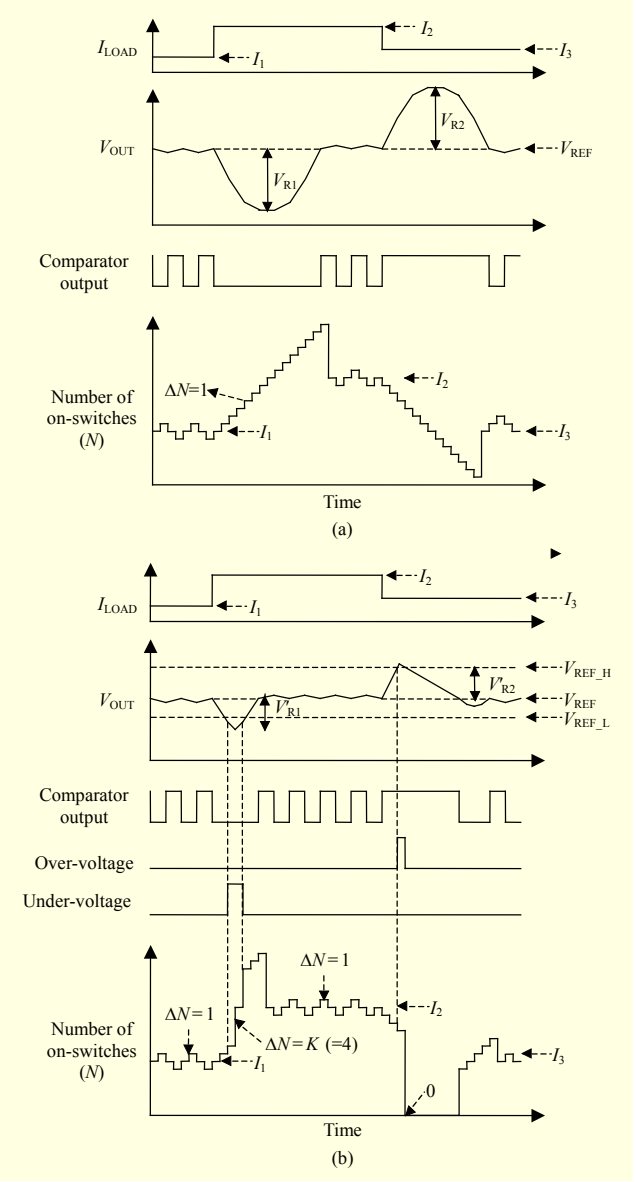

Fig. 4. Operations of digital LDO regulator (a) without and (b) with over-voltage and under-voltage detection scheme.

this scheme, if V_{OUT} > V_{REF_H}, then the on-switch number immediately becomes "0" and the LDO regulator stops supplying the current. Therefore, the positive ripple voltage is restricted by V_{REF_H}. On the contrary, if V_{OUT} < V_{REF_L}, then the on-switch number changes by K instead of one (ΔN = K). In Fig. 4(b), K is set to four. The on-switch number changes rapidly (ΔN = K = 4) so that I_{SUPPLY} follows I_{LOAD} in a short time. This decreases the negative ripple voltage. When V_{OUT} > V_{REF_L}, ΔN returns to "1." The on-switch number changes in increments of one (ΔN = 1) for the fine supply current control.

Figure 5 shows the voltage sensing circuit including the over-voltage and under-voltage detection. The voltage sensing circuit consists of three comparators, four resistors, and two

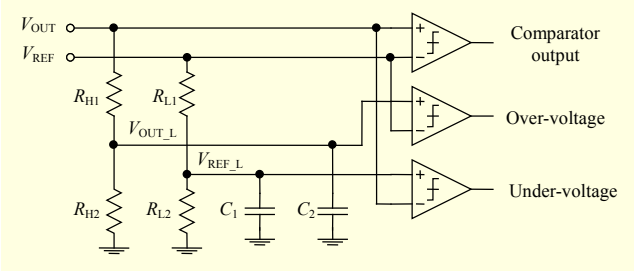

Fig. 5. Voltage sensing circuit.

capacitors. For the under-voltage protection, two resistors, R_{L1} and R_{L2}, make V_{REF_L}, which is as follows:

$$V_{REF\_L} = \frac{R_{L2}}{R_{L1} + R_{L2}} \times V_{REF}. \quad (1)$$

For the over-voltage protection, two resistors, R_{H1} and R_{H2}, make V_{OUT_L} instead of V_{REF_H}, where V_{OUT_L} is as follows:

$$V_{OUT\_L} = \frac{R_{H2}}{R_{H1} + R_{H2}} \times V_{OUT}. \quad (2)$$

The comparator can determine if V_{OUT} is larger than V_{REF_H}, by comparing V_{OUT} with V_{OUT_L}. Assume that $V_{OUT} = V_{REF\_H}$ when $V_{OUT\_L} = V_{REF}$. Then, V_{REF_H} is as follows:

$$V_{REF\_H} = \frac{R_{H1} + R_{H2}}{R_{H2}} \times V_{REF}. \quad (3)$$

In the simulation, V_{REF_H} is set to be 5% higher than V_{REF}, and V_{REF_L} is set to be 2.5% lower than V_{REF}. When $V_{REF} = 220$ mV, $V_{REF\_H} = 231$ mV, and $V_{REF\_L} = 214.5$ mV ($\Delta V_{REF\_H} = 11$ mV and $\Delta V_{REF\_L} = -5.5$ mV).

Two capacitors, C_1 and C_2, are used for supplying two stable voltages V_{REF_L} and V_{OUT_L} from the kickback noises of the comparators. The capacitors are implemented with the gate capacitances of NMOS transistors. In this design, the gate area ($W \times L$) of the NMOS transistors for C_1 and C_2 is about 20 times larger than that of the input transistors of the comparators.

Figure 6 shows the simulated waveforms of the proposed digital LDO regulator. The LDO regulator was implemented using a 0.11 μm CMOS process. The simulations are performed at $V_{IN} = 0.25$ V, $V_{REF} = 0.22$ V, $f_{CLK} = 1$ MHz, $C_{EXT} = 1$ μF, and $K = 8$. The load current I_{LOAD} is changed arbitrarily from 0 μA to 200 μA. After V_{REF} is changed from 0 V to 0.22 V, the start-up time is 228 μs. The start-up time is improved by the under-voltage detection with $K = 8$. When the current changes between 20 μA to 200 μA, the undershoot (negative ripple) and overshoot (positive ripple) voltages are 5.9 mV and 6.8 mV, respectively. The undershoot voltage is reduced by the under-voltage detection with $\Delta V_{REF\_L} = -5.5$ mV. The overshoot voltage is restricted by the over-voltage detection with $\Delta V_{REF\_H} = 11$ mV.

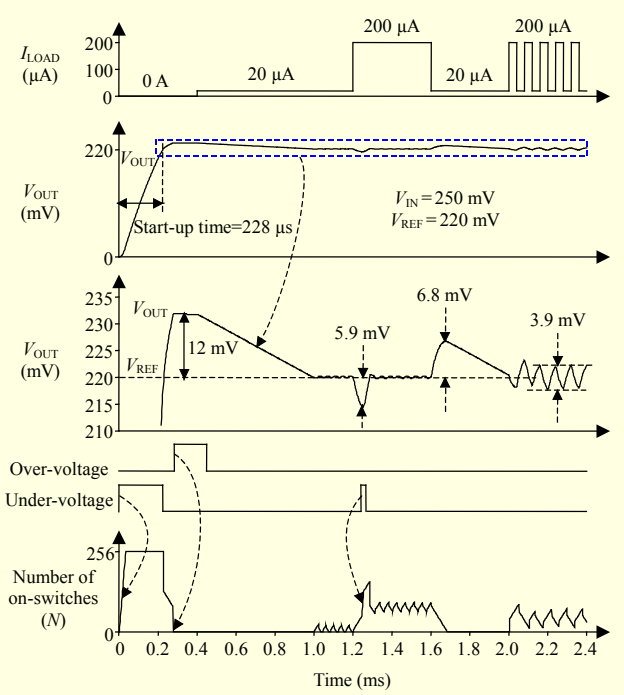

Fig. 6. Simulated waveforms of proposed LDO regulator.

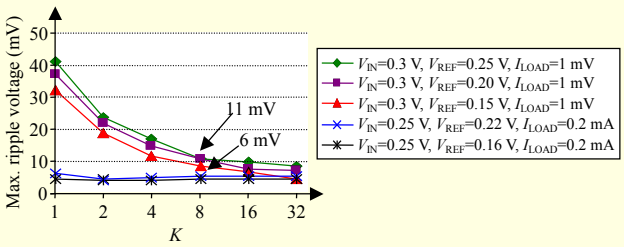

Fig. 7. Maximum undershoot voltage according to K.

The undershoot voltage increases proportional to I_{LOAD} and decreases proportional to I_{LSB}, f_{CLK}, and C_{EXT}, where I_{LSB} is the supply current difference of I_{SUPPLY} when $\Delta N = 1$. The I_{LSB} is proportional to the sizes of the power switches, the supply voltage (V_{IN}), and the voltage difference between V_{IN} and V_{OUT} (= V_{REF}). The larger K decreases the undershoot voltage by changing $K \times I_{LSB}$ instead of I_{LSB} when $V_{OUT} < V_{REF\_L}$. The variable K is selected to take the value of "8" from the simulations in Fig. 7. The value of K is fixed at the IC fabrication.

The ripple voltages (the overshoot and undershoot voltages) are proportional to I_{LOAD} and are inversely proportional to f_{CLK}, $I_{SUPPY,MAX}$, and C_{EXT}. The proposed digital LDO regulator works at very low supply voltage under a subthreshold voltage, at which both f_{CLK} and $I_{SUPPY,MAX}$ decrease significantly. The slow supply-current transitions due to the low f_{CLK} and low $I_{SUPPY,MAX}$ cause a larger decoupling capacitor, which acts as a

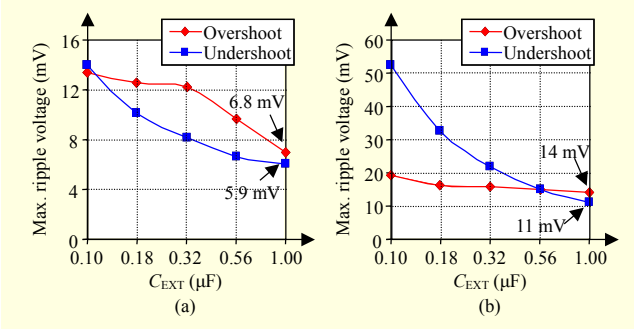

Fig. 8. Maximum ripple voltages when (a) I_{LOAD} = 20 μA to 200 μA at V_{IN} = 250 mV and V_{REF} = 220 mV and (b) I_{LOAD} = 0.1 mA to 1 mA at V_{IN} = 300 mV and V_{REF} = 250 mV.

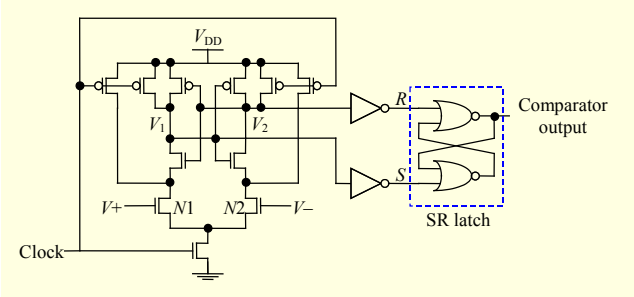

Fig. 9. Comparator.

current buffer for the fast transient load current. Therefore, the proposed digital LDO regulator needs a much larger decoupling capacitor than the analog LDO regulators. Figure 8(a) shows the maximum ripple voltages when I_{LOAD} = 20 μA to 200 μA, V_{IN} = 250 mV, and V_{REF} = 220 mV. The overshoot and undershoot voltages are 6.8 mV and 5.9 mV at C_{EXT} = 1 μF, respectively. Figure 8(b) shows the maximum ripple voltages when I_{LOAD} = 0.1 mA to 1 mA, V_{IN} = 300 mV, and V_{REF} = 250 mV. The overshoot and undershoot voltages are 11 mV and 14 mV at C_{EXT} = 1 μF, respectively. In this design, the external decoupling capacitor (C_{EXT}) is selected to 1 μF.

Figure 9 shows the comparator circuit in the voltage sensing circuit, which is the sense-amplifier-type flip-flop. When the clock signal is "0," the nodes *S* and *R* (set and reset) are "0." When the clock signal changes to "1," one of the nodes becomes "1." This updates the SR latch storing the comparator output. The comparator output is used in the digital controller during the next clock cycle.

Figure 10 shows the minimum required supply voltage (V_{DD}) of the comparator according to V_{REF} at f_{CLK} = 1 MHz. In the simulation, two input voltages (*V*+ and *V*–) of the comparator have the voltage difference of 2 mV and the common mode voltage of V_{REF}. The minimum V_{DD} is 238 mV at V_{REF} = 140 mV. The lower V_{REF} decreases the gate-source voltages

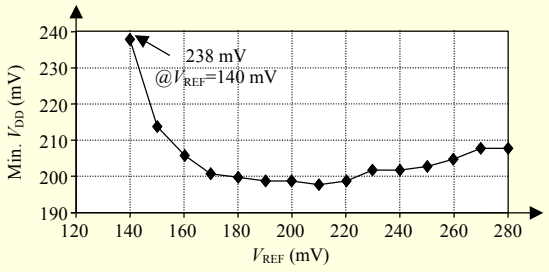

Fig. 10. Minimum required V_{DD} of comparator according to V_{REF} at f_{CLK} = 1 MHz when input voltage difference is 2 mV.

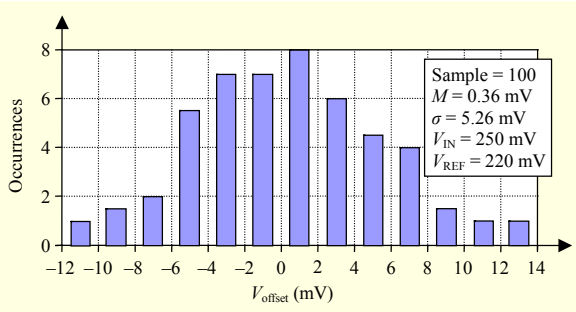

Fig. 11. Monte Carlo simulation at V_{IN} = 250 mV and V_{REF} = 220 mV.

and drain currents of the transistors *N*1 and *N*2 in the comparator in Fig. 9. The reduced drain currents cause slow sensing operations in the comparator because the voltages of V_1 and V_2 change slowly. However, the higher V_{DD} improves the sensing speed in the nodes V_1 and V_2. To finish the sensing operation at f_{CLK} = 1 MHz, the lower V_{REF} needs the higher V_{DD}. The reference voltage (V_{REF}) can be lowered to 140 mV at V_{DD} = 250 mV.

The voltage difference between V_{REF} and V_{OUT} of the LDO regulator comes from the input offset voltage of the comparator (V_{offset}). The offset voltage is mainly affected by the process mismatches and variations. Figure 11 shows the Monte Carlo simulation results at V_{IN} = 250 mV and V_{REF} = 220 mV. The mean (*M*) and standard deviation (σ) of the offset voltage for 100 samples were 0.36 mV and 5.26 mV, respectively. The output voltage error due to the offset voltage can be adjusted by trimming V_{REF}. Also, the two reference voltages (V_{OUT_L} and V_{REF_L}) for the over-voltage and under-voltage detections can be trimmed with the resistors R_{H1}, R_{H2}, R_{L1}, and R_{L2} to cancel the offset voltages of the comparators. If the reference voltage trimming is impossible, then ΔV_{REF_H} (= V_{REF_H} − V_{REF}) and ΔV_{REF_L} (= V_{REF} − V_{REF_L}) should be larger than the offset voltages.

3. Switch Array

The digital LDO regulator uses 256 transistor switches for

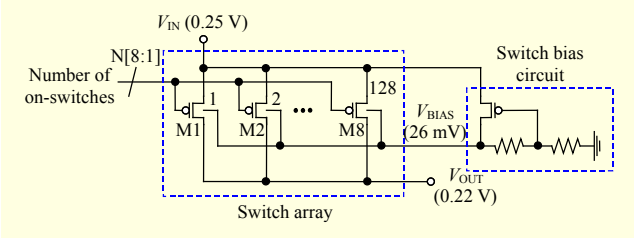

Fig. 12. Switch array.

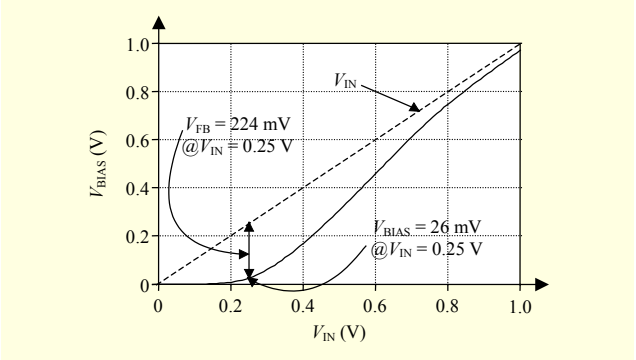

Fig. 13. Bias voltage (V_{BIAS}) according to V_{IN}.

fine current control. In this design, the switch array uses eight binary weighted transistor switches instead of the same 256 transistor switches [7]–[8], to reduce the switch array area, as shown in Fig. 12. The switch bias circuit is used to improve the current driving capability of the PMOS transistors in the switch array.

When V_{IN} = 0.25 V, the gate-source voltage of the turn-on PMOS transistor switches are in the subthreshold voltage regions. The current driving capability of the PMOS transistor is reduced significantly, so much so that large transistors are needed to flow the large load current. To improve the current driving capability, the forward bias voltage (V_{FB}= V_{IN}– V_{BIAS}) is applied to the PMOS transistors. The forward bias voltage must be well controlled to prevent the current flowing in the parasitic PN junction diode between P+ source and N-well. Figure 13 shows the bias voltage (V_{BIAS}) according to V_{IN}. The switch bias circuit generates the forward bias voltage (V_{FB}) of 224 mV at V_{IN} = 0.25 V. The forward bias voltage is much lower than the turn-on voltage of the PN junction diode (about 0.7 V). The switch bias circuit is safe for a wide range of V_{IN} (0.25 V to 1.2 V).

Figure 14 shows the maximum supply current ($I_{SUPPLY,MAX}$) when all switches are turned on and the voltage difference between V_{IN} and V_{OUT} is 50 mV. The maximum supply current of the proposed switch array with the forward bias voltage (630 μA) is 3.1 times larger than that of the conventional switch array (204 μA) at V_{IN} = 0.25 V. Therefore, the size of the switch array can be reduced in proportion to the current driving

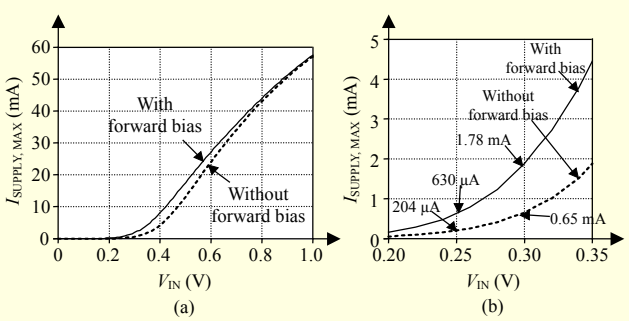

Fig. 14. Maximum supply current of switch array (a) V_{IN} = 0 V to 1 V and (b) V_{IN} = 0.2 V to 0.35 V.

improvement.

For the fast current tracking scheme, $I_{SUPPLY,MAX}$ needs be two times larger than I_{LOAD}. For example, if $I_{SUPPLY,MAX}$ is 400 μA, then the recommended current of I_{LOAD} is smaller than 200 μA. Of course, I_{LOAD} can increase up to $I_{SUPPLY,MAX}$. However, if $I_{SUPPLY,MAX}$ is smaller than 2 × I_{LOAD}, then the current tracking time increases.

III. Measurement Result

The LDO regulator chip was fabricated using a 0.11 μm CMOS process. Figure 15 shows the chip microphotograph. Table 1 lists the characteristics of the LDO regulator chip. The chip core area is 7,700 μm^2 (110 μm × 70 μm). All measurements were performed at C_{EXT} = 1 μF and f_{CLK} = 1 MHz. The minimum voltages of V_{IN} and V_{OUT} are 250 mV and 140 mV, respectively. The maximum load currents at V_{IN} = 0.25 V and V_{IN} = 0.3 V are 0.2 mA and 1 mA, respectively. When V_{IN} = 0.25 V, V_{REF} = 0.22 V, and I_{LOAD} = 0.2 mA, the current and power efficiencies are 99.45% and 87.52%, respectively. When the load current is changed from 20 μA to 200 μA, the ripple voltage of V_{OUT} is 8 mV at V_{IN} = 0.25 V.

Figures 16(a) and 16(b) show the measured V_{OUT} according

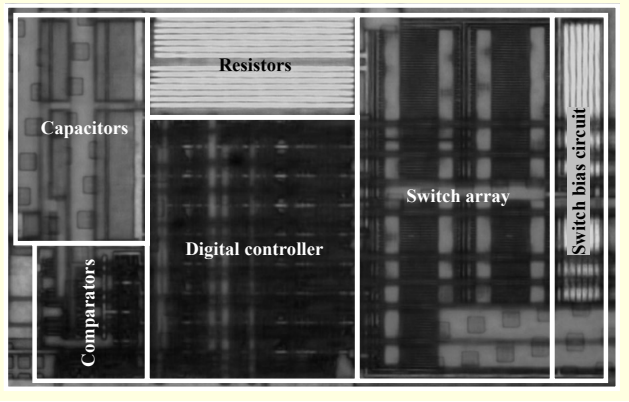

Fig. 15. Chip microphotograph.

Table 1. Characteristics of LDO regulator chips.

Technology	0.11 μm CMOS process	
Area	7,700 μm^2 (110 μm × 70 μm)	
Ext. Cap.	1 μF	
f_{CLK}	1 MHz	
V_{IN}	0.25 V–1.2 V	
V_{OUT}	0.14 V–0.22 V	0.14 V–0.28 V
Max. I_{LOAD}	0.2 mA @ V_{IN}=0.25 V	1 mA @ V_{IN}=0.3 V
Quiescent current	1.10 μA @ V_{IN}=0.25 V	1.37 μA @ V_{IN}=0.3 V
Current (power) efficiency	99.45% (87.52%) @ V_{IN}=0.25 V, V_{REF}=0.22 V, I_{LOAD}=0.2 mA	99.86% (83.22%) @V_{IN}=0.3 V, V_{REF}=0.25 V, I_{LOAD}=1 mA
Line regulation	1.5 mV/V @ I_{LOAD}=0.2 mA	2.5 mV/V @ I_{LOAD}=1 mA
Load regulation	2 mV/mA @ V_{IN}=0.25 V, V_{REF}=0.15 V	2 mV/mA @ V_{IN}=0.3 V, V_{REF}=0.25 V
Ripple/overshoot /undershoot of V_{OUT}	8 mV/5 mV/5 mV @ V_{IN}=0.25 V, V_{REF}=0.22 V, I_{LOAD}=20 μA–200 μA	13 mV/8 mV/8 mV @ V_{IN}=0.3 V, V_{REF}=0.25 V, I_{LOAD}=0.1 mA–1 mA

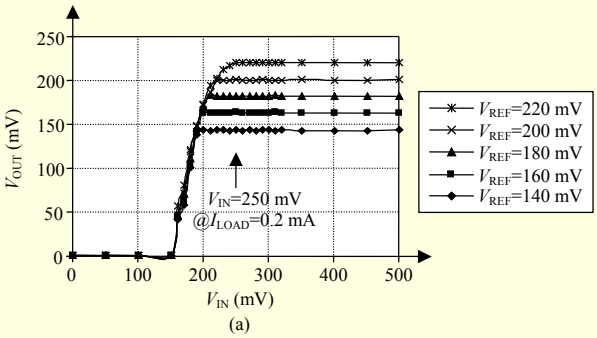

Fig. 16. Measured V_{OUT} according to V_{IN} when V_{REF} is changed (a) I_{LOAD} = 200 μA and (b) I_{LOAD} = 1 mA.

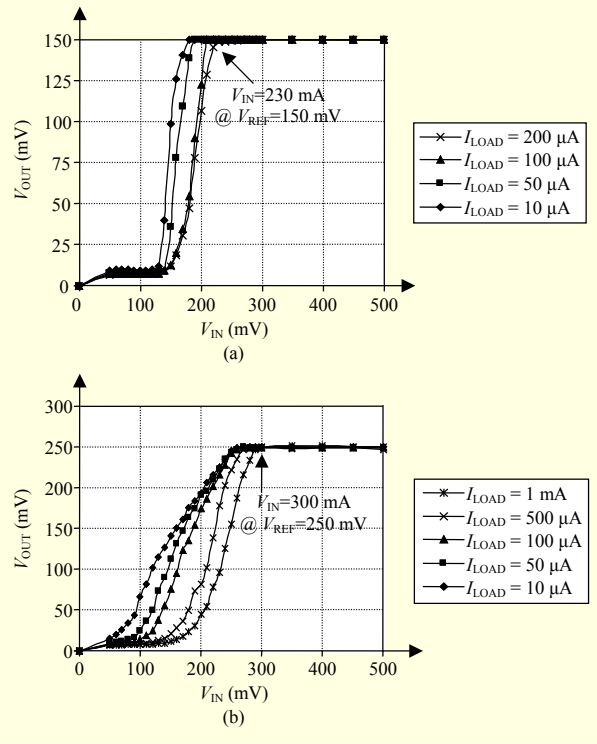

Fig. 17. Measured V_{OUT} according to V_{IN} when I_{LOAD} is changed (a) V_{REF} = 150 mV and (b) V_{REF} = 250 mV.

to V_{IN} at I_{LOAD} = 0.2 mA and I_{LOAD} = 1 mA, respectively. The digital LDO regulator can regulate V_{OUT} from 140 mV to 220 mV at V_{IN} = 250 mV and I_{LOAD} = 0.2 mA. Also, it can regulate V_{OUT} from 140 mV to 280 mV at V_{IN} = 300 mV and I_{LOAD} = 1 mA. The line regulations are 1.5 mV/V and 2.5 mV/V at I_{LOAD} = 0.2 mA and I_{LOAD} = 1 mA, respectively.

Figures 17(a) and 17(b) show the measured V_{OUT} according to V_{IN} at V_{REF} = 150 mV and V_{REF} = 250 mV, respectively. The current I_{LOAD} is changed from 10 μA to 1 mA. The load regulation is 2 mV/mA. The minimum V_{IN} can be as low as 230 mV at I_{LOAD} = 0.2 mA and V_{REF} = 150 mV. However, the minimum V_{IN} for low voltage drop regulation is 250 mV, as shown in Fig. 16(a).

Figure 18 shows the measured current efficiency and quiescent current of the digital LDO regulator according to I_{LOAD}. These are measured at f_{CLK} = 1 MHz. The constant current of 0.8 μA to 1 μA is drained through the resistor strings in the voltage sensing circuit and the switch bias circuit. When V_{IN} = 250 mV, V_{REF} = 150 mV, and I_{LOAD} = 0.2 mA; the current efficiency, power efficiency, and quiescent current are 99.45%, 87.52%, and 1.10 μA, respectively. When V_{IN} = 300 mV, V_{REF} = 250 mV, and I_{LOAD} = 1 mA, the current efficiency, power efficiency, and quiescent current are 99.86%, 83.22%, and 1.37 μA, respectively.

Figure 19(a) shows the measured transient waveforms of V_{OUT} when I_{LOAD} changes from 20 μA to 200 μA at V_{IN} = 250 mV, and V_{REF} = 220 mV. The ripple voltage of V_{OUT} is 8 mV.

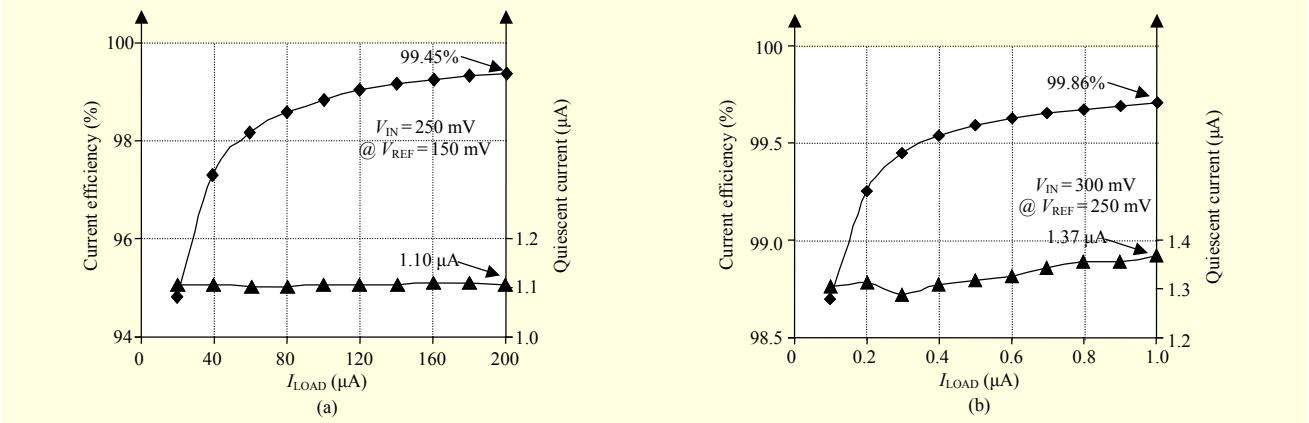

Fig. 18. Measured current efficiency and quiescent current according to I_{LOAD} when (a) V_{IN} = 250 mV and V_{REF} = 150 mV and (b) V_{IN} = 300 mV and V_{REF} = 250 mV.

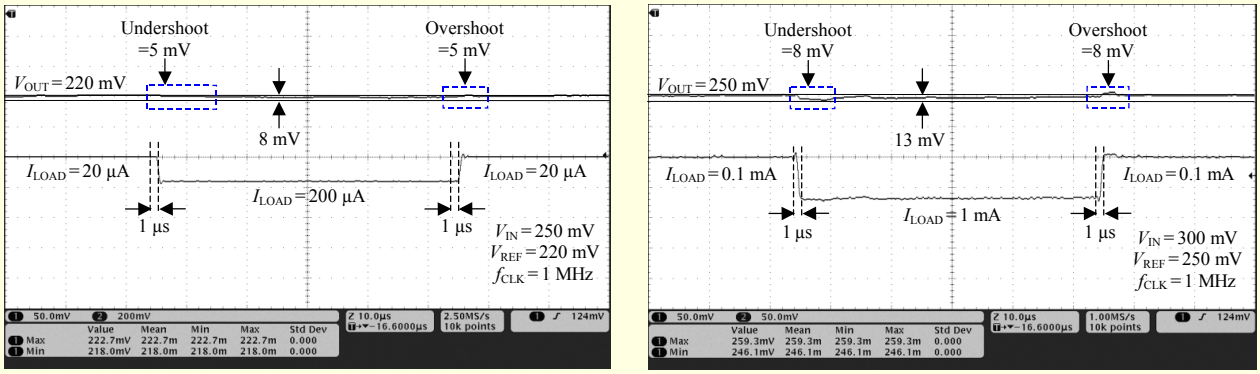

Fig. 19. Measured transient waveforms of V_{OUT} when (a) I_{LOAD} changes from 20 µA to 200 µA at V_{IN} = 0.25 V and V_{REF} = 0.22 V and (b) I_{LOAD} changes from 0.1 mA to 1 mA at V_{IN} = 0.3 V and V_{REF} = 0.25 V.

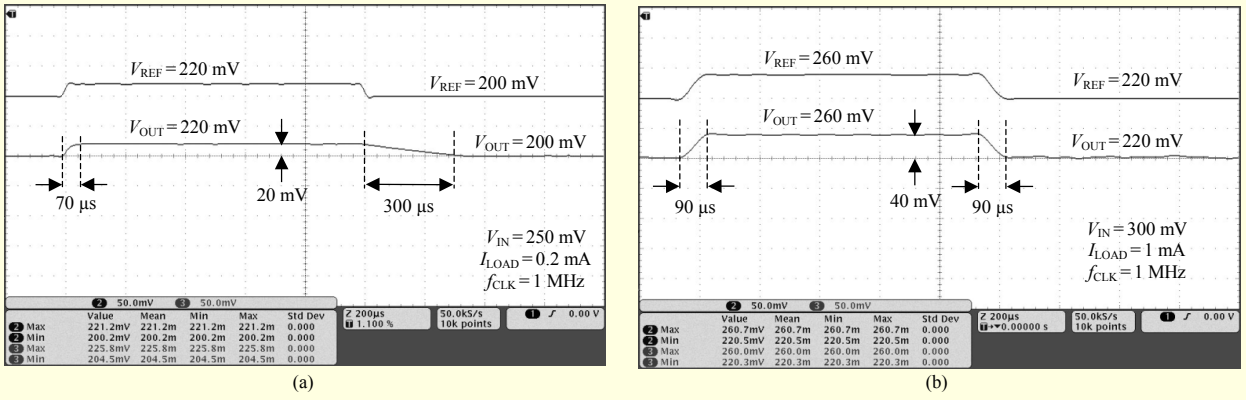

Fig. 20. Measured transient waveforms of V_{OUT} when (a) V_{REF} changes from 200 mV to 220 mV at V_{IN} = 0.25 V and I_{LOAD} = 0.2 mA and (b) V_{REF} changes from 220 mV to 260 mV at V_{IN} = 0.3 V and I_{LOAD} = 1 mA.

Both the measured undershoot and overshoot voltages are 5 mV. Figure 19(b) shows the measured transient waveforms of V_{OUT} when I_{LOAD} changes from 0.1 mA to 1 mA at V_{IN} = 300 mV, and V_{REF} = 250 mV. The ripple voltage of V_{OUT} is 13 mV. Both the measured undershoot and overshoot voltages are 8 mV.

Figure 20 shows the measured transient waveforms of V_{OUT} when V_{REF} changes. In Fig. 20(a), when V_{REF} changes from 200 mV to 220 mV at V_{IN} = 250 mV, I_{LOAD} = 0.2 mA, and f_{CLK} = 1 MHz, the rising and falling times of V_{OUT} are 70 µs and

Table 2. Performance comparisons of low-voltage LDO regulator chips.

	EL 2006 [3]	ISSCC 08 [4]	JSSC 10 [5]	JSSC 10 [6]	CICC 10 [7]	IET 2013 [8]	This work	
							V_{IN}=0.25 V	V_{IN}=0.3 V
Process	180 nm	350 nm	90 nm	90 nm	65 nm	90 nm	110 nm	
LDO type	Analog	Analog	Analog	Analog	Digital	Digital	Digital	
Area (mm^2)	0.122	0.053	0.155	0.019	0.042	0.026	0.0077	
V_{IN} (V)	0.65–0.95	1.05–3.5	0.95–1.4	0.75–1.2	0.5	0.38	0.25–1.2	
V_{OUT} (V)	0.5	0.9	0.7–1.2	0.5–1.0	0.45	0.12–0.32	0.14–0.22	0.14–0.28
$I_{LOAD,MAX}$ (mA)	50	4.04–164	100	100	0.2	1	0.2	1
$I_{Quiescent}$ (μA)	12.72	50	14	8	2.7	6.85	1.1	1.37
Current (power) efficiency (%)	99.9 (76.9)	99.7 (85.4)	99.9 (85.7)	99.9 (66.7)	98.7 (88.8)	99.3 (83.6)	99.45 (87.52)	99.86 (83.22)
Line regulation (mV/V)	0.23	1.06	N/A	3.78	3.1	2.9	1.5	2.5
Load regulation (mV/mA)	0.19	0.0614	0.4	0.1	0.65	0.11	2	2
Decoupling cap.	No cap.	1 μF	6 pF	7 pF	0.1 μF	0.1 μF	1 μF	1 μF
Overshoot (mV)	N/A	N/A	70	114	30	50	5	8
Undershoot (mV)	300	6.6	70	73	40	65	5	8

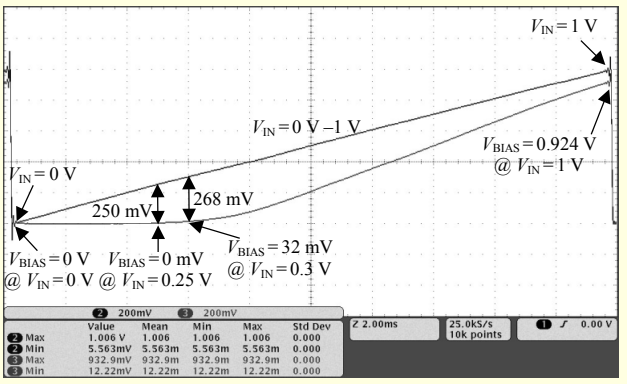

Fig. 21. Measured waveforms of bias voltage (V_{BIAS}) according to V_{IN}.

300 μs, respectively. The rising times of V_{OUT} and V_{REF} are similar. But, the falling time of V_{OUT} is slower than that of V_{REF} due to the small load current. In Fig. 20(b), when V_{REF} changes from 220 mV to 260 mV at V_{IN} = 300 mV, I_{LOAD} = 1 mA, and f_{CLK} = 1 MHz, the rising and falling times of V_{OUT} are both 90 μs. The transition times of V_{OUT} are almost the same as those of V_{REF}. The measurement shows that V_{OUT} follows the voltage change in V_{REF} rapidly.

Figure 21 shows the measured waveforms of the bias voltage (V_{BIAS}) according to V_{IN}. The forward bias voltage (V_{FB} = V_{IN} – V_{BIAS}) improves the current driving capability of the PMOS switch transistors. The forward bias voltages are 250 mV and 268 mV at V_{IN} = 0.25 V and V_{IN} = 0.3 V, respectively. The forward bias voltage is under 280 mV for V_{IN} = 0.25 V to 1.2 V, which is much lower than the turn-on voltage of the PN junction diode (about 0.7 V).

Table 2 compares low-voltage LDO regulator chips. The digital LDO regulators reduce the minimum power supply voltage ($V_{IN,MIN}$) and the minimum output voltage ($V_{OUT,MIN}$) compared with the analog LDO regulators. The proposed digital LDO regulator shows the better performances than the recently published low-voltage LDO regulators [3]–[8]. This work achieves the lowest supply voltage, the lowest regulated output voltage, the smallest area, the smallest overshoot and undershoot voltages.

IV. Conclusion

A 250 mV supply voltage digital LDO regulator was proposed. The proposed LDO regulator reduces the supply voltage to 250 mV by implementing with all digital circuits in a 0.11 μm CMOS process. The LDO regulator achieves a fast settling time of output voltage with a fast current tracking scheme and limits the overshoot and undershoot voltages using the over-voltage and under-voltage detection circuits. The size of the power switch arrary is reduced to 1/3 by applying the forward body bias voltage. The fabricated LDO regulator worked at 0.25 V to 1.2 V supply voltage. It achieved 250 mV supply voltage and 220 mV output voltage with 99.5% current efficiency and 8 mV ripple voltage at 20 μA to 200 μA load

current.

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