# Electrothermal Analysis for Super-Junction TMOSFET with Temperature Sensor

Young Hwan Lho and Yil-Suk Yang

**For a conventional power metal–oxide–semiconductor field-effect transistor (MOSFET), there is a trade-off between specific on-state resistance and breakdown voltage. To overcome this trade-off, a super-junction trench MOSFET (TMOSFET) structure is suggested; within this structure, the ability to sense the temperature distribution of the TMOSFET is very important since heat is generated in the junction area, thus affecting its reliability. Generally, there are two types of temperature-sensing structures — diode and resistive. In this paper, a diode-type temperature-sensing structure for a TMOSFET is designed for a brushless direct current motor with on-resistance of 96 mΩ·mm$^2$. The temperature distribution for an ultra-low on-resistance power MOSFET has been analyzed for various bonding schemes. The multi-bonding and stripe bonding cases show a maximum temperature that is lower than that for the single-bonding case. It is shown that the metal resistance at the source area is non-negligible and should therefore be considered depending on the application for current driving capability.**

**Keywords: TMOSFET, super-junction TMOSFET, trench MOSFET, embedded temperature sensor, bipolar sensor structure.**

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## I. Introduction

Super-junction (SJ) metal–oxide–semiconductor field-effect transistor (MOSFET) [1]–[2] power devices are well known for lower on-state resistance and gate charge. However, it is difficult to fabricate an exact balanced doping profile, and the impact of an imbalanced doping profile results in varying breakdown voltages (BVs). In the structure of an SJ MOSFET, heavily doped alternate P-N pillars act as a substitute for the lightly doped drift region of conventional power MOSFETs [3].

In a conventional MOSFET, there exists a trade-off between specific on-state resistance and BV. An interesting trade-off curve between the specific on-resistance and the BV capability can be created by using a doping gradient in the drift region as a parametric variable. The specific on-resistance in a non-uniform trench MOSFET (TMOSFET) is lower than that in a conventional MOSFET as BV increases [3].

A non-uniform SJ TMOSFET structure is used to overcome the specific on-resistance made in the drift region at the same BV. The BV of an SJ TMOSFET tends to increase as the length of the drift region increases and is independent of the doping concentration at the N-drift region. Then, the N-drift region can afford to be doped at a much higher concentration to reduce the on-state resistance of the drift region below that of the conventional structure without affecting the BV.

An SJ TMOSFET, on the other hand, has P and N pillars, which are of equal widths, $W_P$ and $W_N$, respectively, and is based on an SJ DMOSFET [1]–[2]. The doping concentrations of the P and N pillars in an SJ TMOSFET are denoted by $N_A$ and $N_D$, respectively. The relationship between the doping concentrations and widths of the pillars is as follows:

$$N_D W_N = N_A W_P, \quad (1)$$


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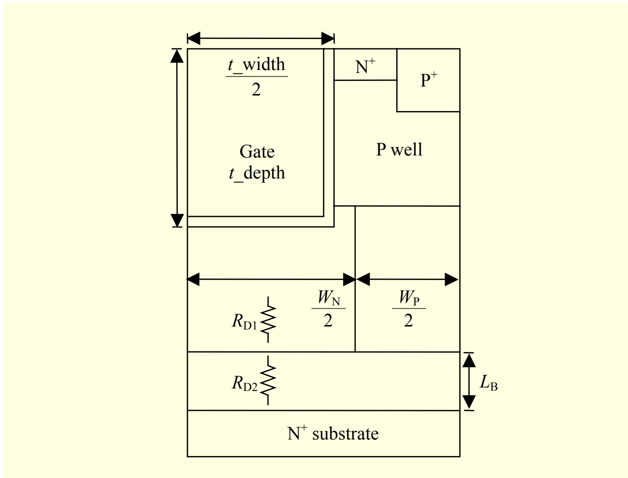


Fig. 1. Structure of SJ TMOSFET.

In this paper, a bipolar diode structure is used as a temperature sensor because of the linear dependency of its diode voltage on temperature [4]–[5]. A temperature-dependent model with self-heating characteristics has been implemented and will be described in the next section.

The MOSFET chip is divided into a 5 × 5 array of cells, each of which is 1 mm × 1 mm in size. Each unit cell is connected to the source metal, and the equivalent subcircuit model is implemented and simulated by SPICE. The power dissipation is calculated, and the junction temperatures are found for the power dissipation at each cell by using a thermal impedance model. The temperature at each unit cell is also calculated by using ANSYS software.

The structure of our SJ TMOSFET with embedded diode-type temperature sensor is shown in Fig. 1; it is composed of alternate P-N pillars, each of which is of the same width, in the drift region.

## II. SJ TMOSFET with Temperature Sensor

### 1. On-Resistance of SJ TMOSFET

The on-resistance of an SJ TMOSFET is determined by the resistance between the channel and drift regions. An increased doping concentration in the drift region enables a dramatic reduction of the drift region resistance, for a required BV. The on-resistance [3] can be obtained by currents flowing from the channel between the source and the drain electrodes, and is modelled as follows:

$$R_{\mathrm{ON}} = R_{\mathrm{CS}} + R_{\mathrm{N}} + R_{\mathrm{CH}} + R_{\mathrm{D1}} + R_{\mathrm{D2}} + R_{\mathrm{CD}}, \tag{2}$$

where $R_{CS}$ is the contact source resistance, $R_N$ is the source resistance, $R_{CH}$ is the channel resistance, $R_{CD}$ is the drain contact resistance, $R_{D1}$ is the N-type drift region resistance, and $R_{D2}$ is the substrate resistance. Figure 1 illustrates the various components of the SJ TMOSFET. Channel resistance and drift region resistance mainly affect on-resistance; the other types of resistance are significantly negligible and can be ignored in this paper.

#### A. Channel Resistance

The value of specific on-resistance from a channel in the non-uniform TMOSFET structure is the same as that for a uniform TMOSFET structure.

$$R_{\mathrm{CH,SP}} = \frac{L_{\mathrm{CH}} W_{\mathrm{cell}}}{2\mu_{ni} C_{\mathrm{OX}} \left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)}, \tag{3}$$

where $L_{CH}$ is the channel length, $W_{cell}$ is the width of a unit cell, $\mu_{ni}$ is the electron mobility, $C_{OX}$ is the gate capacitance, $V_G$ is the gate voltage, and $V_{TH}$ is the threshold voltage. The $R_{on,sp}$ from the channel in the non-uniform TMOSFET is 0.0184 mΩ·cm$^2$ when the gate bias is 10 V.

#### B. Drift Region Resistance

The resistance in the drift region consists of $R_{D1,SP}$ and $R_{D2,SP}$. The analytical modeling of the drift region resistance is complicated by the non-uniform doping profile that contains an electron mobility that varies with doping concentration. The drift region resistance contribution from the mesa region (N-pillar region) can be obtained by considering a small segment (d$y$) of the drift region at a depth $y$ from the bottom of the gate electrode. The specific resistance [2] of the drift region is computed by

$$R_{\mathrm{D1,SP}} = \left(\frac{W_{\mathrm{cell}}}{W_{\mathrm{M}}}\right) \int_0^{L_{\mathrm{D}}} \rho_{\mathrm{D}}(y)\,\mathrm{d}y, \tag{4}$$

where $W_M$ is the width of pillar N, and the resistivity $\rho_D(y)$ is a function of the position of $y$ in the drift region. The resistivity of the drift region is given by

$$\rho_{\mathrm{D}}(y) = \frac{1}{q\mu_n(y) N_{\mathrm{D}}(y)}, \tag{5}$$

where $q$ is the charge, $\mu_n(y)$ is the electron mobility, and $N_D(y)$ is the doping density of the drift region.

An additional resistance contribution of $R_{D2,SP}$ in the non-uniform TMOSFET structure is related to the buffer layer located below the bottom of the trenches. In this portion of the structure, the current density is uniform and current flow occurs across the entire cell width. The specific on-resistance [2] can be obtained from


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$$R_{\mathrm{D2,SP}} = \left(\frac{W_{\mathrm{cell}}}{W_{\mathrm{M}}}\right)\int_0^{L_{\mathrm{D}}} \frac{1}{q\mu_n(y)N_o e^{-gy}}\mathrm{d}y = \left(\frac{W_{\mathrm{cell}}}{W_{\mathrm{M}}}\right)\frac{1}{q\mu_n(y)N_o g}\left(e^{gL_{\mathrm{D}}}-1\right), \tag{6}$$

where $N_o$ is the doping concentration at the top of pillar N, $g$ is the exponential gradient doping profile, and $L_{\mathrm{D}}$ is the drift length of pillar N.

The doping profile at the N-drift region decreases exponentially, in which the concentration at the top of the N pillar is $1 \times 10^{16}$ cm$^{-3}$ and that at the bottom is $2 \times 10^{16}$ cm$^{-3}$ in the case of a 120 V non-uniform SJ TMOSFET structure with a doping gradient of $2.75 \times 10^3$ cm$^{-1}$. In the structure, the P-base region has a doping profile with a peak doping concentration of $1.5 \times 10^{17}$ cm$^{-3}$. The specific on-resistance for the drift region is 67 mΩ·mm$^2$, which satisfies design requirements.

## 2. Temperature Sensor

The diode-type temperature sensor is formed at the well region. As can be seen in Fig. 2(a) [6], the upper $P^+$ layer surrounded by the $N^+$ cathode layer plays the role of reducing electron injection toward the drain at the bottom, in which the parasitic operation of the vertical NPN bipolar transistor is eliminated. Figure 3 represents the vertical doping profile for the cathode layer; here, it can be seen that the net doping at 1 µm has increased to $8 \times 10^{19}$/cm$^3$, which is enough to prevent an electron injection. In the P-N diode-type temperature sensor depicted in Fig. 4, the cathode should possess a negative voltage so as to turn on the embedded diode. In the structure, most of the current flows horizontally at the surface from the cathode to the anode; however, about 10% of the current from the cathode flows to the substrate drain area, which reduces the unnecessary operation of the vertical NPN transistor formed between the cathode and the drain. The diode current at the surface of the SJ TMOSFET exponentially increases as the forward voltage increases. For the negative cathode voltage, the diode current (composed of both an anode and a cathode current) in the upper line in Fig. 5 linearly decreases at logarithmic scale. The current voltage characteristics for different temperatures of the diode, formed at the surface, are plotted in Fig. 6(a). The subthreshold region below the turn-on voltage of 0.7 V is applicable to the temperature sensor. As the temperature increases in Fig. 6(b), the voltage between the anode and the cathode linearly decreases at a rate of 1.74 mV/°C when a forcing current of 1 µA at the anode is measured.

In the SJ TMOSFET structure, the diode-type temperature sensor is implemented toward the upper part for measuring $V_{\mathrm{BE}}$.

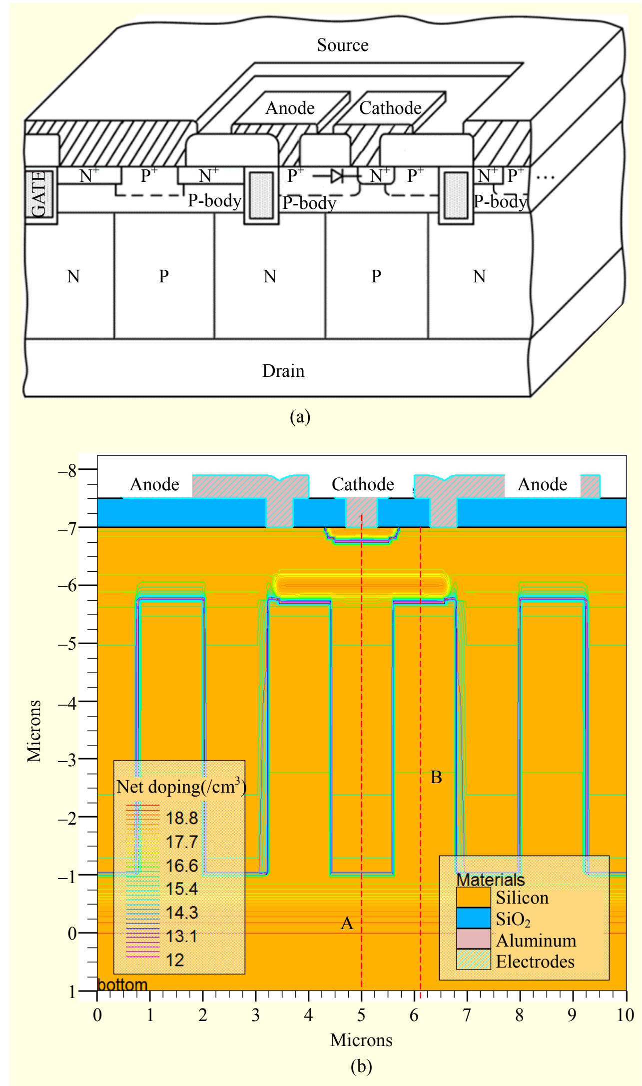



Fig. 2. Diode temperature sensor: (a) structure and (b) cross-section.

In the temperature range of 300 K to 450 K, a linear fit is applied to the relationship between the forward voltage versus temperature (K), which is obtained for an emitter current, as shown in Fig. 6(b). The diode-type temperature sensor's forward voltage line linearly decreases as temperature increases under a constant bias current.

For temperature sensing, the temperature change of the base-emitter voltage ($V_{\mathrm{BE}}$) under a constant emitter current is measured. The forward voltage is a well-known electrical parameter for measuring the temperature of a semiconductor device. The relationship [3] between the current, voltage, and temperature of an ideal PN-junction is given by

$$I_{\mathrm{PN}} = I_{\mathrm{S}}\left(e^{\frac{qV_{\mathrm{PN}}}{kT}}-1\right), \tag{7}$$

where $I_{\mathrm{S}}$ is the saturation current of the diode, $I_{\mathrm{PN}}$ is the current

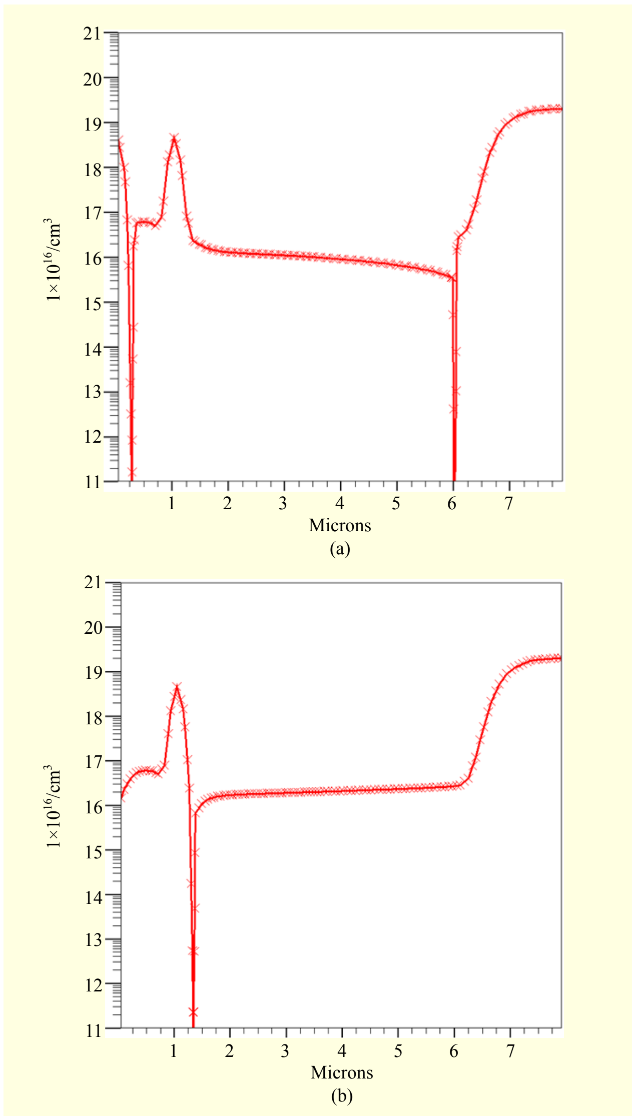



Fig. 3. Vertical doping profile from top to bottom at center of cathode in Fig. 2: (a) along line A and (b) along line B.

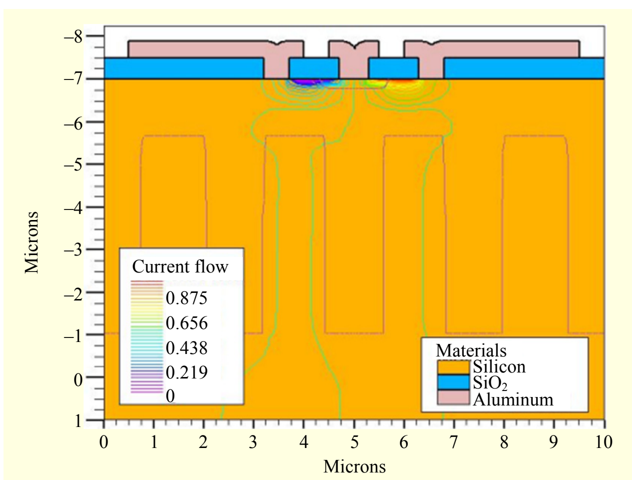



Fig. 4. Current flow line when $V_{\text{cathode}} = -0.7$ V.

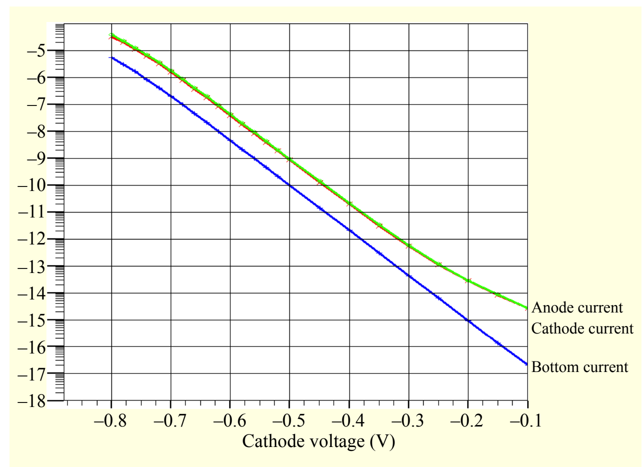
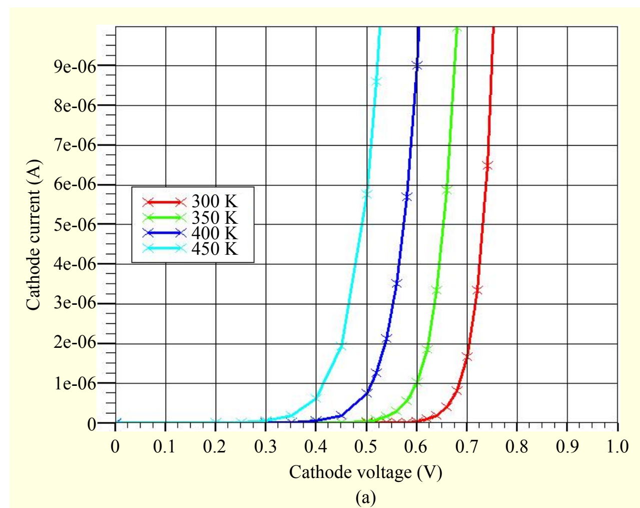



Fig. 5. Diode currents vs. negative cathode voltage (logarithmic scale).



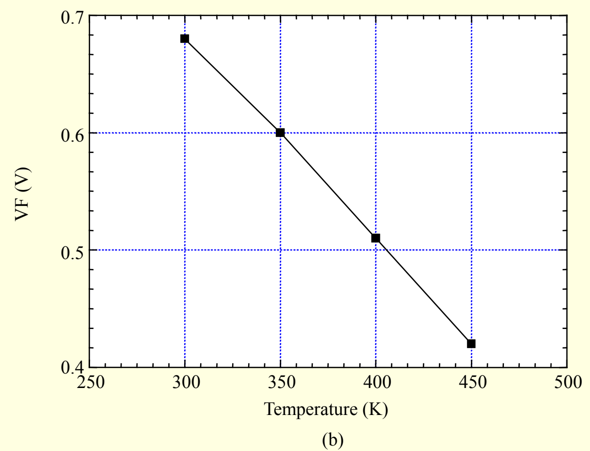




Fig. 6. Diode characteristics: (a) I-V characteristics for different temperatures and (b) forward voltage vs. temperature at current of 1 μA.

flowing through the PN-junction, $V_{\text{PN}}$ is the voltage across the junction, $q$ is the electron charge, $k$ is Boltzmann's constant,

Table 1. Specifications of SJ TDMOSFET [2].

| Device parameter | Value | Device parameter | Value |
|---|---|---|---|
| Cell pitch | 2.4 μm | Trench depth | 1.75 μm |
| N, P pillar doping concentration | $1\times10^{16}$/cm$^3$ | Trench width | 0.28 μm |
| Gate oxide thickness ($t_{ox}$) | 500 Å | N$^+$ source width | 0.25 μm |
| P well depth ($X_j$) | 1.2 μm | P$^+$ body contact width | 1.5 μm |

and $T$ is temperature. The saturation current [3] is described by

$$I_S = I_O T^{\gamma} e^{\frac{-E_g}{kT}}, \quad (8)$$

where $\gamma$ is a constant equal to about a value of three, $I_O$ is a constant, and $E_g$ is the bandgap of Si (1.12 eV at $T = 275$ K).

The bipolar transistor is formed by the emitter (N$^+$ source), base (P-body), and collector (N$^-$ epi) regions shown in Fig. 2. The base-emitter voltage [5] depends on the temperature under a biased constant current, and the change of $V_{BE}$ under this biased constant current can be measured as follows:

$$V_{BE} = V_{BE}(T_R) + \beta_{V_{BE}}(T - T_R), \quad (9)$$

where $V_{BE}(T)$ is the temperature-dependent base-emitter voltage, $T_R$[K] is the reference temperature, and $\beta_{V_{BE}}$ [V/K] is the temperature coefficient. The temperature coefficient of $\beta_{V_{BE}}$ is measured as –2 mV/K [5]. The measurement temperature range is –60 °C to 180 °C. The structure of the SJ TMOSFET is composed of alternate P-N pillars. The doping concentration and pillar widths are determined to balance the charge distribution of the structure. The main characteristics of an SJ TMOSFET with bipolar sensor are shown in Table 1.

## 3. Temperature Measurement

To measure the temperature of the chip, a constant current source is connected to the anode of the embedded diode-type temperature sensor [7]–[8], shown in Fig. 2. A square wave is applied to the gate of the SJ TMOSFET, and the embedded diode-type temperature sensor is internally mounted to the source. When the constant current at the diode temperature sensor is flowing, the temperature can be converted to a corresponding transient variation of voltage with respect to time, and then measured. It is possible to check the sensing temperature of the SJ TMOSFET, as is depicted in Fig. 7.

The threshold voltage of the SJ TMOSFET [9]–[10] decreases as the ambient temperature increases.

$$V_{th} = V_{th0} - \rho(T - T_0), \quad (10)$$

$$\mu_n = \mu_0\left(\frac{T}{T_0}\right)^{-m}, \quad (11)$$

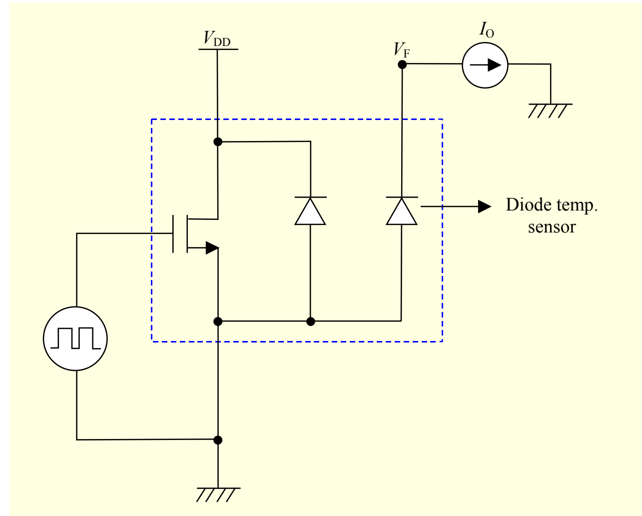



Fig. 7. Equivalent circuit for temperature measurement circuit.

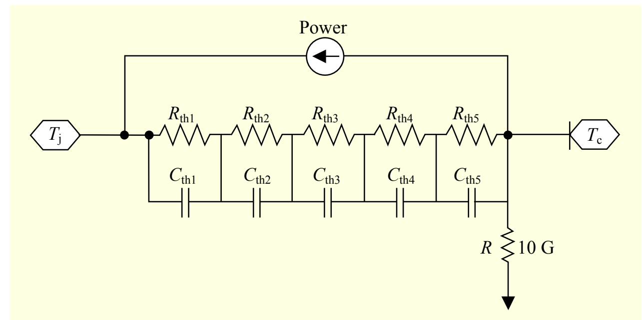



Fig. 8. Thermal impedance model for package.

where $V_{th}$ is the drain-source voltage, $V_{th0}$ is the threshold voltage at room temperature, $T$ is the junction temperature (K), $T_0$ is the reference temperature (300 K), $\rho$ is a threshold voltage coefficient of –0.0046 (V/K), $\mu_n$ is the electron mobility (V/m$^2$s), $\mu_0$ is the electron mobility at room temperature, and $m$ is an electron-mobility reduction model exponent of 1.5.

A thermal impedance model is designed (see Fig. 8). The relationship between power and temperature in this model is given by

$$T = P \times R_{th}, \quad (12)$$

where $T$ indicates temperature, $R_{th}$ represents thermal resistance, and $P$ represents power (in watts).

## 4. Self-Heating Electrothermal Model

In Fig. 8, $T_c$ is case temperature, $T_j$ is junction temperature, and $R$ of 10 GΩ is dummy resistance. The five combinations of both $R_{th}$ (thermal conductivity) and $C_{th}$ (heat capacity) are for modeling the transient thermal characteristics.

A thick aluminum layer (3 μm) is used to reduce the source resistance. An analysis of the distributed source resistance is

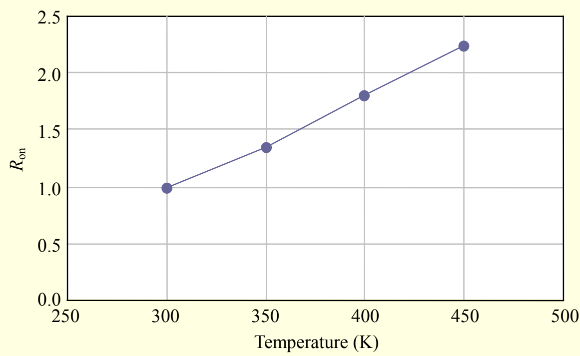



Fig. 9. Normalized on-resistance vs. temperature.

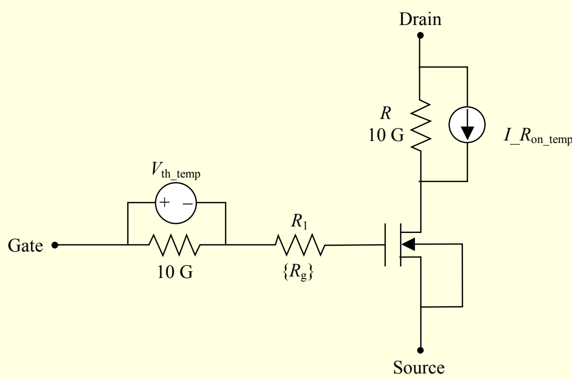



Fig. 10. Temperature-dependent equivalent circuit model of unit cell with threshold voltage and on-resistance.

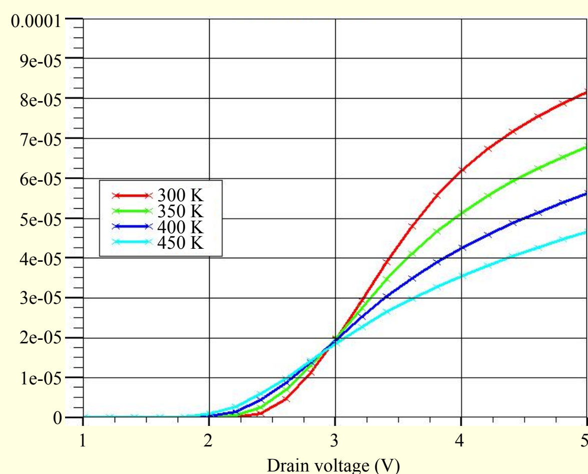



Fig. 11. $I_d$ vs. voltage ($V_d = V_g$) for four different temperatures.

needed, since this type of resistance is caused by the source metal in the case of low on-resistance.

As shown in Fig. 9, the normalized on-resistance linearly increases at a rate of 1.51%/K as the temperature increases; this rate is used for the equivalent circuit model of $I_R_{on_temp}$ in Fig. 10.

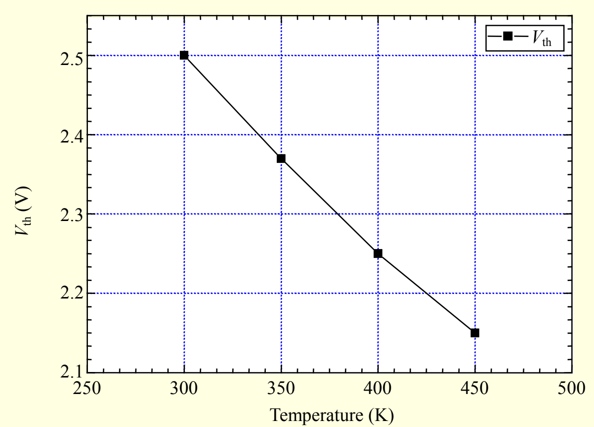



Fig. 12. Threshold voltage vs. temperature.

Figure 11 represents the relationship between the drain current, $I_d$, and the voltage applied to the shorted gate and drain. The figure shows that the threshold voltage decreases as the temperature increases. In the case of a high temperature during the operation of the SJ TMOSFET, the current level is greatly degraded by the ohmic voltage drop. In other words, the threshold voltage applied at $V_{th_temp}$ (see Fig. 10) decreases at a rate of approximately 2.3 mV/°C as temperature increases (see Fig. 12).

A model of a temperature-dependent MOSFET, in Fig. 10, having a shift in threshold voltage is considered. The related reduction in threshold voltage is represented by $V_{th_temp}$, which reflects the effect of temperature; the on-resistance, $R_{ds,on}$, increases as temperature increases; and vice versa.

The power dissipated by the SJ TMOSFET is transferred into the "thermal impedance model for package" (see Fig. 8), and the junction temperature ($T_j$) is then computed. Both the shift in threshold voltage and the on-resistance for the given temperature are transmitted to the equivalent circuit models of $V_{th_temp}$ and $I_R_{on_temp}$, respectively, in Fig. 10. The thermal impedance for a unit cell of 1 mm$^2$ is assumed to be uniformly distributed.

To reduce the on-resistance of a TMOSFET of 100 V and 100 A for a BLDC motor, an SJ TMOSFET is designed and its design parameters verified. A new type of stripe bonding is applied to a thermal package, and the characteristics of this type of bonding are well analyzed.

## III. Simulations and Analyses

Figure 13 shows electrothermal simulation flow [11]–[12]. To carry out electrothermal simulation, a unit-cell SJ TMOSFET, a self-heating thermal model, connected with resistor arrays at the source is considered [13]. A SPICE simulation is executed to obtain a steady-state transient solution.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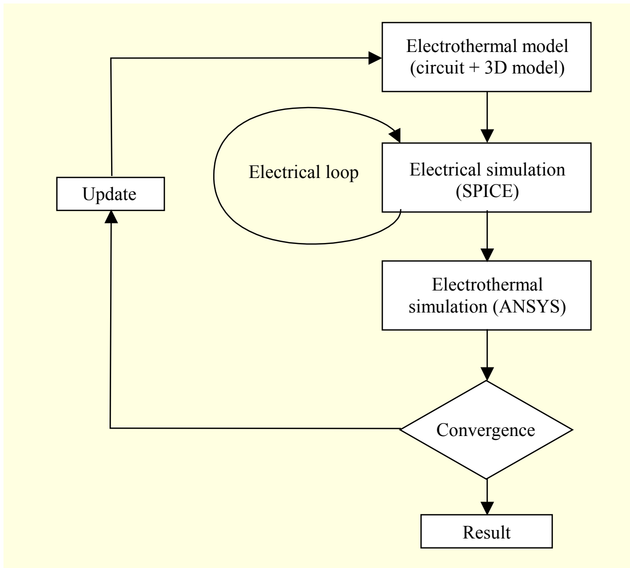


Fig. 13. Electrothermal simulation flow.

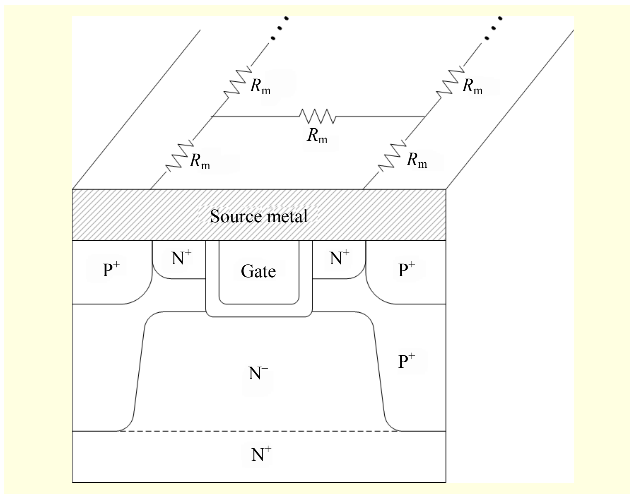


Fig. 14. Unit-cell structure of SJ TMOSFET.

The power dissipation at each unit cell of the SJ TMOSFET can be computed and transferred to an ANSYS model by using the heat-flow command described in this paper. Finally, the temperature distribution can then be obtained.

The current density in an SJ TMOSFET with ultra-low on-resistance ($R_{ds,on}$) is greatly affected by the parasitic resistance at the source metal at the top layer (see Fig. 14). To secure the reliability of the SJ TMOSFET, it is important for the temperature at the chip (see Fig. 15) to be uniformly distributed. As the number of bonding wires increases, the peak temperature point at the chip can be widely distributed. Through a SPICE simulation, we can check whether the number of bonding wires and their relative positions affect the temperature at the chip. In the case of a single bonding wire (see Fig. 16), the maximum and minimum temperatures are measured as 67.1 °C and 40.1 °C, respectively. Similarly, for four bonding wires (see Fig. 17), we have 47 °C and 41 °C, respectively. These results are similar to those of the stripe bonding in Fig. 18.

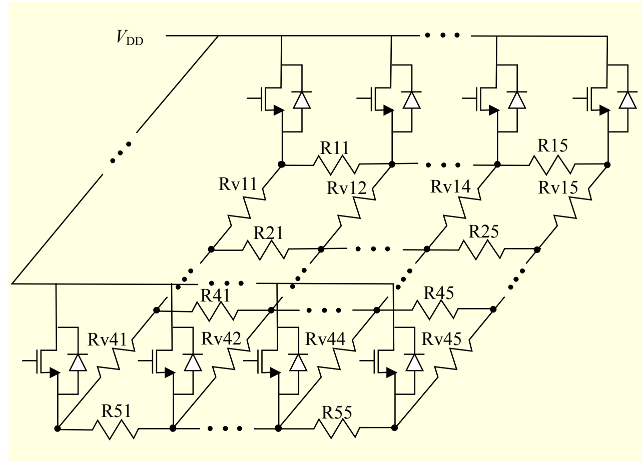


Fig. 15. Equivalent resistance model for an SJ TMOSFET with 5 × 5 array meshes (distributed source resistance and MOSFET equivalent model with 5 × 5 array meshes).

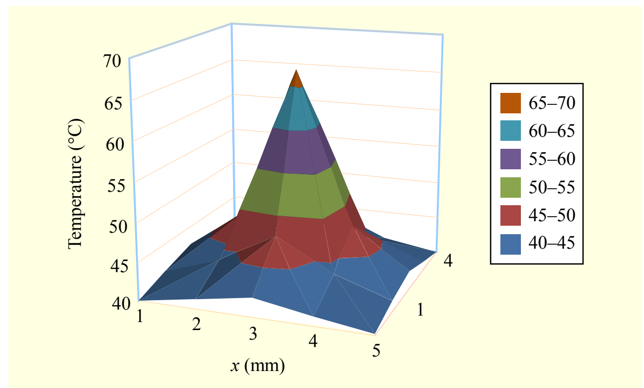


Fig. 16. Temperature distributions at points for single bonding wire.

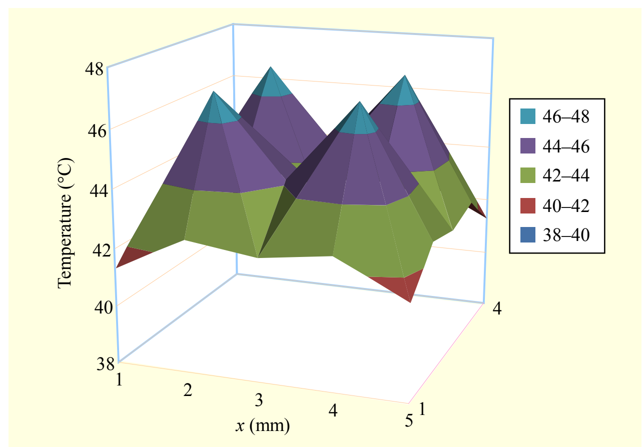


Fig. 17. Temperature distributions at points for four bonding wires.

An electrothermal SPICE model for a power MOSFET is

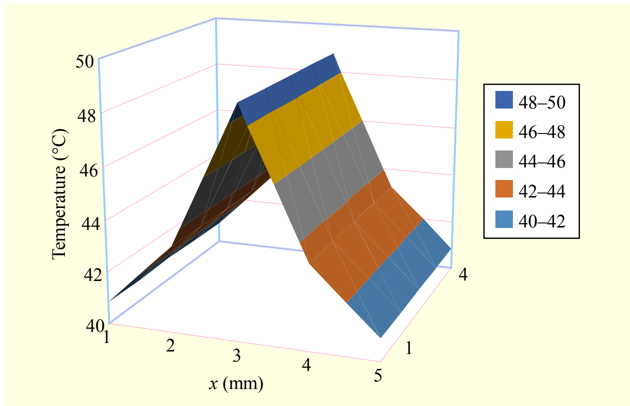


Fig. 18. Temperature distributions at points for stripe bonding.

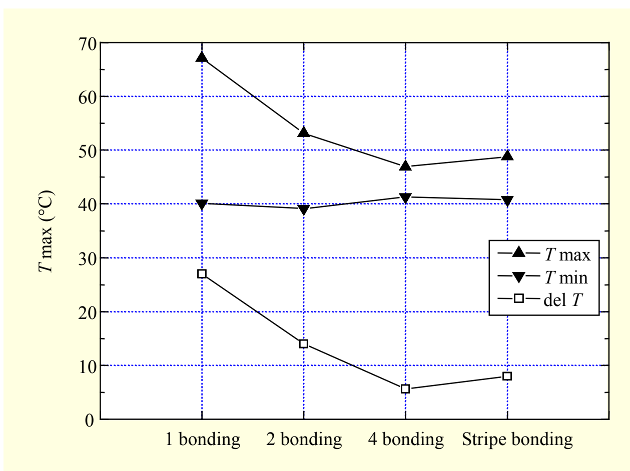


Fig. 19. Maximum, minimum, and difference values of temperature vs. different bonding schemes.

implemented. The thermal impedance models of TO220 and TO247 packages are referred to as a Fairchild MOSFET [12].

The sheet resistance of aluminum, which is used for the source metal at the top layer, is 15 mΩ·mm$^2$ for a thickness of 2 μm. The area of the chip is 1 mm$^2$, and the drift resistance between grid points is computed to be approximately 25 mΩ; the resistance of bonding wire is 0.1 mΩ. In the SJ TMOSFET equivalent resistance model (see Fig. 15) [12], [14], mesh resistance is caused by the source metal located at the uppermost area; the drift resistance at the SJ TMOSFET and resistance at the bonding is modeled as an array. Every node point at the resistor array located at the source metal (for a distributed resistance) is connected to the source (see Fig. 14). The simulation circuit is composed of 5 × 5 SJ MOSFETs and 4 × 4 resistor arrays.

The cross-section of a unit cell belonging to an SJ TMOSFET (based on Table 1) is shown in Fig. 14. Here, $R_m$ is the distributed resistance at the source metal — dependent mainly on the thick aluminum found at the top layer.

After analyzing the power dissipation by using LTspice [15],

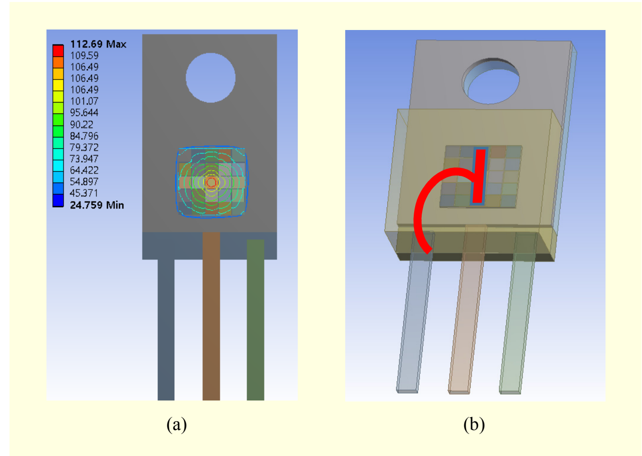


Fig. 20. Structure in ANSYS 3D model: (a) one bonding wire and (b) stripe bonding.

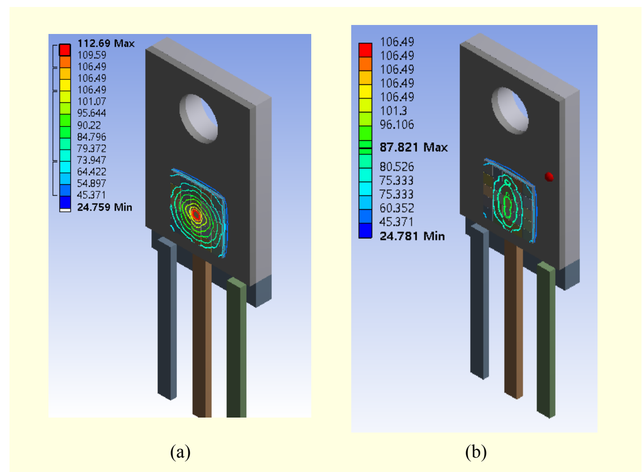


Fig. 21. Temperature distribution: (a) one bonding wire and (b) stripe bonding.

temperature characteristics were accomplished by using both SILVACO TCAD Atlas and ANSYS software [16]. It is shown that the power dissipation when $V_{\text{drain}} = 0.5$ V is concentrated at the center; the peak points for a single bonding wire, four bonding wires, and stripe bonding are shown in Figs. 16, 17, and 18, respectively.

The temperature dissipation becomes both widely and uniformly distributed as the number of bonding wires increases. The temperature dissipations for the various different bonding schemes are shown in Fig. 19.

A SPICE self-heating electrothermal model for the TO220 package supplied by the Fairchild Semiconductor company is implemented, with an area of 25 (5 × 5) mm$^2$ for a chip, consisting of TMOSFETs and resistor arrays. The junction temperature, which affects the threshold voltage and on-resistance, is measured at each TMOSFET. Then, the operating voltage is determined by a SPICE simulation. Figures 20(a)

and 20(b) show a single-bonding-wire structure and a stripe-bonding structure, respectively. The temperature distributions of both the single-bonding and stripe-bonding structures are simulated, as shown in Figs. 21(a) and 21(b), respectively. The single-bonding-wire structure has a maximum temperature of 112.69 °C at the center of the chip and a minimum temperature of 24.759 °C at the end of its leg (see Fig. 20(a)). Similarly, the stripe-bonding structure has a maximum temperature of 87.821 °C at the center of the chip and a minimum temperature of 24.781 °C at the end of its leg. These results indicate that the heat is more widely dispersed in the stripe-bonding-structure case. Both the SPICE simulation and the ANSYS package thermal simulation show similar temperature distributions. The former is considered in the design of the model for the self-heating circuit with threshold voltage and on-resistance for junction temperature (the distributions being obtained from either the chip temperature in ANSYS or the junction temperature in SPICE). For a power TMOSFET with ultra-low on-resistance [17] and high current application, temperature distributions along a vertical line through the center of the chip (see Fig. 20(b)) are similar to those for the four-bonding-wire structure; however, the stripe-bonding structure has the added advantage of reducing the cost of package assembly. Thus, the stripe-bonding structure is recommended to disperse any concentrations of high temperature.

## IV. Conclusion

The structure of an SJ TMOSFET with an embedded temperature sensor and a simulation for analyzing the characteristics of the diode-type temperature sensor were completely examined. It was found that the forward voltage of the diode-type temperature sensor linearly decreased as the temperature increased. To achieve a uniformly distributed power dissipation, distributed wire bonding with multiple wires should be used to accommodate heat at the bonding point where the current is concentrated.

When assembling the power MOSFET with ultra-low on-resistance, the number of bonding wires and their relative positions should be carefully considered so as to prevent localized current flowing. The MOSFET should be designed in consideration of both the junction temperature and the current distribution at each of the given bonding wires. Here, the appropriate number of bonding wires and schemes should be determined, considering the maximum power dissipation and the package type. The maximum temperature is limited to a certain value to guarantee the reliability of the chip. In addition, the stripe bonding scheme is strongly recommended for packaging a power MOSFET with ultra-low on-resistance.

## References


[1] B.J. Baliga, "*Advanced Power MOSFET Concepts*," NY, USA: Springer-Science, 2010, pp. 265–354.

[2] Y.H. Lho et al., "Design of Non-uniform 100-V Super-Junction Trench Power MOSFET with Low On-Resistance," *IEICE Electron. Exp*., vol. 9, no. 13, July 2012, pp. 1109–1114.

[3] B.J. Baliga, "*Fundamentals of Power Semiconductor Devices*," NY, USA: Springer-Science, 2008, pp. 279–286.

[4] D.L. Blackburn, "Temperature Measurements of Semiconductor Devices," *IEEE SEMI-THERM Symp*., Mar 9–11, 2004, pp. 70–80.

[5] H. Kock et al., "Design of a Test Chip with Small Embedded Temperature Sensor Structures Realized in a Common-Drain Power Trench Technology," *IEEE Int. Conf. Microelectronic Test Structure*, Amsterdam, Netherlands, Apr. 4–7, 2011, pp. 176–181.

[6] SILVACO TCAD Manual, Atlas, 2011.

[7] H. Dia et al., "A Temperature-Dependent Power MOSFET Model for Switching Application," *Int. Workshop Thermal Investigation ICs Syst*., Oct. 7–9, 2009, pp. 87–90.

[8] S. de Filippis et al., "ANSYS Based 3D Electro-Thermal Simulations for the Evaluation of Power MOSFETs Robustness," *Microelectronics Rel*., vol. 51, 2011, pp. 1954–1958.

[9] M. Pfost and J. Joos, "Measurement and Simulation of Self-Heating in DMOS Transistors up to Very High Temperatures," *Int. Symp. Power Semicond. Devices ICs*, Orlando, FL, USA, May 18–22, 2008, pp. 209–212.

[10] V. Košel et al., "Non-linear Thermal Modeling of DMOS Transistor and Validation Using Electrical Measurements and FEM Simulations," *Microelectronics J*., vol. 41, no. 12, Dec. 2010, pp. 889–896.

[11] M. Lofti and D. Zohir, "The Electro-Thermal Sub-circuit Model for Power MOSFETs," *Microelectronics Solid State Electron*., vol. 1, no. 2, 2012, pp. 26–32.

[12] *A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options*, *Fairchild Semicond*., *Appl*., Note AN-7510, Oct. 2003.

[13] E. Marcault et al., "Distributed Electrothermal Modeling Methodology for MOS Gated Power Devices Simulations," *Int. Conf. Mixed Des. Integr. Circuits Syst*., Gdynia, Poland, June 20–22, 2013, pp. 301–305.

[14] J.B. Sauveplane et al., "3D Electro-Thermal Investigations for Reliability of Ultra-Low ON State Resistance Power MOSFET," *Microelectronics Rel*., vol. 48, 2008, pp. 1464–1467.

[15] LTspice IV, Linear Technology Corporation, 2014.

[16] ANSYS Fluent User's Guide Release 14.0, Nov. 2011.

[17] J.B. Sauveplane et al., "Smart 3-D Finite-Element Modeling for the Design of Ultra-Low On-Resistance MOSFET," *IEEE Trans. Adv. Packag*., vol. 30, no. 4, Nov. 2007, pp. 789–794.

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