시뮬레이션 기법을 이용한 LDPC 부호와 터보부호에 대한 EXIT 차트 생성 비교

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Comparison of EXIT chart generation for LDPC and turbo codes

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요 약

본 논문에서는 반복 복호 과정에서 연판정 정보값들의 변화로 인하여 성능이 개선되는 상황을 분석하기 위하여 사용되는 EXIT(extrinsic information transfer) 차트를 LDPC 부호와 터보 부호에 대하여 생성하는 기법을 소개하고, EXIT 차트 생성과정에서 비트 오류를 제외하였을 경우 나타나는 효과에 대해 살펴보기로 한다. 본 논문에서 제시된 시뮬레이션을 이용한 EXIT 챠트 생성 기법은 매우 간단한 방법으로 반복 복호를 사용하는 오류정정부호의 정보흐름을 파악할 수 있는 효율적인 방법이다. 시뮬레이션 결과 분석을 통하여 비트 오류를 제외할 경우 지나치게 정보량이 높은 구간에서만 EXIT 챠트가 생성된다는 사실을 확인할 수 있었다.

Key Words : extrinsic information transfer (EXIT) chart, low density parity check (LDPC) codes, turbo codes, forward error correction coding (FEC), iterative decoding.

ABSTRACT

In this paper, we present two simulation methods to investigate the effect of excluding bit errors on generating the extrinsic information transfer (EXIT) chart for low density parity check (LDPC) and turbo codes. We utilized the simulation methods including and excluding bit errors to generate EXIT chart which was originally proposed for turbo codes. The generated EXIT charts for LDPC and turbo codes shows that the presented methods appropriately demonstrates the performance behaviours of iterative decoding for LDPC and turbo codes. Analysis on the simulation results demonstrates that the EXIT chart excluding the bit errors shows only a small part of the curves where the amount of information is too large.

Ⅰ. Introduction

The most powerful channel coding schemes, namely, the turbo codes and the low density parity check (LDPC) codes have in common the principle of iterative decoding [1]. The introduction of turbo codes as a tool of error-correction coding rekindle the subsequent rediscovery of LDPC codes.

LDPC codes have been the subject of many researches in recent years due to their excellent performance close to the Shannon limits [2]-[3]. Bit error rate (BER) is generally used as a measurement of the performance for forward error correction (FEC) coding schemes. In addition to this BER performance, the convergence behaviour needs to be investigated for any FEC coding scheme with iterative decoding [4].

Pioneered by Stephan ten Brink, the performance of iterative decoding in the fall-off region can be visualised by the extrinsic information transfer (EXIT) chart [5]. The EXIT chart is a semi-analytical tool which allows to visualise the decoding trajectory of iterative decoders and evaluates their convergence behaviour by measuring the mutual exchange of information between the soft-input and soft-output (SISO) of the decoder [6].

This process of information exchange is described by a characteristic transfer diagram. EXIT chart analysis

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provides a good guidance in designing effective and efficient iterative processors and codes that converge rapidly. Originally the EXIT chart was developed to analyze turbo and turbo-like codes based on convolutional codes. Subsequently, the EXIT chart has been extended to LDPC codes [7].

There are two ways of generating EXIT chart. The first one is to generate it by using mathematical formulation of information transfer based on information theory [4]. The other one is to generate it by simulations [6], and it was first attempted for turbo codes. In this method, Monte Carlo simulations are performed over an AWGN channel as in the conventional BER performance simulation system. Subsequently, two different equations to estimate amount of information are applied in the case of without and with bit error, respectively.

In this paper, we apply the method introduced in [6] to LDPC codes as well as turbo codes. For each of the case, we investigate the effect of excluding bit errors. In the case of lower signal to noise ratio (SNR), the EXIT chart excluding the bit error shows very limited region, due to excluding the bit errors.

The paper is organised in the following way. In Section II, we present simulation methods to produce EXIT charts for turbo and LDPC codes. The EXIT charts are generated by including and excluding the effect of bit errors during the simulation. Section III presents the analysis and results of the simulation methods for both LDPC and turbo codes. Finally, Section V concludes the paper.

Ⅱ. The EXIT Chart Generation with Simulations

1. Turbo Codes

EXIT chart generation for turbo codes was attempted by using a simulation method as illustrated in Fig. 1 [6]. The EXIT chart generation simulator is composed of the encoder, two component decoders, and the AWGN communication channel. The channel has noise variance of σ_{CH}^2, and each decoder is provided by a priori channel information.

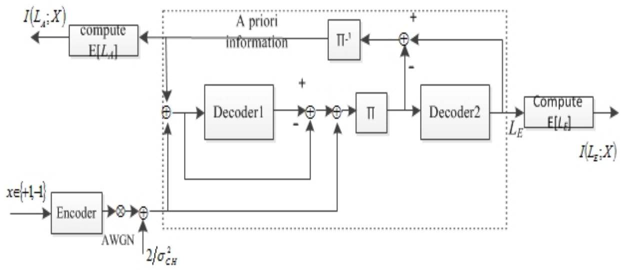

Fig. 1. Block diagram for estimating the EXIT chart of turbo codes

The two component decoders iteratively exchange soft log likelihood ratio (LLR) values in order to estimate the final decoded result. For the first half iteration the extrinsic information of decoder 1 after interleaving becomes the a priori information of decoder 2. For the next half iteration the decoders interchange their roles, i.e., the extrinsic information of decoder 2 after deinterleaving becomes a priori information of decoder 1. This allows the separate investigation and optimization of each constituent decoder. Therefore each decoder not only receives the transmitted values normalised by the communication channel state information of, $2/\sigma_{CH}^2$, but also the a priori knowledge from the other decoder [8].

With this iterative process, it is not easy to investigate how the information exchanged between decoders are evolved. By using the EXIT chart, we can visualise the mutual information between the deinterleaved extrinsic soft information into decoder 1 versus the soft output of the decoder 2. xÎ{+1,-1} are information bits which are transmitted over a noisy channel after encoding, and L_A and L_E are the a priori and extrinsic soft information of the decoder.

In an AWGN channel the inputs and the outputs of the encoder and decoder, respectively, are considered to be random variables such that X is a random variable representing the bits x of the message [9]. The measure of mutual information, $I(L;X)$ as defined by Shannon, is given as a measure of the expected value of the pointwise mutual information and the expectation is over the one parameter distribution as shown in [10].

For equally likely random variable, x and LLR's for symmetric and consistent L values, the mutual information is given as [5]:

$$\begin{aligned} I(L;X) &= 1-\int_{-\infty}^{+\infty} p(L|x=+1)\log_2\left(1+e^{-L}\right)dL \\ &= 1-E\left\{\log_2\left(1+e^{-L}\right)\right\}, \end{aligned} \quad (1)$$

where

$$p(L|x=+1) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-(L - x\sigma^2/2)^2/2\sigma^2}. \quad (2)$$

The mutual information, $I(L;X)$ in (1) can be rewritten as follows:

$$I(L;X) \approx 1 - \frac{1}{N}\sum_{n=1}^{N} \log_2\left(1 + e^{-x_n L_n}\right), \quad (3)$$

where N is the number of decoder output samples. The probability of error P_{e_n} is given by:

$$P_{e_n} = \frac{e^{+|L_n|/2}}{e^{+|L_n|/2} + e^{-|L_n|/2}} \quad . \quad (4)$$

The final estimation of the mutual information is therefore computed as follows:

$$I(L;X) \approx 1 - \frac{1}{N}\sum_{n=1}^{N} H_b\left(P_{e_n}\right)$$

$$= 1 - \frac{1}{N}\sum_{n=1}^{N} H_b\left(\frac{e^{+|L_n|/2}}{e^{+|L_n|/2} + e^{-|L_n|/2}}\right), \quad (5)$$

where $H_b(p)$ is the binary entropy function with probability of p, which can be described as follows:

$$H_b(p) = -pIog_2 p - (1-p)Iog_2(1-p). \quad (6)$$

The above new nonlinear transformation allows estimation of the mutual information only from the magnitudes without knowing the correct data. The EXIT chart is obtained by plotting the mutual relation between L_A and L_E.

2. LDPC Codes

Figure 2 shows the block diagram for estimating EXIT chart of LDPC codes using the simulation method [7]. Unlike the simulator for turbo codes, which is composed of two component decoders, the simulator for LDPC codes is composed of one decoder where information exchange is made between bit and check nodes, under the influence of AWGN communication channel with noise variance of σ_{CH}^2.

Inside the decoder there is iterative soft information exchange between the check nodes, c and the variable nodes, v. The final decision is made at the output of v. With this iterative process, investigation of information is made at the input of c as well as at the output of v, in order to investigate how the information exchanged between v and c of the decoder is evolved. In other words, L_A is measured at the input of c and L_E is measured at the output of v when encoded information are transmitted over an AWGN channel.

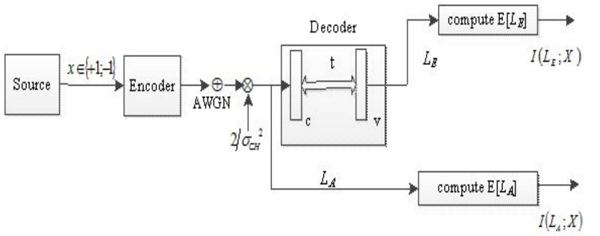

Fig. 2. Block diagram for estimating the EXIT chart of LDPC codes.

We consider that soft output values estimated at the variable and check nodes are LLR values, where the sign of a variable node message specifies the bit estimate and the magnitude indicates its level of reliability. The computation is done in the same manner as the turbo codes with and without bit errors.

Ⅲ. Results and Analysis

1. Turbo Codes

In order to see the effect of excluding the effect of bit errors during the simulation, we generated the EXIT chart for turbo codes in two ways. First, we generated the EXIT chart by including the bit error effect by using (5). Second, we generated by considering only the bits without errors with (3).

Figure 3 shows EXIT chart generated with turbo code with a code rate of 1/3 and an information length of 378 bits. Inside the turbo code, two recursive systematic convolutional (RSC) component codes with a constraint length of 3 are used. For iterative decoding algorithm, Max-log-MAP algorithm is used. In the EXIT chart, evolution of information was made by changes of SNR values in terms of bit energy to noise spectral density (E_b/N_0).

As shown in Fig. 3, in the case of turbo codes, when we exclude bit errors, we can only see only a single point, the curve where the mutual information has very high value, i.e., near to 1. This is because of the rapid saturation of turbo codes in the absence of errors. Due to this, excluding bit errors prevent us from investigating evolution of information. In addition, we can see that as the number of iteration increases, the performance of the system increases, locating the EXIT chart at the upper part.

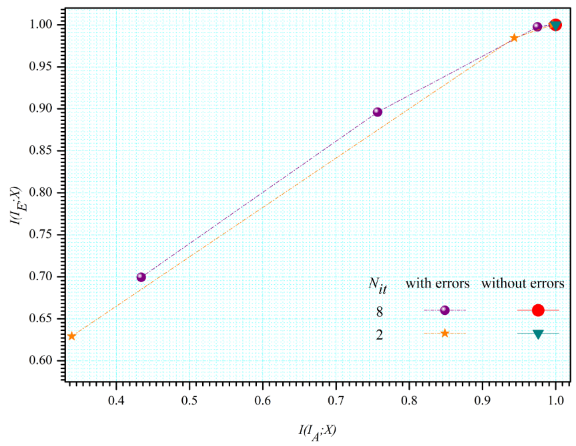

Fig. 3. EXIT chart comparison for turbo codes.

2. LDPC Codes

In the same manner as the turbo codes, including bit errors with (5) and excluding bit errors with (3), EXIT chart for LDPC code was generated using the (77,42) size compatible (SC)-array by applying a sum-product iterative decoding algorithm. As shown in Fig. 4, if we do not consider the bit error effect, we can only investigate the EXIT chart with very higher $I(L_A;X)$ versus $I(L_E;X)$ values. However, the basic trend of the chart does not change even if we do not include the bit error effect. With the same code, we can also see the EXIT chart with a larger N_{it} located in the upper part, indicating rapid revolution.

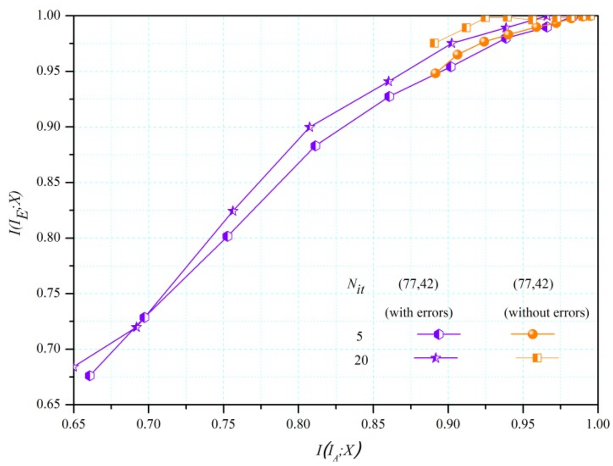

Fig. 4. EXIT chart comparison for the (77,35) LDPC code with given N_{it} values.

Fig. 5 shows the comparison of the EXIT charts for the same code by changing N_{it}, when E_b/N_0=5dB. As shown in Fig. 5, for a given $I(L_A;X)$, $I(L_E;X)$ with fixed E_b/N_0 and changing N_{it} or vice versa the trend of the curve does not change. However, by excluding bit errors, there is rapid evolution of information.

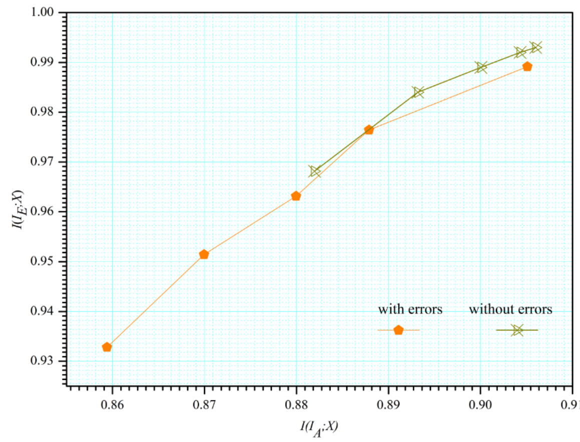

Fig. 5. EXIT chart comparison for the (77,35) LDPC code when E_b/N_0=5dB.

V. Conclusion

In this paper, we presented two simulation methods of drawing the EXIT chart for LDPC and turbo codes. We compared EXIT chart for LDPC and turbo codes with and without bit errors. The results demonstrated that excluding bit errors does not change the convergence behavior, but only higher range of the information can be investigated. In the case of turbo codes, due to the very limited investigation region in the curve, we could not see any evolution of the information if we exclude bit errors.

References

[1] A. Hasan Khan, K. C. Roy, "Comparison of turbo codes and low density parity check codes,"IOSR journal of electronics and communication engineering, vol. 6, no. 6, pp. 11-18, July-August 2013, Suresh University, Jaipur.

[2] E. Sharon, A. Ashikhmin, and S. Litsyn, "Analysis of low density parity check codes based on EXIT functions," IEEE transactions on communications, vol. 54, no. 8, pp. 1407-1414, August 2006.

[3] E. Sharon,"Analysis of belief propagation decoding of LDPC codes over the biAWGN channel using improved Gaussian approximation based on the mutual information measure," IEEE conference on electrical and electronics engineering, pp. 262-264, 1 December 2002, Israel.

[4] S. T. Brink, "Convergence behaviour of iteratively decoded parallel concatenated codes," IEEE transactions on communications, vol. 49, no. 10, pp. 1727-1737, October 2001.
[5] J. Hagenauer, "The EXIT chart-introduction to extrinsic information transfer in iterative processing,"IEEE conference on signal processing, pp. 1541-1548, 6-10 September 2004, Vienna.
[6] R. M. Nyamukondiwa, M. Zhang, and S. Kim, "EXIT chart generation for LDPC codes," accepted for presentation at International symposium on information technology convergence conference (ISITC), 15–17 October, 2015, Tianjin, China.
[7] R. M. Nyamukondiwa, M. Zhang, and S. Kim, "Effect of excluding bit errors on generating EXIT chart," 2015년도 제1회 한국위성정보통신학회 국내학술발표대회 논문집 제1권1호, pp. 32-33, 제주대학교, 2015년 6월 23일-24일
[8] J. Hagenauer, "The turbo principle in mobile communications," International symposium on information theory and its applications, 7–11 October, 2002. Xi'an, PRC.
[9] A. Farchane, M. Belkasmi, and A. Azouaoui, "EXIT chart for iterative decoding of product and concatenated block codes," International journal of computer science issues (IJCSI), vol. 10, no.2, pp. 1694-0784, July 2013.
[10] D. J. MacKay and R. M. Neal, "Near shannon limit performance of low density parity check codes," Electronics Letters, vol. 32, no. 18, pp. 1645–1646, 1996.

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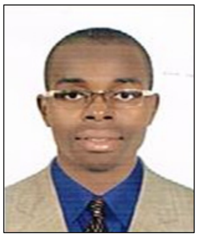

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