Design of Multi-time Programmable Memory for PMICs

Yoon-Kyu Kim, Min-Sung Kim, Heon Park, Man-Yeong Ha, Jung-Hwan Lee, Pan-Bong Ha, and Young-Hee Kim

In this paper, a multi-time programmable (MTP) cell based on a 0.18 μm bipolar-CMOS-DMOS backbone process that can be written into by using dual pumping voltages — VPP (boosted voltage) and VNN (negative voltage) — is used to design MTP memories without high voltage devices. The used MTP cell consists of a control gate (CG) capacitor, a TG_SENSE transistor, and a select transistor. To reduce the MTP cell size, the tunnel gate (TG) oxide and sense transistor are merged into a single TG_SENSE transistor; only two p-wells are used — one for the TG_SENSE and sense transistors and the other for the CG capacitor; moreover, only one deep n-well is used for the 256-bit MTP cell array. In addition, a three-stage voltage level translator, a VNN charge pump, and a VNN precharge circuit are newly proposed to secure the reliability of 5 V devices. Also, a dual memory structure, which is separated into a designer memory area of 1 row × 64 columns and a user memory area of 3 rows × 64 columns, is newly proposed in this paper.

Keywords: PMIC, multi-time programmable, dual memory.

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I. Introduction

Power management integrated circuits (PMICs) receive input power from an information device, such as a mobile phone, a laptop computer, a TV, or a monitor, and convert and supply a stable, effective level of power to the host system [1]. PMICs require an Electrically Erasable Programmable Read-Only Memory (EEPROM) IP performing a soft-start time setting for the protection of circuits and enhancement of operating reliability with respect to the determination of a power-on and power-off sequence, setting of an output voltage, setting of an output pull-down resistance, setting of an inductor current limit, and the inrush current of each converter in the multiple converter.

In general, a non-volatile memory (NVM) for PMICs using side-wall selective transistor cells (SSTCs) [2] (namely, double poly EEPROM cells — the cell sizes of which are about 0.99 μm^2) requires five to eight extra mask layers with a bipolar-CMOS-DMOS (BCD) backbone process. Thus, the NVM IP used for PMIC chips uses multi-time programmable (MTP) cells (namely, single poly EEPROM cells — the cell sizes of which are several tens of μm^2 or so) and usually requires one or two additional mask layers. Since MTP memory needs only a simple process and is cost-effective, it is widely used in PMICs [3].

The characteristics of recently published MTP memory IPs are compared in Table 1. For an MTP cell using a logic process, a peripheral circuit can be designed with 5 V or 3.3 V transistors. 5 V transistors are used as medium voltage (MV) devices in MTP memory IPs [3]–[6] for PMICs and 3.3 V transistors in MTP memory IPs [7] for radio-frequency identification (RFID) tag chips. A conventional MTP cell for

Table 1. Comparison of MTP IP characteristics.

Ref no.	Memory process	Cell size	Tunnel oxide thickness	Erase voltage	Program voltage
[3]	0.35 μm BCD	37.7	125 Å	15 V	18.5 V
[4]	0.13 μm Logic	12.1	85 Å	12 V	12 V
[5]	0.18 μm BCD	2	110 Å	9 V	5.5 V
[6]	0.25 μm Logic	62.5	85 Å	9 V	5.5 V
[7]	0.13 μm Logic	N/A	70 Å	7 V	7 V

PMICs requires an additional device of either a high voltage (HV) or parasitic HV, or an LDMOS transistor, to secure the reliability of 5 V devices since the erase or program voltage is above 9 V. In addition, the cell size increases since the tunnel oxide capacitor and sense transistor exist separately. Also, there are the disadvantages of a longer writing time and higher test cost since the effective capacitance of the coupling capacitor (CC) is small.

With regards to MTP memories for PMICs that are mounted on the display modules of mobile phones, design techniques for a dual memory structure for the trimming of analog circuits in both PMIC chips and in display driver chips used by users are required. In addition, the PMIC used in a mobile phone can read out an MTP cell datum with an external voltage of 1.8 V or so at power-up and should do a trimming of analog circuits including the bandgap reference voltage generator. Thus, MTP memories for PMICs require a design technique of a wide operating voltage range of 1.8 V to 5.5 V in read modes. In addition, the design of a peripheral circuit having a V_T measuring function of an MTP cell is required.

In this paper, an MTP cell that can be written into by using dual pumping voltages — VPP and VNN — is used to design MTP memories without HV devices based on a 0.18 μm BCD backbone process. The used MTP cell consists of a control gate (CG) capacitor, a TG_SENSE transistor, and a select transistor [8]. While the TG_SENSE transistor functions as a tunnel gate (TG) transistor that initiates a Fowler–Nordheim (FN) tunneling process through a tunnel oxide of 82 Å in the erase and program modes, it operates as a sense transistor in read mode. To reduce the MTP cell size, the TG oxide and sense transistor are merged into a single TG_SENSE transistor; only two p-wells (PWs) are used — one for the TG_SENSE and sense transistors and the other for the CG capacitor; moreover, only one deep n-well (DNW) is used for the 256-bit MTP cell array. In addition, both the drain-source voltage (VDS) and the gate-source voltage (VGS) of MV devices should be applied with 7.5 V and 10 V or so to design a circuit with only MV devices of 5 V and to secure the reliability of devices without HV devices. Thus, a three-stage voltage level translator, a VNN charge pumping circuit, and a VNN precharge circuit are newly proposed in this paper to guarantee the reliability of devices.

The dual memory structure proposed in this paper is separated into a designer memory area of 1 row × 64 columns and a user memory area of 3 rows × 64 columns. While the reading and latching of 64-bit parallel datum is made simultaneously at a low voltage of 1.8 V for the designer memory, the user memory can be read out byte by byte and can be used for the analog trimming of the display driver chips through the I^2C interface. The dual memory structure provides users with a greater level of convenience of use compared to when a conventional single memory structure is used. In addition, this can be operated as a single memory structure in applications that require no user-memory area. Thus, a switchable MTP memory structure between dual and single memory structure modes is newly proposed.

A parallel data (PD) buffer functioning as a data latch is newly proposed as well. MTP memories for PMICs can be operated at a low voltage within the wide voltage range of 1.8 V to 5.5 V in read mode. The cell size of the proposed MTP memory based on a 0.18 μm Magnachip Semiconductor process is 5.5 μm × 6.0 μm (= 33 μm^2), and the layout size of the 256-bit MTP memory IP is 480 μm × 668.89 μm (= 0.321 mm^2).

II. Circuit Design

A conventional MTP cell and its layout image are shown in Fig. 1. The layout size of the conventional MTP cell is 4.575 μm × 8.25 μm (= 37.74375 μm^2) [3]. Erasing and programming of the MTP cell is carried out using an FN tunneling process [3] through the tunnel oxide under the floating gate (FG). In Fig. 1, the operation of ejecting electrons from the FG is *erasing* and that of injecting electrons into the FG is *programming*. In the erase mode, electrons are ejected from the FG by the FN tunneling process if the word line (WL)

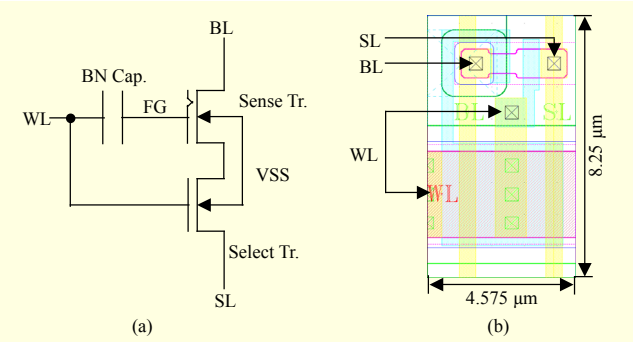

Fig. 1. Conventional MTP cell: (a) circuit and (b) layout image [3].

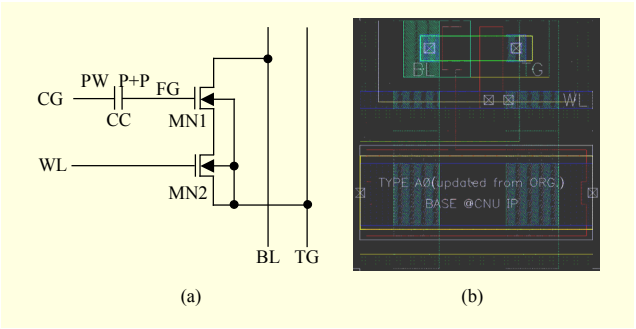

Fig. 2. MTP cell: (a) circuit and (b) layout image.

and bit line (BL) of a selected cell are applied with 0 V and 15 V, respectively. In the program mode, electrons are injected to the FG via FN tunneling if the WL and BL of the selected cell are applied with 18.5 V and 0 V, respectively. The source line (SL) is in a floating state in the write modes and 0 V in the read modes. The conventional MTP cell requires an additional HV transistor to secure the reliability of 5 V devices since the erase and program voltages are 15 V and 18.5 V, respectively.

As shown in Fig. 2(a), an MTP cell used in this paper consists of a CG CC of PW-P+P structure, a TG_SENSE transistor (MN1), and a select transistor (MN2) to reduce off-leakage current on BL when over-erased. To reduce the size of the MTP cell with a generic CMOS process, the DNW of the 256-bit MTP memory cell array is shared and the number of used CMOS devices is just three. Also, the PWs of the TG_SENSE and select transistors are shared. While the TG_SENSE transistor serves as a TG transistor for FN tunneling in the erase and program modes, it operates as a sense transistor in the read modes. If the PW and NW in the array are butted directly, the well junction can be broken down by the well junction BV between the PW and NW in the DNW in the write modes. To increase the BV of the well junction, the DNW is left as it is by keeping the well spacing between the PW and NW to 0.6 μm without any additional mask instead of a direct butting. In this way, the well-junction BVs of the PW and NW can be secured at above 20 V. While the TG_SENSE transistor functions as a TG transistor starting the FN tunneling through the tunnel oxide of 82 Å in the erase and program modes, it operates as a sense transistor in the read mode. In addition, the MTP cell can be erased or programmed through MN2 and can achieve a tunnel oxide thickness of 82 Å via FN tunneling. In addition, the gate oxide thicknesses of the CC capacitor and the MN2 transistor is 125 Å; namely, the gate oxide thickness of a 5 V transistor. The layout size of an MTP cell based on a 0.18 μm process is 5.5 μm × 6 μm (= 33 μm^2). Figure 2(b) shows its layout image.

The cell bias voltages of the MTP cell according to the operation modes are applied as follows. In the erase mode, electrons are ejected from the FG by the FN tunneling if the CG and TG of the selected cell are applied with –6.5 V and +6.5 V, respectively. In the program mode, electrons are injected to the FG by the same FN tunneling process if the CG and TG of the selected cell are applied with +6.5 V and –6.5 V, respectively. In the read mode, while the BL of the erased cell outputs 0 V, that of the programmed cell is changed to VRD-V_T through a pull-up resistor due to the V_T loss of the NMOS transistor; namely, the BL switch. To prevent a disturbance effect on the FG of the non-selected cells due to the CG and TG voltages of the selected cells, the non-selected CG and non-selected TG are biased at VPPL (= VPP/3) and VNNL (= VNN/3), respectively. In the erase mode, the non-selected CG and non-selected TG are biased at VPPL and VNNL, respectively. Also, in the program mode, the non-selected CG and non-selected TG are biased at VNNL and VPPL, respectively. Furthermore, to prevent a read disturbance effect, the BL voltage is developed to a difference equation, which is below 1.5 V, in the read modes. Table 2 compares the proposed MTP cell to its conventional counterpart. The most notable improvement of the proposed MTP cell is the reduction in the number of additional masks.

Table 2. Comparing proposed MTP cell with its conventional counterpart.

Items		Conventional	Newly proposed
Process		MC 0.35 μm BCD	MC 0.18 μm BCD
Cell size		37.74375 μm^2	33 μm^2
No. of additional masks		3	1
VDD	Read	2.5 V–5.5 V	1.8 V–5.5 V
	Write	2.5 V–5.5 V	3.0 V–5.5 V
Temperature		–40°C–85°C	–40°C–125°C
Write time		5 ms	5 ms
Endurance		1 K cycles	1 K cycles
Retention		10 years	10 years

For MTP memories for PMIC chips mounted on the display modules of mobile phones, users require a dual memory structure for the trimming of analog circuits in both PMIC chips and in display driver chips used by them. Thus, the proposed dual memory structure in this paper is divided into a designer memory area of 64 bits and a user memory area of 192 bits. The designer memory can be read out and latched at the same time in 64-bit units in parallel. The trimming of analog circuits comprising a bandgap reference voltage generator designed inside the PMIC chips is done through the latched parallel datum. On the other hand, the user memory can be read out in 8-bit units and is used for the trimming of the

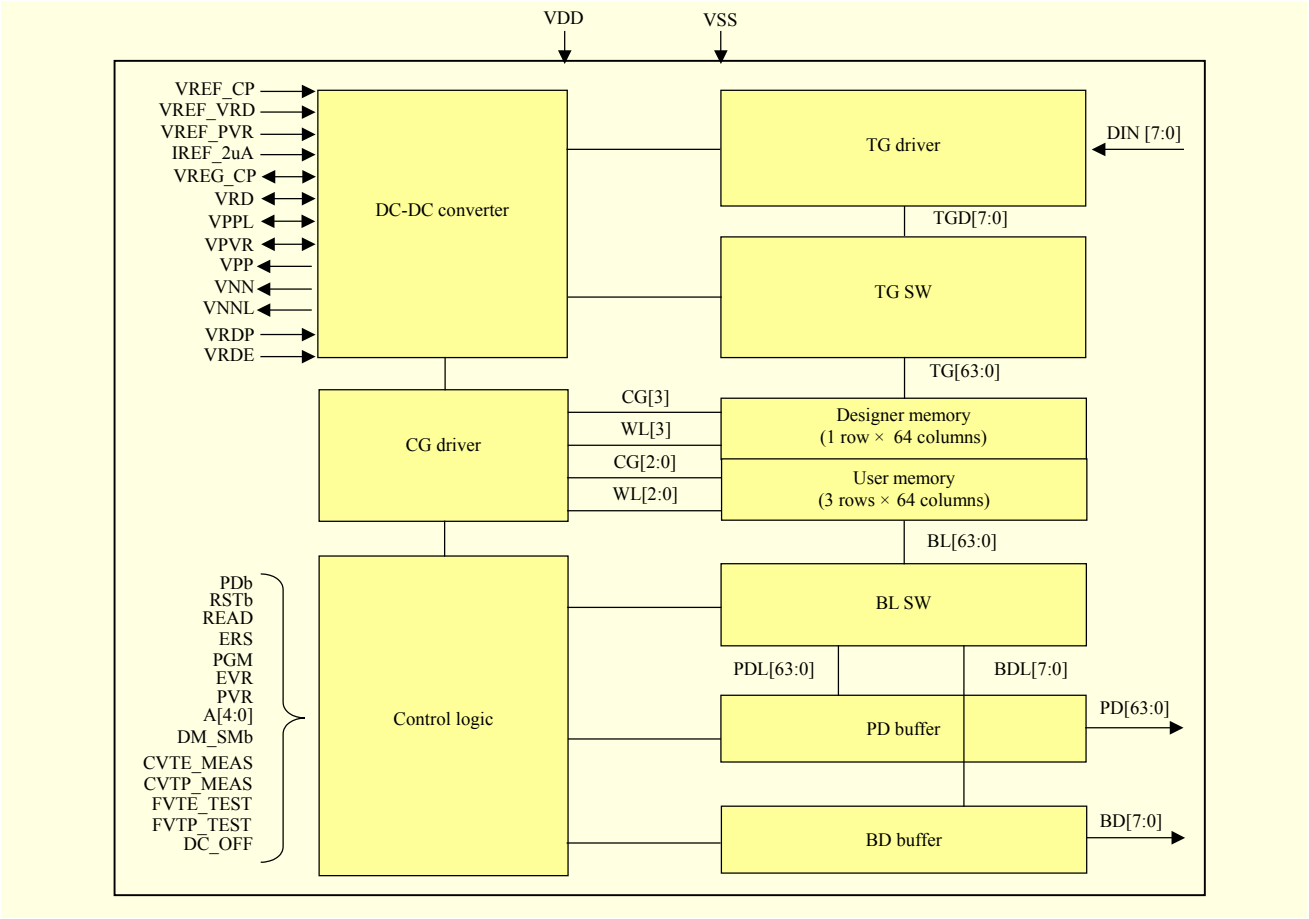

Fig. 3. Block diagram of designed 256-bit MTP IP.

display driver chips through the I^2C interface. A dual memory structure, which is switchable to a conventional memory structure in applications requiring no user-memory area, is newly proposed.

In Table 3, we summarize the major specifications of the 256-bit MTP memory IP designed with the proposed MTP cells in Fig. 2. The cell array is arranged in 4 rows by 64 columns. A single power supply of VDD is used. There are read (PD read and byte data (BD) read), write (erase and program), write-verify-read (program-verify-read and erase-verify-read), and other (stand-by, power-down, and reset) modes as operation modes. The range of VDD is 1.8 V to 5.5 V in the read modes and 3 V to 5.5 V in the write and write-verify-read modes. The write time of the MTP memory IP is 5 ms and the access time is 500 ns.

As shown in Fig. 3, the designed 256-bit MTP memory IP consists of an MTP memory cell array of 4 rows × 64 columns; a CG driver circuit selecting one of four rows by decoding the row address A[4:3] and supplying a voltage to the corresponding WL and CG nodes; a BL switch (SW) circuit transferring a BL[63:0] datum to program data line (PDL)[63:0] and BDL[7:0] by demultiplexing in the read modes; a PD buffer reading out a PDL[63:0] datum; the BD buffer reading out a

Table 3. Major specifications of 256-bit MTP IP.

Items		Main features
MTP cell array		4 rows × 64 columns
Cell type		Single poly EEPROM cell
VDD	Read	1.8 V–5.5 V
	Write	3.0 V–5.5 V
	Write-verify-read	3.0 V–5.5 V
Operating mode	Read	PD read/BD read
	Write	Erase /Program
	Write-verify-read	EVR/PVR
	Others	Stand-by/power-down/reset
Temperature range		–40°C–125°C
Write time		5 ms
Access time		500 ns

BDL[7:0] datum; a TG driver; and a control logic that supplies internal control signals that are suitable for the operational modes. There are PDb, RSTb, READ, ERS, PGM, EVR, and PVR as input control signals. In addition, the dc-dc converter generates VPP (= +6.5 V), VNN (= –6.5 V), VPPL (= +2.17 V), and VNNL (= –2.17 V) required for erasing and programming. When the cell datum selected by the row decoding of A[4:3] is developed on BL[63:0], the BL SW in Fig. 3 distributes the developed datum according to the selected memory area. While BL[63:0] is transferred to PDL[63:0] if the designer memory area is selected, a selected byte datum of BL[63:0] by the column decoding of A[2:0] is transferred to BDL[7:0] when the user memory area is selected. In Fig. 3, writing is done byte by byte. Selection of the dual or single memory can be made according to dual memory or single memory bar (DM_SMb), which can be applied with VDD or 0 V.

The VDS and VGS of MV devices should be applied with 7.5 V and 10 V (or so), respectively, to design a circuit with just MV devices of 5 V and to secure the reliability of devices without HV devices. In the conventional CG driver in Fig. 4, there is no problem with the reliability of devices, since the maximal VDS voltage of 5 V transistors is 6.5 V in the case that the inhibit voltage is 0 V in the write modes. However, there is a problem in that the CG driver can be applied with a voltage greater than the drain-source breakdown voltage (BVDSS) of 5 V MOS transistors in the write modes since the CG driver is applied with a VDS of 8.67 V in the write modes in the case when the inhibit voltages of VPPL and VNNL are used. Thus, a three-stage voltage level translator is newly proposed to secure the reliability of devices.

As shown in Fig. 5, a CG driver is newly proposed using three-stage voltage-level shifters (VRD - VNNL_CG, ROW_HV - VNNL_CG, and ROW_HV - ROW_LV) to have a switching voltage under BVDSS. Additionally, three PMOS transistors — MP4, MP5, and MP6 — with their gates connected to GND and three NMOS transistors — MN4, MN5, and MN6 — with their gates connected to NG_VRD are added; namely, a switching power supply. The VDS voltage of each MOS device in the third voltage-level shifter can be limited below 6.5 V by these six additional transistors. In addition, there is no problem with the gate oxide BV even if the voltages between gate and source for some transistors such as MN1, MN2, and MN3 in the erase mode are applied with 8.17 V (= 2.17 V to –6 V). Also, since the TG driver in Fig. 6 uses three stages like the CG driver, it is designed such that the maximal VDS voltage applied to the 5 V devices is below 6.5 V.

The PD buffer to latch a PDL datum and then output it to the PD port is shown in Fig. 7(a). PDL is precharged to VDD

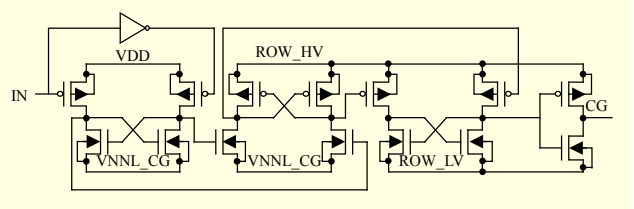

Fig. 4. Conventional CG driver.

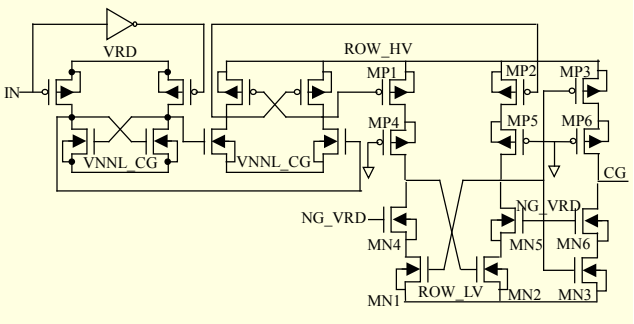

Fig. 5. Newly proposed CG driver.

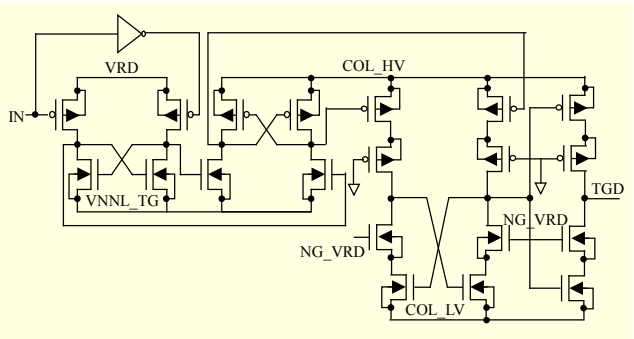

Fig. 6. Newly proposed TG driver.

by the PMOS transistor MP0 if a short pulse is applied to PDL_PCGb before WL is activated in the read modes. Then, as WL is activated, PDL keeps VDD for a programmed cell since there is no current over it while PDL is almost 0 V for an erased cell (because of on-current over it). After a to-be-read PDL datum is sufficiently transferred to PDL, the PDL datum can be output if PDL_SAENb is enabled. MP1, a load transistor of high impedance, functions as an active load to prevent the PDL from dropping to a low level by the leakage currents of the MTP cells connected to BL through the BL switch if the programmed cells are selected in the read modes. Also, MN0 keeps the PDL voltage at $-V_T$ in the program mode. Figure 7(b) shows the BD buffer, which latches the BDL datum and outputs it to the BD port. A tri-state buffer is connected in the next stage of the D latch. In V_T measuring mode, the selected MTP cells flow current to the BD port through the MN1 transistor in Fig. 7(b) as the tri-state buffer stays in a high-impedance state if CVT_MEAS increases to an HV.

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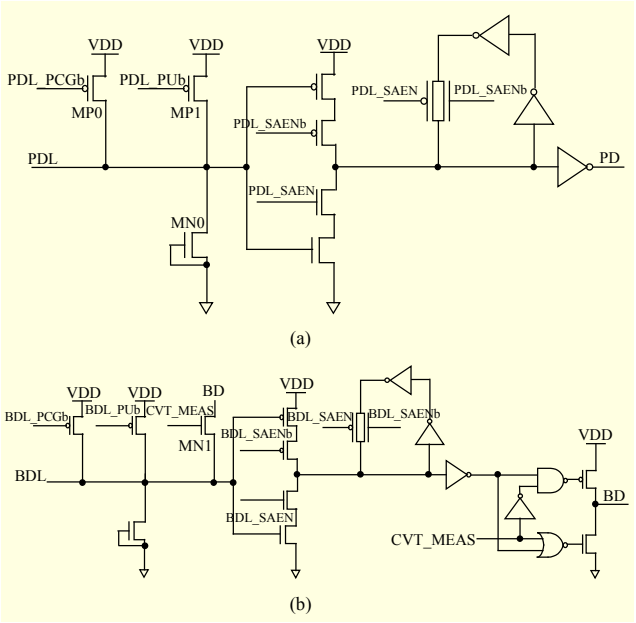

Fig. 7. Circuit of data output buffer: (a) PD buffer and (b) BD buffer.

Table 4. Output voltages of dc-dc converter according to operation mode.

Operating mode	VREG_CP	VRD	VPP	VNN	VPPL	VNNL	VPVR
Read	0 V	1.4 V–1.6 V	VDD	0 V	VDD	0 V	2.3 V–2.5 V
Erase	1 V–1.083 V	1.4 V–1.6 V	6 V–6.5 V	–6 V––6.5 V	2 V–2.17 V	–2 V––2.17 V	2.3 V–2.5 V
Program	1 V–1.083 V	1.4 V–1.6 V	6 V–6.5 V	–6 V––6.5 V	2 V–2.17 V	–2 V––2.17 V	2.3 V–2.5 V
EVR	0 V	1.4 V–1.6 V	VDD	0 V	VDD	0 V	2.3 V–2.5 V
PVR	0 V	1.4 V–1.6 V	VDD	0 V	VDD	0 V	2.3 V–2.5 V
Stand-by	0 V	1.4 V–1.6 V	VDD	0 V	VDD	0 V	2.3 V–2.5 V
Reset	0 V	1.4 V–1.6 V	VDD	0 V	VDD	0 V	2.3 V–2.5 V
Power-down	0 V	VDD	VDD	0 V	VDD	0 V	VDD

The designed dc-dc converter consists of low-dropout (LDO) regulators — VPPL, VRD, VPVR, and VREG_CP — and charge pump circuits — VPP, VNN, and VNNL. VREG_CP supplies a regulated voltage of 1 V to 1.083 V and is used as a reference voltage for the charge pump circuits. Read voltage (VRD) is the CG voltage selected in the read modes and supplies 1.4 V to 1.6 V, except in power-down mode (as shown in Table 4). VPPL is used as the positive inhibit voltage in the write modes and supplies a regulated voltage of 2 × VREG_CP. Program-verify-read voltage (VPVR) is used as a voltage for the margin test of programmed cells in the program-verify-read mode and supplies a voltage of 2.3 V to 2.5 V, which is at least 0.7 V higher than VRD. VPP and VNN are generated to be 6 × VREG_CP and –6 × VREG_CP by a negative feedback mechanism. VNNL is used as the negative inhibit voltage in the same way as VPPL in the write modes and supplies –2 × VREG_CP by a negative feedback mechanism.

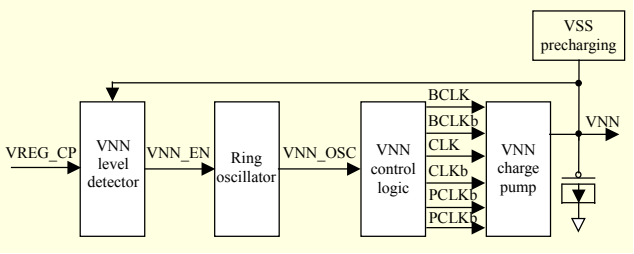

Fig. 8. Block diagram of VNN charge pump.

A block diagram of the designed VNN charge pump is shown in Fig. 8. The VNN generator consists of a 7-stage VNN charge pump, a control logic, a ring oscillator, and a level detector. The conventional negative charge pump using HV devices is as shown in Fig. 9. In the case where the G4 voltage of MT4 (namely, the charge transfer switch in the last pumping stage is VDD in the steady state when CLK is 0 V) and VNN reaches the target voltage, the voltage between both terminals of the gate oxide can be applied by an over-voltage of 12 V since VDD is 5.5 V and VNN is –6.5 V in the worst-case scenario. Thus, there is a disadvantage of requiring additional masks due to the uses of HV devices and metal–insulator–metal (MIM) capacitors in the conventional charge pump.

To secure the reliability of the used 5 V devices instead of HV devices, the first-stage VNN charge pump and other following unit charge pumps are designed differently. In the VNN charge pump, an over-voltage can be applied since the pumping voltage of each stage decreases with respect to higher VNN output stages. On the other hand, charge transfer is better for higher gate voltage in the first-stage charge pump since the pumping voltage is low. In consideration of these factors, G1 and G2 of the first-stage charge pump in Fig. 10(a) turn on the charge transfer switches MN1 and MN2, respectively, by VPPL (= 2.17 V); namely, the LDO output voltage, instead of the external VDD. On the other hand, G3 of the unit charge pumps connected in cascade in Fig. 10(b) from the second stage onward is applied with VSS and turns on the charge transfer switch MN3. As such, the voltage between both terminals of the gate oxide can be reduced when the charge transfer switches are turned on since VSS is applied instead of

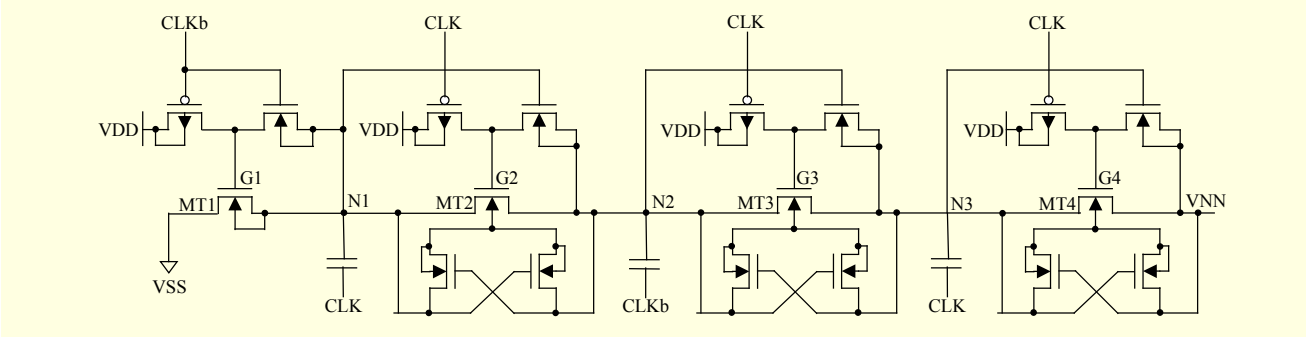

Fig. 9. Conventional VNN charge pump.

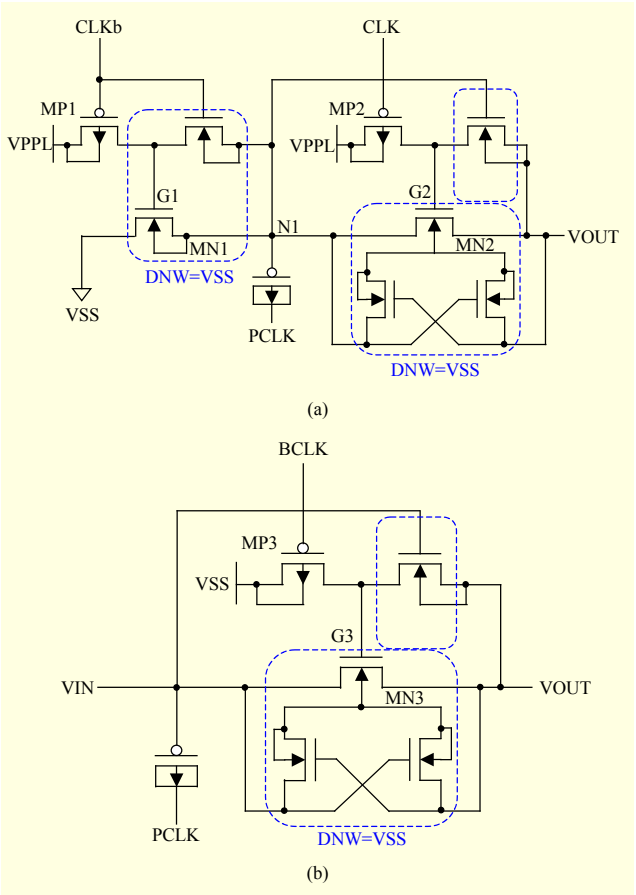

Fig. 10. Newly proposed VNN charge pump: (a) 1st-stage charge pump and (b) unit charge pump.

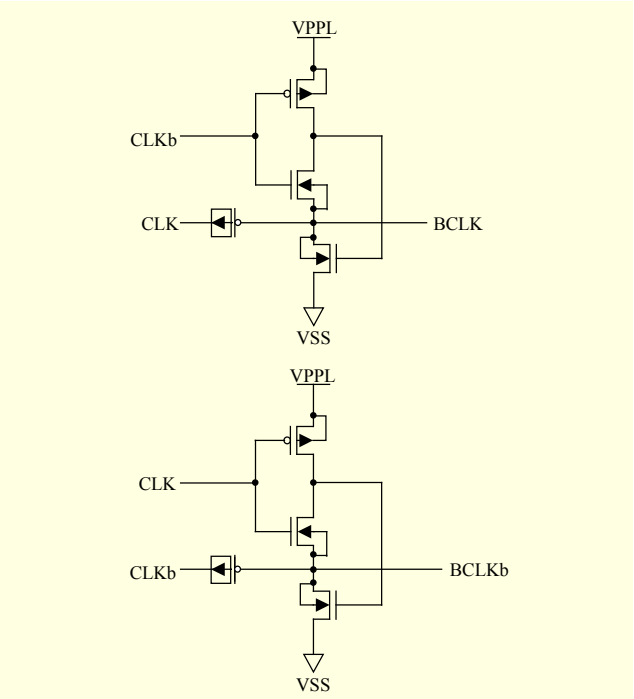

Fig. 11. Circuit of boosted clock generator.

VDD. In addition, the negative boosted clock is used for the gate voltage of MP3 to supply VSS to G3. Furthermore, the layout size can be reduced by using a PMOS capacitor having great capacitance per unit area instead of an MIM capacitor without any additional masks. Thus, if a 5 V PMOS capacitor is used, then an HV can be applied to both terminals of the gate oxide of the pumping capacitor in the final stage when PCLK is high. To solve this problem, VPPL is used for PCLK and PCLKb instead of VDD, as shown in Fig. 11.

The VNN level detector proposed in Fig. 12 is used to pump VNN, which is invariant to PVT variations. The VNN level detector controls the VNN charge pump by comparing VSS (virtual ground) with VFB_VNN, which is a voltage divided by M (= 6) NMOS transistors using a PMOS OP-AMP. In the write modes, VFB_VNN is a divided voltage of (VREG_CP-VNN)/7 and becomes 0 V in the steady state. If VFB_VNN becomes 0 V, then VNN becomes the target voltage of −6.5 V (= −6 × VREG_CP). The VNNL level detector is the same as the VNN level detector except that M is changed from six to three in the NMOS voltage divider. Since VREG_CP is generated with a LDO circuit using VREF_CP invariant to PVT variations, VPP, VNN, and VNNL are also invariant to PVT variations.

For the proposed VNN precharge circuit in Fig. 13, MN2 is

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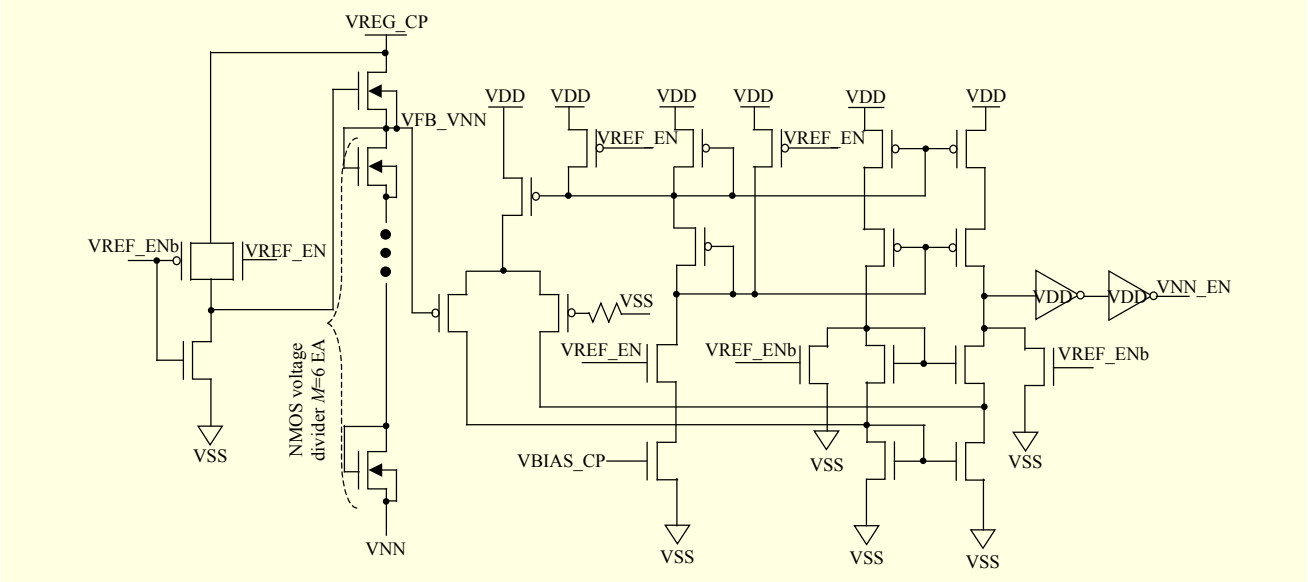

Fig. 12. Newly proposed VNN level detector.

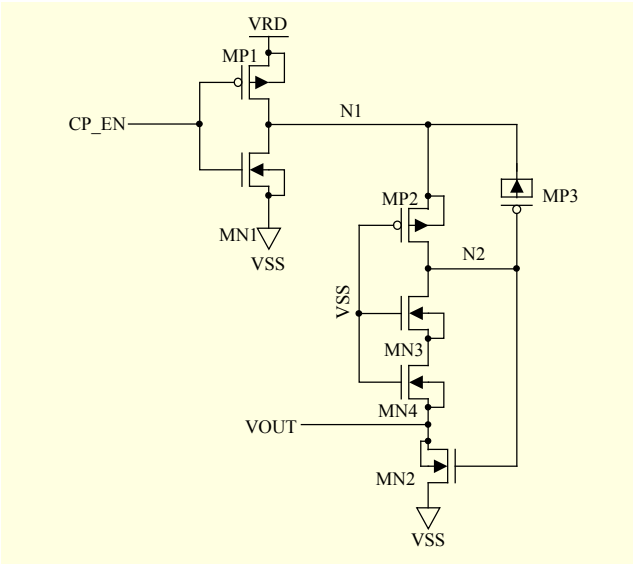

Fig. 13. Proposed VNN precharging circuit.

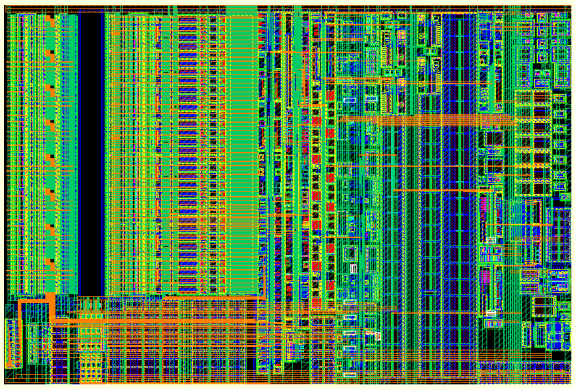

Fig. 14. Layout image of designed 256-bit MTP IP.

turned off and the voltages between the gates and the sources of MN3 and MN4 stay below 6.5 V at the same time as the node voltage of N2 is coupled from VRD (= 1.5 V) to 0 V by the capacitive coupling of a PMOS transistor, MP3, in entering the write modes. Also, the voltage between the source and the drain of MP2 stays below 6.5 V by the capacitive coupling of MP3 in exiting from the write modes. The reason for connecting MN3 and MN4 in series is also to keep the voltage between the drain and the source of each NMOS transistor under 6.5 V in exiting from the write modes.

Figure 14 shows the layout image of the designed 256-bit MTP memory IP with a 0.18 μm generic Magnachip Semiconductor process, and the layout size is 480 μm × 668.89 μm (= 0.321 mm^2).

III. Measurement Results

Figure 15 shows V_T measurement results for the manufactured MTP cells based on a 0.18 μm process with respect to the number of write cycles and with program voltages as a parameter. The figure shows the measured curves of V_T characteristics according to splits of the program voltage, ±6 V and ±6.5 V, in CG and TG, with a write time of 5 ms. It can be seen that the erase V_T decreases and the program V_T increases as the program voltage increases. After 1,000 erasing/writing cycles at a program voltage of ±6 V with a write time of 5 ms, the V_T of a programmed cell is lowered from 2.92 V to 2.9 V and the V_T of an erased cell is raised from –1.3 V to –0.5 V.

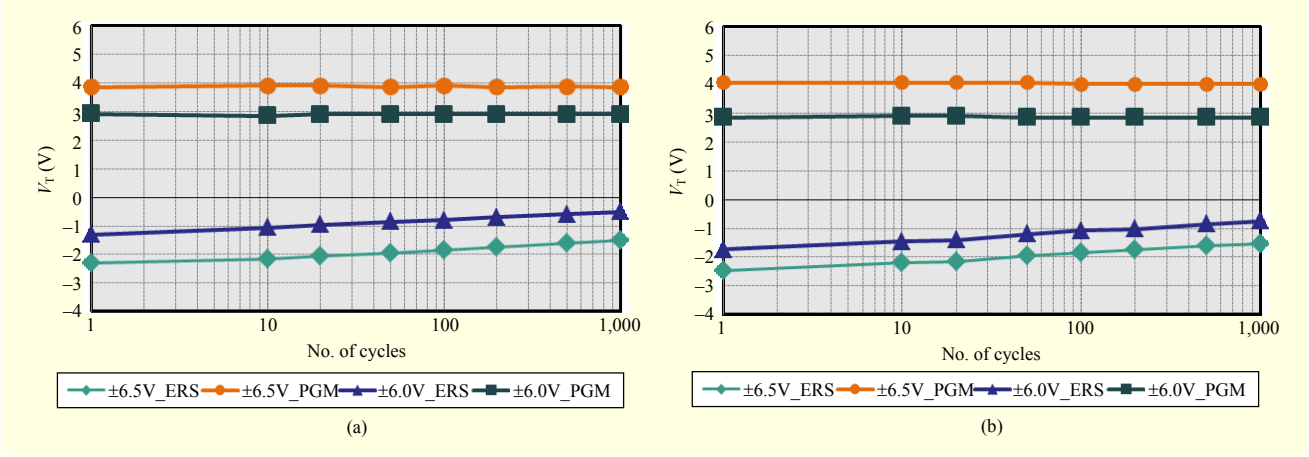

Fig. 15. V_T measurement results of manufactured MTP cells with respect to program voltages: (a) temp = 25°C and (b) temp = 125°C.

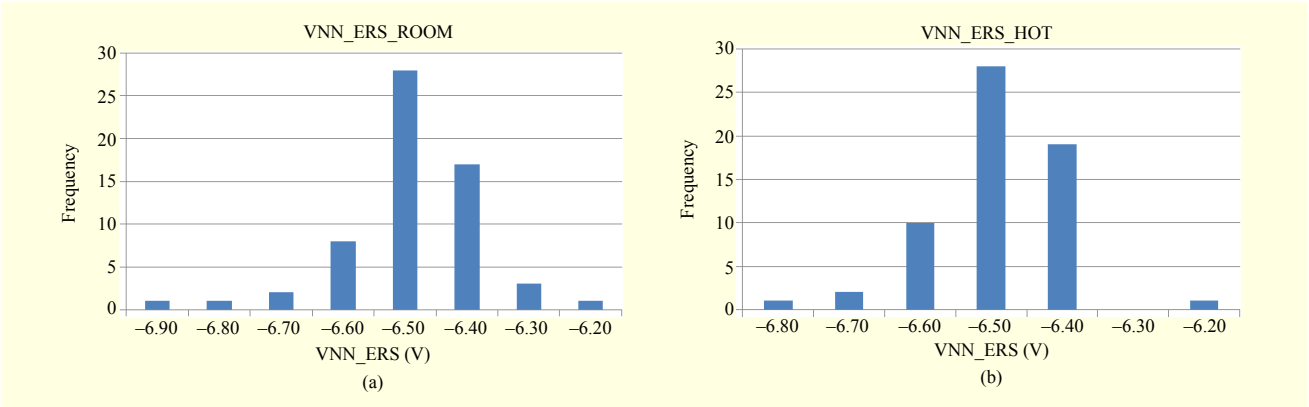

Fig. 16. Measurement results of VNN in erase mode with respect to temperatures: (a) temp. = 25°C and (b) temp. = 125°C.

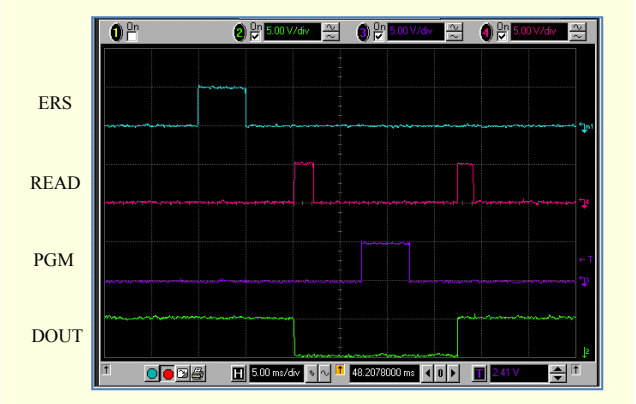

Fig. 17. Measured waveforms of 256-bit MTP memory test chips.

Figure 16 shows a frequency plot of the measured VNN voltages in the erase mode over 61 test chips at a room temperature of 25°C and at a hot temperature of 125°C. The average and three-sigma of VNN voltages are –6.539 V and 0.317 V, respectively, at the room temperature. At the hot temperature, they are –6.54 V and 0.272 V, respectively. In the program mode, VNN results are similar to those in the erase mode. Good results that can be applied to MTP memory IPs are obtained.

Figure 17 shows measured waveforms for the manufactured 256-bit MTP memory IP based on a Magnachip Semiconductor 0.18 μm process. When a series of erase, read, program, and read operations are performed continuously, it is confirmed that an erased MTP cell outputs "0" and a programmed cell outputs "1."

IV. Conclusion

PMIC chips require simple-process and cost-effective MTP memory IPs that can perform a soft-start time setting for the protection of circuits and enhancement of operational reliability from a sequence determination of power-on and power-off; output voltage setting; output pull-down resistance setting; inductor current limit setting; and inrush current of each converter among multiple converters.

In this paper, an MTP cell that can be written into by using dual pumping voltages — VPP and VNN — is used to design MTP memories without HV devices based on a

0.18 μm BCD backbone process. The used MTP cell consists of a CG capacitor, a TG_SENSE transistor, and a select transistor. To reduce the MTP cell size, the TG oxide and the sense transistor are merged into a single TG_SENSE transistor; only two PWs are used — one for the TG_SENSE and sense transistors and the other for the CG capacitor; and only one DNW is used for the 256-bit MTP cell array. In addition, a three-stage voltage level translator, a VNN charge pump, and a VNN precharge circuit are newly proposed to secure the reliability of 5 V devices.

Also, a dual memory structure, which is separated into a designer memory area and a user memory area, is newly proposed in this paper. While the reading and latching of 64-bit parallel datum is made simultaneously at a low voltage of 1.8 V for the designer memory, the user memory can be read out byte by byte and can be used as the analog trimming of the display driver chips through the I^2C interface. The dual memory structure can give user's convenience of use compared with a conventional single memory structure. Thus, a switchable MTP memory structure that is capable of switching between dual and single memory structures is newly proposed.

It is required that MTP memories used in PMICs operate at a low voltage, within the wide voltage range of 1.8 V to 5.5 V, in read modes. Also, a PD buffer functioning as a data latch is also newly proposed. The proposed MTP cell size based on a Magnachip Semiconductor 0.18 μm process is 5.5 μm × 6.0 μm (= 33 μm^2), and the layout size of the designed 256-bit MTP IP is 480 μm × 668.89 μm (= 0.321 mm^2).

It can be seen by the measurement results of V_T characteristics for the manufactured MTP cells with a 0.18 μm process that the erase V_T decreases and the program V_T increases as the program voltage increases according to splits of the program voltage, ±6 V and ±6.5 V in CG and TG, with a write time of 5 ms. After 1,000 erasing/writing cycles at a program voltage of ±6 V with a write time of 5 ms, the V_T of a programmed cell is lowered from 2.92 V to 2.9 V and the V_T of an erased cell is raised from –1.3 V to –0.5 V. It can be also seen that the erased cell flows on-current of more than 100 μA at program voltages of ±6 V and ±6.5 V with a write time of 5 ms.

For the proposed VNN charge pump, the average and three-sigma of VNN voltages are –6.539 V and 0.317 V, respectively, at room temperature. At a hot temperature, they are –6.54 V and 0.272 V, respectively. In the program mode, the VNN results are similar to those in the erase mode. Good results that can be applied to MTP memory IPs are obtained. It is also confirmed by tests over the manufactured 256-bit MTP memory IPs with a 0.18 μm generic CMOS process that the MTP memory IPs are functioning normally with a program voltage of ±6.5 V.

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