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A Ripple Rejection Inherited RPWM for VSI Working with Fluctuating DC Link Voltage

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Abstract – A two stage ac drive configuration consisting of a single-phase line commutated rectifier and a three-phase voltage source inverter (VSI) is very common in low and medium power applications. The deterministic pulse width modulation (PWM) methods like sinusoidal PWM (SPWM) could not be considered as an ideal choice for modern drives since they result mechanical vibration and acoustic noise, and limit the application scope. This is due to the incapability of the deterministic PWM strategies in sprawling the harmonic power. The random PWM (RPWM) approaches could solve this issue by creating continuous harmonic profile instead of discrete clusters of dominant harmonics. Insufficient filtering at dc link results in the amplitude distortion of the input dc voltage to the VSI and has the most significant impact on the spectral errors (difference between theoretical and practical spectra). It is obvious that the sprawling effect of RPWM undoubtedly influenced by input fluctuation and the discrete harmonic clusters may reappear. The influence of dc link fluctuation on harmonics and their spreading effect in the VSI remains invalidated. A case study is done with four different filter capacitor values in this paper and results are compared with the constant dc input operation. This paper also proposes an ingenious RPWM, a ripple dosed sinusoidal reference-random carrier PWM (RDSRRCPWM), which has the innate capacity of suppressing the effect of input fluctuation in the output than the other modern PWM methods. MATLAB based simulation study reveals the fundamental component, total harmonic distortion (THD) and harmonic spread factor (HSF) for various modulation indices. The non-ideal dc link is managed well with the developed RDSRRCPWM applied to the VSI and tested in a proto type VSI using the field programmable gate array (FPGA).

Keywords: Ripple dosed sinusoidal reference random carrier pulse width modulation (RDSRRCPWM), Random pulse width modulation (RPWM), Harmonic spread factor (HSF), Voltage source inverter (VSI).

1. Introduction

The voltage gain, the quality of output and the harmonic profile of the voltage source inverter (VSI) are decreed by the pulse width modulation (PWM) strategy employed [1-4]. This is true when the dc link is ideal, i.e. when the dc link is ripple-free [5]. A host of PWM strategies have been researched with specific targets viz. enhancing the fundamental [6-8], controlling the VSI in pulse dropping region [9, 10], extending the linearity of output voltage with modulation index [11, 12], single mode of control [13], device thermal management [14], reduction of switching losses [15], reduction of distortion [16-18], distribution of harmonic power [19] etc. These PWM strategies perform truthfully when the practical conditions in system are ideal. In many circumferences, the implementation of PWM strategy experiences a noticeable deviation of performance indices from their theoretical values. This mismatch is due to spectral errors which appear in practical cases and they are unavoidable. Such condition prevails in the drive fed from the single-phase ac source, where the front end converter is a single-phase diode rectifier followed by a dc link filter capacitor and a three phase VSI. The spectral errors of the pulse width modulated waveforms are mainly caused by the input amplitude distortion [20]. The amplitude distortion is the fluctuation in the input dc voltage and it has the significant impact on the spectral errors, which has not been focused by many authors. The amplitude distortion will result in decrease of the fundamental magnitude, and boost the unexpected lower order harmonic components and even order harmonic components [21]. In few applications ripple free dc-link may not be recommended due to its demerits viz. bulky, heavy and costly dc-link components, and slow response. The bulky capacitance in the dc link distorts the ac source current and also deteriorates the input power factor. In addition, a huge inrush current flows through a rectifier to the capacitor at turning on

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the drive system. In order to deal with these issues, the additional circuits, such as a power factor correction circuit, an input filter, and a pre-charging circuit, are normally employed. Furthermore, the use of an electrolytic capacitor has a fatal weakness in reliability [22]. The electrolytic capacitor is the most fragile component and hence the lifetime of the system is mainly dependent on that of the electrolytic capacitor.

The dc link voltage fluctuation problem is more serious for an inverter system which utilizes a single phase ac source [23]. The dc-link voltage variation under voltage sag and its dependence on source impedance, dc-link inductance, and output load have been computed [24]. A control strategy based on the concept of average voltage constraint has been suggested for a capacitor-less inverter drive fed by a single-phase ac source [25]. A beat-less control scheme based on the frequency modulation and vector control has been discussed for reducing the beat effect of DC-link voltage fluctuation in the traction drive system without using additional resonant filter at dc-link [25]. Analytical analysis and mathematical closed-form model of three-phase voltage source PWM inverter fed induction motor drive under the dc link ripple voltage component has been presented [26]. A compensation method for fluctuating dc link voltage for railway traction drives has been presented. It employs a repetitive area equalization based algorithm to predict the fluctuating dc link voltage. In steady state, the prediction error are made very small so the pulse widths of the traction inverter can be calculated with precision to avoid beat components in the output [27]. Random pulse width modulation (RPWM) methods address the vibration, acoustic noise, radio interferences etc [19, 28, 29].

The contemporary PWM strategies applied to VSI fed drives are competent in achieving their objectives theoretically [30, 31]. The ripple in the dc-link is the primary contributor for the presence of many harmonic components in the output of the VSI. It is worthwhile to note that these additional components are not present in the switching function. Reduction of acoustic noises and vibration is the basic requirements in many applications, which is being executed by distributing the harmonic power using RPWM methods. The traditional RPWM methods fail when the dc-link capacitor is small or removed. The amplitude distortion not only affects the spreading of harmonics, it also reduces the fundamental component and makes the lower order harmonics to reappear.

This paper proposes an efficient random carrier PWM strategy, which can address above issue effectively. The idea of the proposed ripple dosed sinusoidal reference-random carrier pulse width modulation (RDSRRCPWM) is generating a reference function with dosing of dc-link ripple. Except the reference function, the method remains same as random carrier pulse width modulation (RCPWM) scheme. The modern PWM methods applicable to VSI drive are reviewed in Section II. Section III studies the fluctuation in the dc link voltage and its effect on voltage harmonic spectrum. The principle of proposed RDSRRCPWM is described in section IV. MATLAB based simulation study reveals the fundamental component, total harmonic distortion (THD) and harmonic distortion factor (HSF) for various modulation indices. The modern PWM methods viz. third harmonic injection PWM (THIPWM), triple harmonic injection PWM (TRIPWM), discontinuous PWM (DPWM), space vector PWM (SVPWM) and RCPWM are tested apart from the basic sinusoidal PWM (SPWM). The developed RDSRRCPWM is implemented on a SPARTAN-6 FPGA (XC6SLX45) device for an induction motor drive. The sections V and VI deliver the simulation results and experimental results respectively. The section VII concludes the contribution.

2. Modern PWM Methods

The primary purpose of power electronic converters is to process the power employing static switches to get a desired output from an available input. This modulation of output power is envisaged through control signals that are applied to the switching devices. However, it is seen that the output is contaminated with a wide range of harmonics. The formulation of control strategies will therefore have to be efficient to enable the converters in realizing the dictated performance. The task is demanding because the objectives are two fold; on one hand the converter will have to offer the desired output power and on the other it will have to perform the task with acceptable values of performance indices. The PWM operation synthesizes the output waveform as a composition of pulses of variable width and constant amplitude. The harmonic content of the converter output waveform is usually chosen as the performance criterion and it is desired to minimize it in almost all applications. The triumph of any PWM methods is measured in terms of value of fundamental component of output voltage (V1), THD and the characteristics of the harmonic spectrum. The deteriorate effect on drives such as acoustic noise, electro-magnetic interference (EMI), vibration and harmonic heating depend on the distribution of harmonic power in the spectrum. It is required to have no harmonics of significant magnitude rather than shifting them to higher frequency bands. The THD index does not reflect the spreading effect of the harmonics. Hence a specific index to describe the spreading effect of harmonic power is defined as harmonic spread factor (HSF).

Total Harmonic Distortion: One of the most commonly used terms in harmonic analysis is THD. THD is measure of closeness between the actual waveform with the pure sine wave in shape. For a pure sine wave, the THD value is zero. It is defined as:

$$THD = \sqrt{\sum_{n=2}^{m}\left(\frac{V_n}{V_1}\right)^2} \times 100\% = \frac{\sqrt{\sum_{n=2}^{m} V_n^{\,2}}}{V_1} \times 100\% \quad (1)$$

where, V1 is the rms value of fundamental harmonic voltage. Vn is the rms value of the nth order harmonic voltage.

Harmonic spread factor: HSF is an accurate evaluation index of any waveform for testing its harmonic spreading effects. The HSF quantifies the spread spectra effect of the any PWM scheme. For this purpose, the concept of statistical deviation can be employed and the HSF [19] is defined as follows:

$$HSF = \sqrt{\frac{1}{n}\sum_{k=0}^{n}(H_j - H_0)^2} \quad (2)$$

$$H_0 = \sum_{j>1}^{n}(H_j) \quad (3)$$

where, 'Hj' is the magnitude of jth harmonics, 'H0' is an average value of all 'n' harmonics.

2.1. Sinusoidal pulse width modulation

Generally, two classes of PWM can be identified in implementation aspects: (i) natural-sampled PWM, and (ii) regular-sampled PWM. In a natural-sampled class a low-frequency reference or modulating waveform is compared with a high frequency carrier waveform. These techniques are known as carrier PWM techniques, where the SPWM technique is most common. Natural sampling techniques relay on conventional analogue circuits, where a triangular carrier waveform is compared to a sinusoidal reference waveform. In contrast, the regular sampled PWM techniques for producing switching pattern are based on the optimization of specific performance criteria and implemented using discrete digital hardware. The SPWM technique is commonly used in industrial applications. It is generally accepted that the performance of an inverter with any switching strategy can be related to the harmonic content of its output voltage. With SPWM, however, the relative amplitudes of the harmonics change with the modulation index, Ma. The SPWM technique, however, exhibits poor performance with regard to maximum attainable voltage and power. For instance, in a three-phase SPWM-VSI, the ratio of the maximum attainable (in linear range) fundamental component of the line-to-line voltage to the dc supply voltage is 0.866% and this value indicates poor exploitation of the dc supply.

2.2 Third harmonic injection pulse width modulation

Harmonic injection is adding higher frequency sine wave with the reference (fundamental frequency) sine

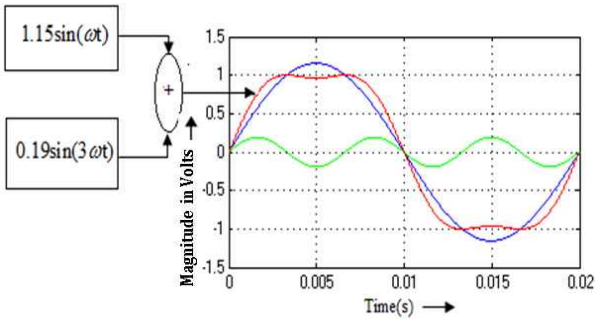

Fig. 1. Reference function in THIPWM

wave. Fundamental output voltage is greatly decided by the width of the pulses in the middle region of the PWM patterns. The number of pulses are described by frequency of the carrier and widths of the pulses are decided by the reference magnitude, which are accurately known through the mathematical relations. It is readily understood that making the reference sine flat by injecting higher order harmonics (3, 9, 15…) with the basic reference, the width (hence the area) of the center pulses can be increased. The establishment of reference function in third harmonic injection PWM (THIPWM) is shown in Fig. 1.

It is a modification over the SPWM technique wherein a suitable amount of third harmonic signal is added to the sinusoidal modulating signal of fundamental frequency, which provides higher fundamental voltage with low harmonic distortion [32]. This harmonic injected reference causes 15.5% increase in the amplitude of the fundamental voltage compared to the basic SPWM. The reference function of the THIPWM is described as follows.

$$y = 1.15 \sin \omega t + 0.19 \sin \omega t \quad (4)$$

2.3 Triplen harmonic injection pulse width modulation

The triplen harmonic injection pulse width modulation (TRIPWM) is a variation of the THIPWM. In TRIPWM, the modulation signal is obtained by adding the harmonic components of integer multiples of 3 to the sine wave [32]. It provides higher fundamental voltage with low harmonic distortion. The resulting flat-topped reference waveform (Fig. 2) helps in obtaining the output voltage values of over modulation region (assuming SPWM) in under modulation

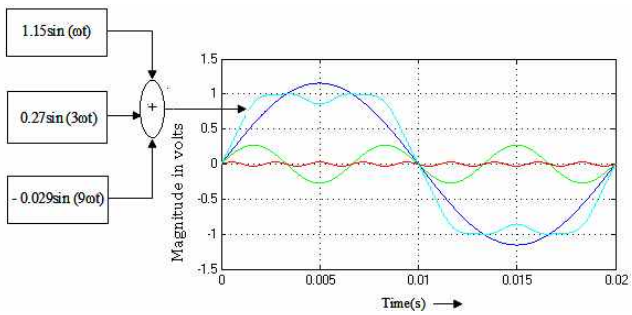

Fig. 2. Reference waveform of TRIPWM

itself. The analytical expression for the reference waveform can be derived from the addition of other triplen harmonics as given as follows.

$$y = 1.15 \sin \omega t + 0.27 \sin \omega t - 0.29 \sin \omega t \quad (5)$$

2.4 Discontinuous PWM

In the discontinuous PWM (DPWM) methods a discontinuous (piece wise continuous) reference function is compared with the triangular carrier. There are about six variations reported in the literature under the name DPWM viz., DPWM0, DPMW1, DPWM2, DPWM3, DPWMMAX and DPWMMIN [33, 34]. The basic idea behind all these variations are employing discontinuous modulating signal instead of basic sinusoidal signal while carrier remains the triangular function. DPWM modulation techniques have the advantage of eliminating one switching transition in each half carrier interval, which allows the switching frequency to increase by a nominal value of 3/2 accordingly for the same inverter losses. This may improve the harmonic performance of the inverter by virtue of the reduced influence of higher frequency switching harmonics. In DPWM, switching losses can be drastically reduced, the waveform quality may be improved, the linear modulation range can be extended, and common mode voltage of motor drives can also be drastically diminished. Table 1 details the expressions for the modulation waves of DPWM1 for one complete cycle. The variation of modulation index, M does not have any effect in the saturation region of the modulating wave. The reference waveform of DPWM1 for phase A is shown in Fig. 3.

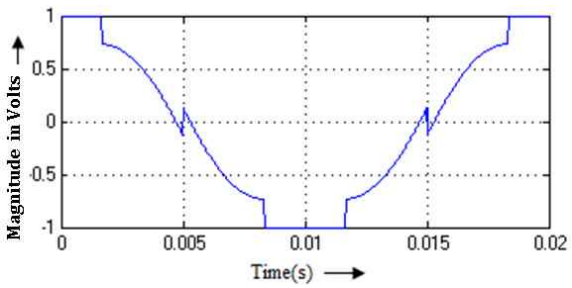

Fig. 3. Reference waveform of DPWM1 for phase A.

2.5 Space vector pulse width modulation

The space vector pulse width modulation (SVPWM) technique was proposed by Pfaff, Weschta and Wick in 1982. This method is an advanced; computation intensive PWM method and possibly the best techniques for variable frequency drive application etc. It is a more efficient technique for generating reduced distortion ac voltage with lower THD. The basic idea of SVPWM is to equalize the volt-seconds (area) between the targeted/required output and the real output sample to sample basis using discrete switching states and their on-times [35, 36].

Fig. 4 shows the Space Vector Diagram (SVD) of a VSI. The possible switching combinations of the VSI form eight distinct states and results in respective vectors (output voltages) namely, V1 to V6 (active vector) and V0 and V7 (null vector). Joining of the tip of all the active vectors forms a hexagon, which consists of six sectors. Every sector is an equilateral triangle of unity side and h (= √3/2) is the height of a sector. On-time calculation for any of the

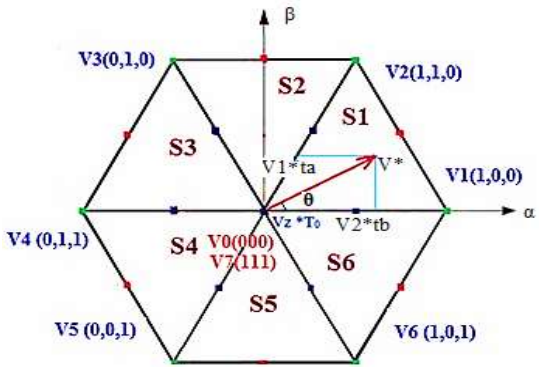

Fig. 4. SVD for VSI

Table 1. Composite modulating function for DPWM1

Technique	DPWM1		
Alpha (degree)	Phase A	Phase B	Phase C
$0\text{-}30^0$	+1	$+1-\sqrt{3}*M*\cos(\theta+\frac{\pi}{6})$	$+1+\sqrt{3}*M*\cos(\theta+\frac{5\pi}{6})$
$30^0\text{-}0^0$	$-1-\sqrt{3}*M*\cos(\theta+\frac{5\pi}{6})$	$-1+\sqrt{3}*M*\sin(\theta)$	-1
$90^0\text{-}150^0$	$+1+\sqrt{3}*M*\cos(\theta+\frac{\pi}{6})$	+1	$+1-\sqrt{3}*M*\sin(\theta)$
$150^0\text{-}210^0$	-1	$-1-\sqrt{3}*M*\cos(\theta+\frac{\pi}{6})$	$-1+\sqrt{3}*M*\cos(\theta+\frac{5\pi}{6})$
$210^0\text{-}270^0$	$+1-\sqrt{3}*M*\cos(\theta+\frac{5\pi}{6})$	$+1+\sqrt{3}*M*\sin(\theta)$	+1
$270^0\text{-}330^0$	$-1+\sqrt{3}*M*\cos(\theta+\frac{\pi}{6})$	-1	$-1-\sqrt{3}*M*\sin(\theta)$
$330^0\text{-}360^0$	+1	$+1-\sqrt{3}*M*\cos(\theta+\frac{\pi}{6})$	$+1+\sqrt{3}*M*\cos(\theta+\frac{5\pi}{6})$

six sectors (Si) (where i = 1, 2, 3, 4, 5, 6) is same therefore, the operation in sector-1 may be considered to understand the SVD based pulse calculation.

The reference voltage V* is the rotating SVD form of three-phase voltage. The projection of V* in the α-β plane at any period will lie in the area of any one of the sector. The constitution of the reference can be done through two edge vectors of the sector with position dependent time values in a fixed sampling interval. The time integral value of V* can be approximated by the sum of the products of two of the vectors and their time widths. For example, in Fig. 4 the reference V* lie in sector-1, which is edged by vectors V1 and V2. Starting from time t0, V* moves to t1 and the relation for the time integral can be written as

$$\int_{t_0}^{t_1} V^* = T_a V_1 + T_b V_2 \tag{6}$$

where, Ta and Tb represent the time widths for vectors V1 and V2 respectively. The integration time interval t0 to t1 are the beginning and the end of the sampling period, Ts (much less than the period corresponding to one sector). By adjusting the values of Ta and Tb, the right-hand side of this expression can be made as close as possible to left-hand side value (but still they can never be completely equivalent to each other). Thus, by keeping the inverter-switching states to constitute V1 for a time period Ta and V2 for a time period Tb, the pulse pattern during the period t0 to t1 is obtained. The same approximation (of V1 and V2) is repeated for all samplings of this sector. In the same sector while the reference V* moves such that the angle θ increases then the corresponding time periods Ta and Tb will be calculated again instant by instant. It is worthwhile to note that when V* approaches V2, the period Tb will be more than Ta. Similarly when V* enters into next sector (sector edged by V2 and V3) the time integral value of V* can be approximated by the sum of the products of V2 and V3 states and their time widths. The same procedure will have to be repeated for all other sectors.

$$V^*T_s = V_1T_a + V_2T_b \tag{7}$$

2.6 RCPWM

Fig. 5 shows the randomized triangular carrier based random carrier pulse width modulation (RCPWM). This is one of the well-established RPWM, which is considered for comparison purpose in this study.

As shown in Fig. 5, the triangular carrier with fixed frequency 'fc+' and the triangular carriers with fixed frequency but opposite phase 'fc-' are given as input to the 2×1 multiplexer. The randomized triangular carrier 'R' can be obtained randomly selecting the fc+ and fc- by the pseudo random binary sequence (PRBS) output bits 0 or 1

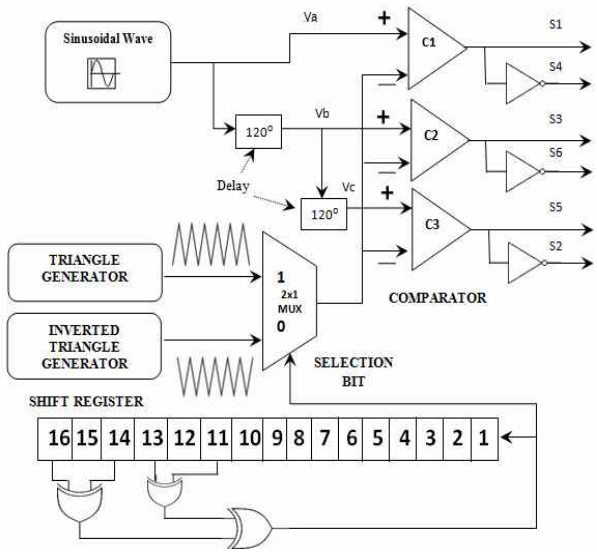

Fig. 5. Random carrier PWM

of the random bit generator.

In order to obtain the random bit number for selecting the winning triangle, a sequential digital circuit with large number of distinct states (higher random repetition cycle) is required. Since the randomness does not rely only on two distinct carriers but also on the sequential pattern used for selection. A linear feedback shift register (LFSR) is the best solution to offer the above requirement (best randomness) [19]. The principle of LFSR is based on the logical operation of several bits of a digital number and is commonly known as pseudo PWM code generator in communication systems. A LFSR is a shift register whose input bit is a linear function of its previous state. The LFSR looks much like a normal register, except that certain bits are the function of other bits in the previous state. With an initial value (seed), the stream of values produced by the register is completely determined by its current (or previous) state in a deterministic manner. Even though, there is register it has higher possibility of entering into a repeating cycle (it has a finite number of possible states), careful design of feedback function can produce a sequence of bits which appears random and which has a very long cycle. Typical applications of LFSR are pattern generators, counters, built-in self-test (BIST), encryption, compression, checksums, pseudo-random bit sequences (PRBS) etc. The triumph in producing randomness depends on number of bits in shift register, feedback function, output stream and tap sequences. For feedback functionality, XOR gate is used. The choice of taps determines how many distinct states are there in a given sequence before the sequence repeats.

In this paper, 16 bits LFSR with a feedback of four tapings are used and the feedback causes the register to loop through repetitive sequences of pseudo-random value. The winning triangle carrier cycle is compared with sinusoidal reference to get the gating pulses.

3. VSI with Fluctuating DC Input and Motivation

The single-phase input is rectified by the rectifier and the fluctuating dc is delivered in the typical ac drive shown in Fig. 6. The ripple present in the dc link is removed by effectiveness of filtering relays on the value of the capacitor used and the contrary objection is system cost and size. The control of VSI is basically in 180 degree conduction mode and SPWM is being the obvious choice in many applications. Even though the performance of SPWM in terms THD, linearity in control etc. are well proved and appreciated, its spectral spreading effect is poor. This causes objectionable torque ripple, vibration and acoustic noise, and problematic in drives application. SPWM by its nature creates harmonics as cluster at switching frequency and its multiples. These carrier frequency harmonics are of dominant in magnitude and create mechanical vibration in the drive [37]. A host of PWM methods, named, RPWM have been researched and proved for distribution of harmonic power. The basic idea in any RPWM is rather than having few harmonics of dominant magnitude, having many harmonics none is

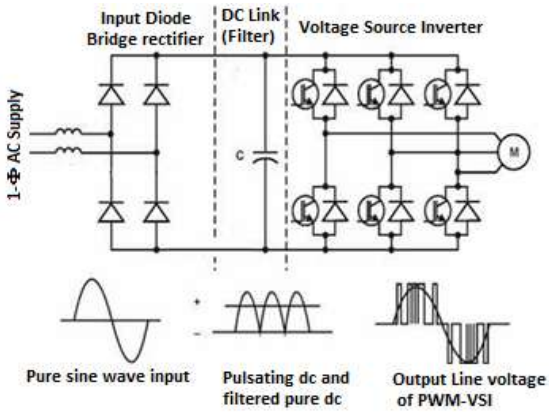

Fig. 6. Typical configuration of VSI drive with front end diode rectifier

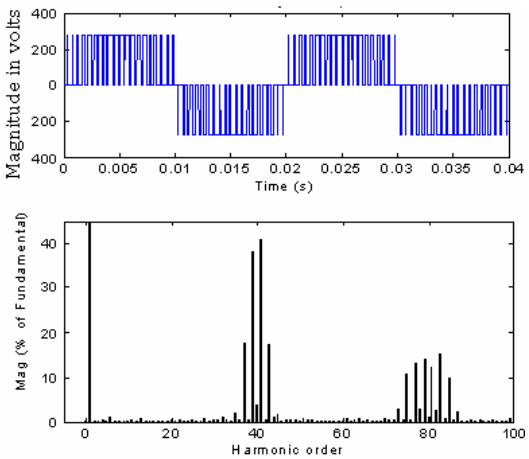

Fig. 7. Inverter output voltage and harmonic spectrum with Constant DC-SPWM

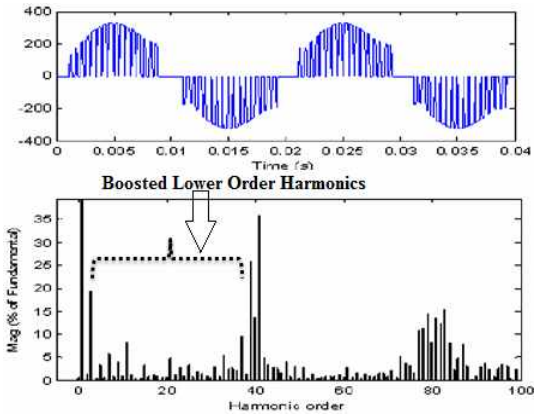

Fig. 8. Inverter output voltage and harmonic spectrum with fluctuating DC-SPWM

with objectionable magnitude. It is worth, noting that the modern PWM methods namely THIPWM, TRIPWM, DPWM and SVPWM methods are triumph in enhancing the fundamental, reducing THD etc, but they are not intended to improve the harmonic spreading effect.

When the VSI is connected to the rectifier, the filtered output is superimposed with the distortions due to insufficient filtering (lesser filtering capacitance value). These amplitude distortions cause deteriorating effects in the performance of VSI. This distorted input causes appearance of the lower order harmonics, decrease the fundamental and increases the THD. For a typical case the output voltage waveforms and the frequency spectra for VSI working with constant as well as distorted dc inputs are represented in Fig. 7 and Fig. 8 with SPWM. From the figures it is understood that lower order and even harmonic components are resulted with the distorted dc input which are completely absent in constant dc input operation. The boosted lower order harmonics are highlighted in the figure. The similar conclusions can only be arrived even with other modern (THIPWM, TRIPWM, DPWM and SVPWM) PWM methods.

Similarly the performance deteriorations of existing RPWM methods have also not been analysed for inverters working with fluctuating dc inputs. There is no specific RPWM is available for rejecting the dc link distortions in harmonic spreading. The previous PWM submissions on fluctuating dc inputs have concentrated only in improving the fundamental and reducing the THD. They never considered the spreading effects of harmonic power. There must be innovative RPWM scheme, which must inherently eliminate the influence of dc link distortions in harmonic spreading effects.

4. Proposed RDSRRCPWM

The proposed ripple dosed sinusoidal reference-random carrier pulse width modulation is represented in Fig. 9. The basic principle of the method is adding the randomness

in triangular carrier and dosing the ripple rejection characteristics in the reference. The actual dc link voltage (Vdc, actual) with insufficient filtering is derived, and the ratio between Vdc, actual and theoretical dc output voltage (Vdc, theoretical) is obtained. This ratio is a ripple function and this function is used to reject the effect of amplitude distortion. This ripple function is dosed with the sinusoidal reference by multiplication. It results in the reference for phase A, and the references for phase B and C are obtained by phase delaying. The new modified sinusoidal reference function is derived as follows.

$$V_{ref,\,\mathrm{mod}} = \frac{V_{dc,theoretical}}{V_{dc,actual}} * V_{ref} \tag{8}$$

A typical triangular carrier and its inverted form are considered. From these two carriers, one is selected by a random bit for every carrier cycle (cycle to cycle basis).

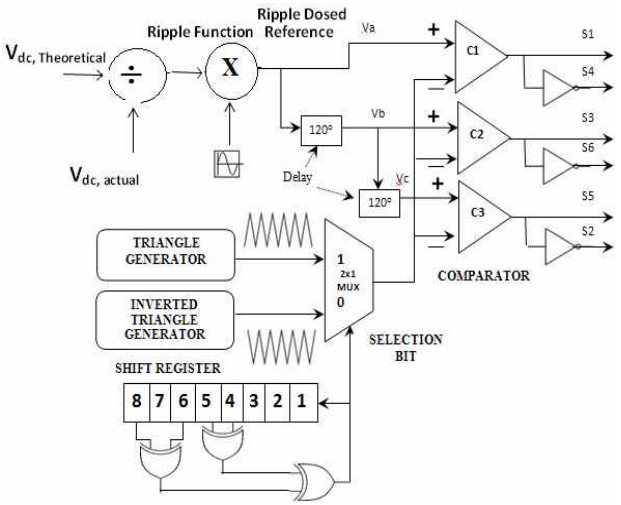

Fig. 9. Proposed RDSRRCPWM

Similar to the case in RCPWM, the random bit is obtained through a LFSR. The continuous output of feedback function is referred as output stream (selection bit). After having chosen the carrier signal, the conventional way of generating gating signal is followed with the reference synthesized in Eq. (8).

5. Simulation Study

The simulation study is performed in MATLAB / Simulink software. A three-phase VSI inverter with a three-phase squirrel cage induction motor load (0.75kW) and ODE Solver ode23tb are considered. For the input ac voltage of 230V (rms) and the output frequency of 50Hz, the study considers capacitance values of 33µF, 330µF and 2400µF.

The switching frequency for SPWM, THIPWM, TRIPWM, DPWM and SVPWM is 3kHz while the RCPWM and RDSRRCPWM employ the 3kHz and its inverted form. This section explores the results such as THD, HSF and fundamental component along with the waveforms and the harmonic spectra.

The results are absorbed for entire range of modulation index (Ma). Fig.10 shows the PWM-VSI drive schematized in MATLAB-Simulink. The simulation is performed for SPWM, THIPWM, TRIPWM, DPWM, SVPWM, RCPWM and RDSRRCPWM methods. The Table 2 demonstrates the effectiveness of the RCPWM over SPWM when used in VSI fed from constant dc. The RCPWM offers reduced HSF and THD, and improved fundamental component. For the modulation index (Ma) value of 0.8, the RCPWM results in 37% reduction of HSF and 35% improvement in fundamental component. When similar study is done with SPWM and RCPWM for the fluctuating dc input with C=22µF, the results are completely deteriorated as confirmed by the Table 3. The performances of the modern

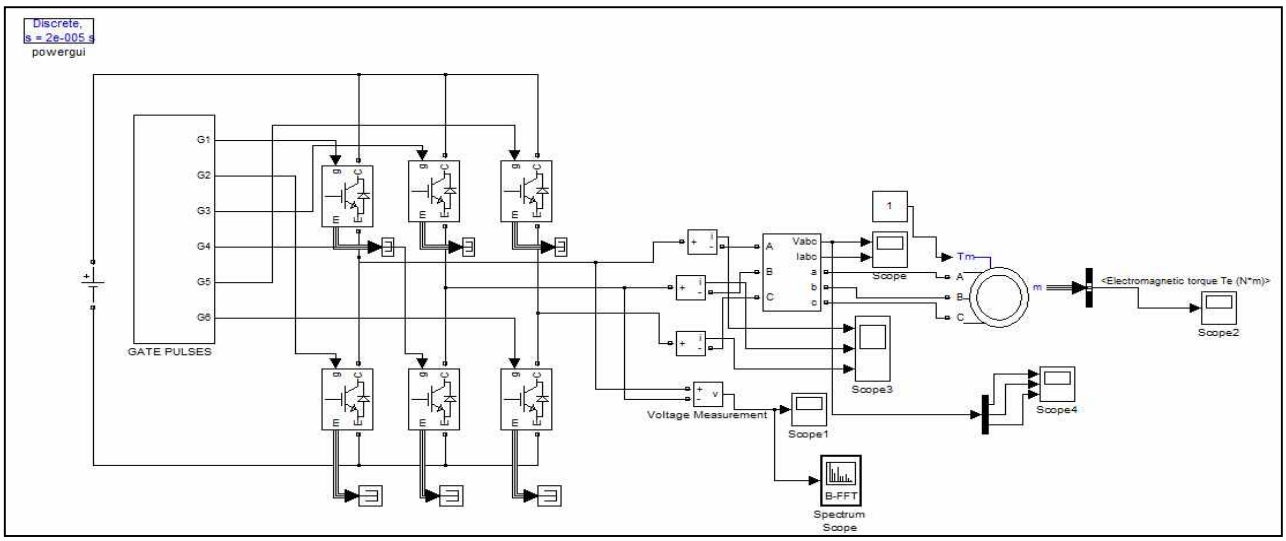

Fig. 10. MATLAB-Simulink Model for PWM-VSI drive

Table 2. Performance of SPWM and RCPWM- constant dc

M_a	V_1 (V)		THD (%)		HSF	
	SPWM	RCPWM	SPWM	RCPWM	SPWM	RCPWM
0.2	72.72	75.31	248.28	240.71	6.475	4.9308
0.4	136.8	144.80	168.07	163.11	6.142	4.6710
0.6	211.1	216.40	122.01	119.76	5.880	4.6054
0.8	289.9	293.80	90.29	89.15	5.566	4.0572
1.0	361.9	367.30	67.60	66.13	4.952	3.7386
1.2	395.2	397.00	58.21	57.55	4.248	3.5091

Table 3. Performance of SPWM and RCPWM with fluctuating dc input, C=22µF

M_a	V_1 (V)		THD (%)		HSF	
	SPWM	RCPWM	SPWM	RCPWM	SPWM	RCPWM
0.2	61.33	69.12	257.28	249.77	11.213	9.990
0.4	130.2	139.80	177.72	169.91	10.940	9.301
0.6	207.0	212.31	133.9	126.73	10.081	9.027
0.8	285.5	290.71	101.52	93.88	9.819	8.698
1.0	357.9	365.30	78.76	70.04	9.001	7.510
1.2	392.1	395.01	66.29	59.15	8.918	6.790

Table 4. Performance of THIPWM, C=22µF

M_a	V_1(V)	THD (%)	HSF
0.2	71.63	252.33	16.89
0.4	150.6	170.61	15.98
0.6	237.1	126.41	14.19
0.8	327.75	97.14	13.95
1.0	411.6	65.18	12.99
1.2	450.9	54.11	10.01

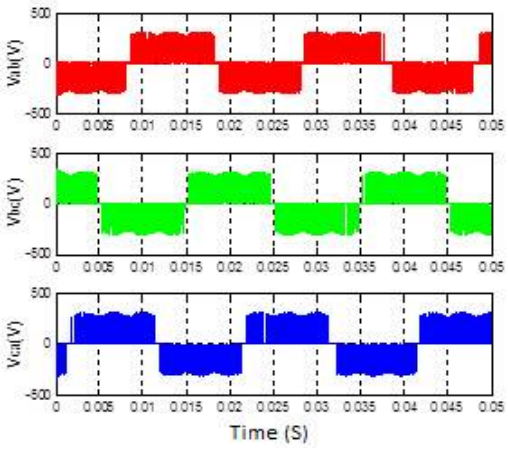

Fig. 11. Simulated line-line voltage waveform for Ma=0.8-RDSRRCPWM

PWM methods are tested for dc-link fluctuation before analyzing the proposed RDSRRCPWM. Fig. 11 and Fig. 12 depict the line voltages and line currents respectively for a representative case (RDSRRCPWM) when input voltage is fluctuating (C=22µF).

The performances of DPWM and SVPWM are presented in Tables 5 and 6 respectively. The fundamental (V1) and THD performances of modern PWM methods are well known. The simulation results confirm it. The harmonic

Table 5. Performance of DPWM

M_a	V_{o1}(V)	THD (%)	HSF
0.2	63.12	261.66	15.81
0.4	140.01	180.21	14.21
0.6	230.19	139.66	13.92
0.8	321.05	103.22	13.05
1.0	407.33	75.08	11.91
1.2	447.9	60.61	9.70

Table 6. Performance of SVPWM

M_a	V_o (V)	THD (%)	HSF
0.4	67.22	161.31	10.10
0.6	142.41	120.81	9.98
0.8	230.81	86.55	9.31
0.9	322.05	71.41	9.08
1.0	406.31	55.51	8.58
1.2	447.21	49.61	7.02

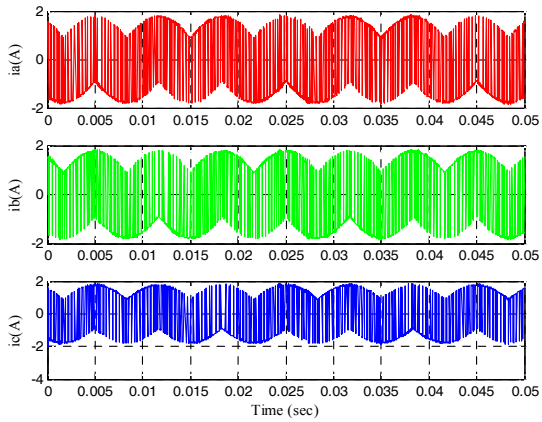

Fig. 12. Simulated line current waveform for Ma=0.8-RDSRRCPWM

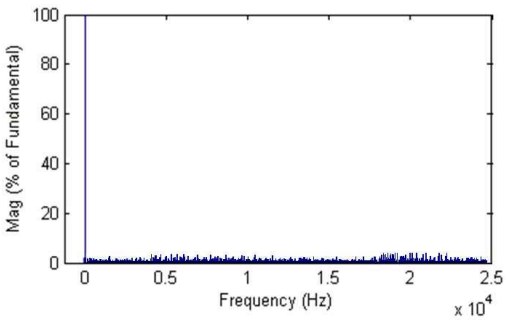

Fig. 13. Harmonic spectrum of output voltage – RDSRRCPWM

spreading effects of them are not validated earlier. The HSF results are interesting and based on the HSF merit these methods can be arranged in their ascending order THIPWM, TRIPWM, DPWM, SPWM, SVPWM and RCPWM. The results prove the failure of RCPWM (developed for constant dc) operating when fluctuating input. With fluctuating dc input (C=22µF), the fundamental value is reduced, and the THD and HSF values are raised. At Ma=0.8, there is about 53% increase in the HSF value is

Table 7. Performance of RDSRRCPWM-fluctuating dc with different capacitors

M_a	V_1 (V)			THD (%)			HSF		
	22µF	330µF	2200µF	22µF	330µF	2200µF	22µF	330µF	2200µF
0.2	74.57	76.53	79.12	240.64	239.36	228.88	8.515	8.087	5.917
0.4	143.7	147.6	151.8	164.59	154.34	132.65	8.278	7.459	5.260
0.6	217.8	221.4	226.1	120.54	116.02	92.16	8.012	7.100	4.515
0.8	294.5	297.1	305.8	90.38	84.89	67.91	7.530	6.407	5.233
1.0	370.2	378.3	381.2	67.84	63.55	51.23	7.034	5.947	4.927
1.2	399.5	401.8	405.4	57.81	52.62	42.56	6.452	5.054	4.661

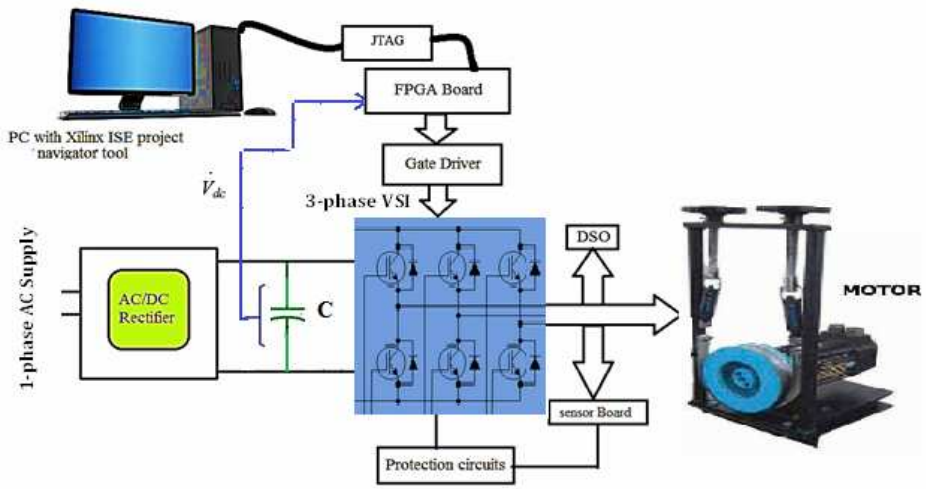

Fig. 14. Over view of the proposed system

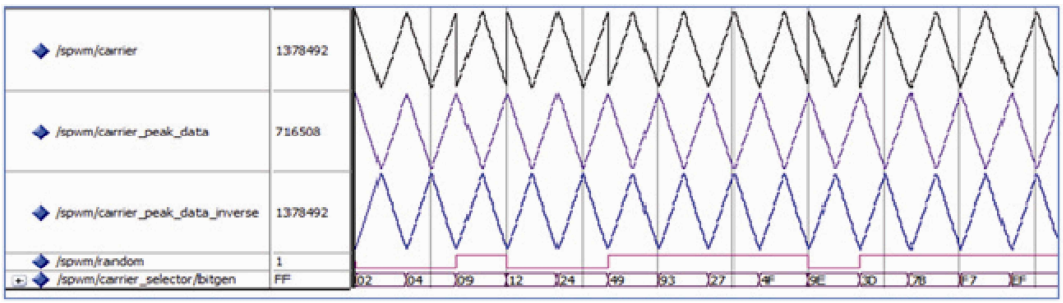

Fig. 15. Random bit generation and triangle selection based on PRBS select bit

evidenced.

The results of RDSRRCPWM with fluctuating dc for different capacitor values (C=22µF, 330µF and 2200µF) are listed in Table 7. The performance enhancement of the drive with fluctuating dc link with RDSRRCPWM is readily understood. The representative harmonic spectrum for RDSRRCPWM is presented in Fig. 13.

6. Hardware Implementation

The Fig. 14 shows the experimental system suggested to implement the proposed RDSRRCPWM. It consists of a diode rectifier, a dc link capacitor, a three-phase VSI (1200 V, 25A and 20 kHz Mitsubishi intelligent power module), a personal computer, SPARTAN-6 FPGA (XC6SLX45) device and a motor load. The proposed RDSRRCPWM architecture is designed using the VHDL language. The functional simulation of the architecture has been carried out using the tool Modelsim 6.3. The Register Transfer Level (RTL) level verification and implementation are done using the synthesize tool Xilinx ISE 13.2. Then the

Table 8. Comparison of simulation and experimental results-RDSRRCPWM for C=22µF

M_a	THD		HSF	
	Sim	Exp	Sim	Exp
0.2	240.64	241.61	8.515	8.551
0.4	164.59	165.05	8.278	8.311
0.6	120.54	122.32	8.012	8.051
0.8	90.38	93.41	7.530	7.555
1.0	67.84	69.21	7.034	7.167
1.2	57.81	59.13	6.452	6.501

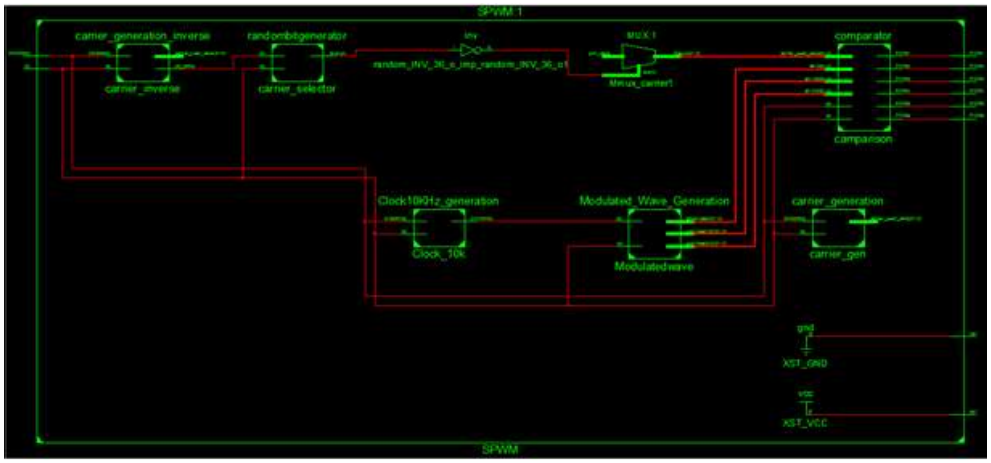

Fig. 16. RTL Schematic View of the RDSRRCPWM design

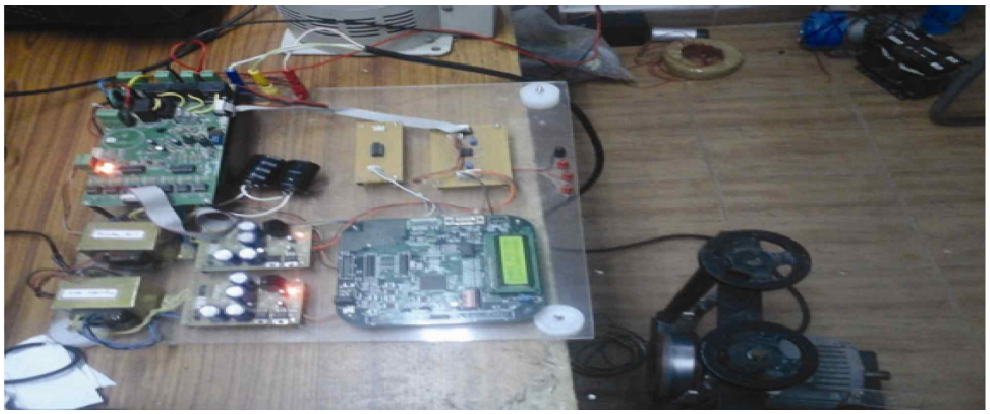

Fig. 17. Experimental setup

Fig. 18. Fluctuating DC link voltage (C=22μF)

designed architecture is configured to the SPARTAN-6 FPGA (XC6SLX45) device. The functionality of each block in the architecture is simulated thoroughly using the Modelsim software. The corresponding simulation outputs are shown in Fig. 15 and Fig. 16.

Fig. 17 shows the photograph of the developed hardware setup. Fig. 18 evidences the fluctuation caused by the lower valued dc link capacitors. Fig. 19 illustrates the output line voltages and currents for RDSRRCPWM with fluctuating dc link voltage (C=22μF). The spectra from Fig. 20 to Fig. 25 corroborate the merits order offered by the simulation results for the dc capacitor value 22μF. The comparison between the simulation and hardware results are done in Table 8. It is found that the experimental results match the simulation counterpart very closely.

7. Conclusion

The harmonic spreading effects of VSI feeding induction

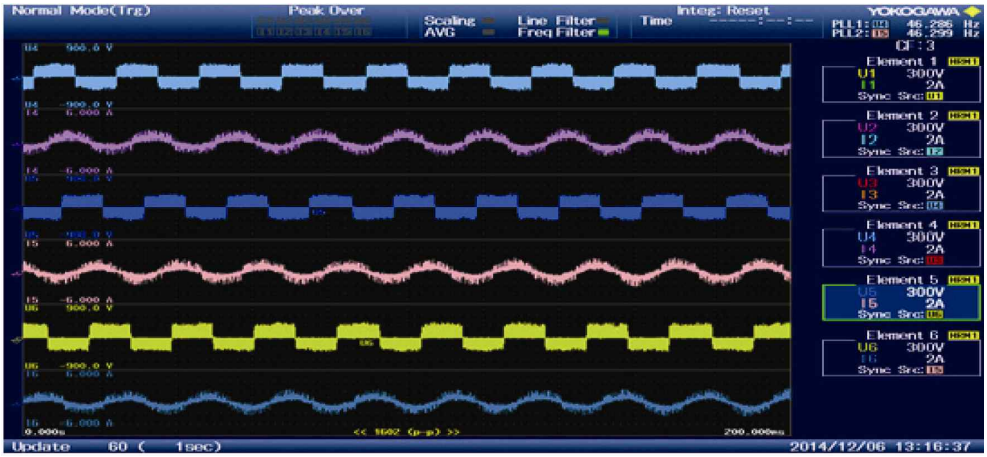

Fig. 19. Three-phase output line voltages and currents-RDSRRCPWM

Fig. 20. Harmonic spectrum of THIPWM- fluctuating dc input (C=22µF)

Fig. 21. Harmonic spectrum of DPWM- fluctuating dc input (C=22µF)

motor is studied for both constant and fluctuating dc input. The modern PWM methods developed with the objectives fundamental enhancement, THD reductions etc. perform poorly in harmonic spreading. The tabulated results such as fundamental magnitude, THD and HSF are more informative. The results insist that the available random PWM methods must be modified with inherent property of rejecting the dc input ripple. When a VSI is fed with the fluctuating dc link voltage, it generates additional harmonics that results from the modulation between the inverter switching function and dc link ripple. Low frequency harmonic currents have many antagonistic effects. The most serious is torque pulsation which causes speed jitter and severe mechanical vibrations. For a large

drive, the acoustic noise generated from low frequency torque pulsation can be quite unbearable. This may result in reduction of efficiency and shortening of motor life. The dc link voltage fluctuation problem is more serious for an inverter system which utilizes a single phase ac source. With the proposed RDSRRCPWM technique highly sprawled harmonic spectrum is guaranteed at the VSI output even with a substantial low frequency voltage ripple in the dc-link.

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