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Peak-Valley Current Mode Controlled H-Bridge Inverter with Digital Slope Compensation for Cycle-by-Cycle Current Regulation

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Abstract – In this paper, digital peak current mode control for single phase H-bridge inverters is developed and implemented. The digital peak current mode control is achieved by directly controlling the PWM signals by cycle-by-cycle current limitation. Unlike the DC-DC converter where the output voltage always remains in the positive region, the output of DC-AC inverter flips from positive to negative region continuously. Therefore, when the inverter operates in negative region, the control should be changed to valley current mode control. Thus, a novel control logic circuit is required for the function and need to be analyzed for the hardware to track the sinusoidal reference in both regions. The problem of sub-harmonic instability which is inherent with peak current mode control is also addressed, and then proposes the digital slope compensation in constant-sloped external ramp to suppress the oscillation. For unipolar PWM switching method, an adaptive slope compensation in digital manner is also proposed. In this paper, the operating principles and design guidelines of the proposed scheme are presented, along with the performance analysis and numerical simulation. Also, a 200W inverter hardware prototype has been implemented for experimental verification of the proposed controller scheme.

Keywords: H-bridge inverter, Peak current mode control, Cycle-by-cycle current limitation, Digital slope compensation.

Nomenclature

V_{in}	Input DC voltage
V_{out}	Output AC voltage
L	Output filter inductor
C	Output filter capacitor
R	Load resistor
R_i	Current- sensing gain
s_n	Inductor current slope during ON- time
s_f	Inductor current slope during OFF- time
s_e	External ramp slope
I_L	Inductor current
I_{ref}	Reference current
T_S	Switching period
D	Duty ratio
D'	Complement of duty ratio 1-D
$\Delta I_{0,1,2}$	Inductor current perturbation (initial or 1st or 2nd)
F_m	Duty ratio modulator gain
k_f'	Feed-forward gain from on-time voltage to control
k_r'	Feed-forward gain from off-time voltage to control
k_r	Feed-forward gain from output voltage to control
H_e	Equivalent sampling-gain in current feedback
TBCTR	Time-Base Counter
TBPRD	Time-Base Period
ISR	Interrupt Service Routine

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1. Introduction

As the demand for small-scale renewable energy systems is rapidly growing, the need for well regulated power electronic controllers also increases [1]. The inverter is an essential component in the system which produces sinusoidal waveforms to supply the ac load or to connect to the grid. The dc/ac single phase inverters are used to interface the power sources with the single-phase grid. The single-phase H-bridge inverter is a simple circuit topology with a small number of components. The inverter is a bi-directional device capable of handling both real and reactive power. Control of the inverter is achieved by varying the turn on time of the upper and lower power switches of each inverter leg. Careful measurements have to be taken not to turn on both the switches in one leg at the same time, to avoid short circuit of the DC supply. The gate driver output should also contain enough dead time to prevent overlapping of conduction periods in each leg.

Current mode control methods have several advantages over voltage mode control methods, such as faster control dynamics, better audio-susceptibility, simple compensation and overcurrent protection [2-3]. In case of small-scale inverters, PI controller is one of the most preferred forms of inverter controllers due to its simplicity and well defined design procedures. However, this kind of controller has relatively poor performance due to the steady-state error with tracking the sinusoidal reference. Furthermore, this controller is unable to reject the noise in the current signal

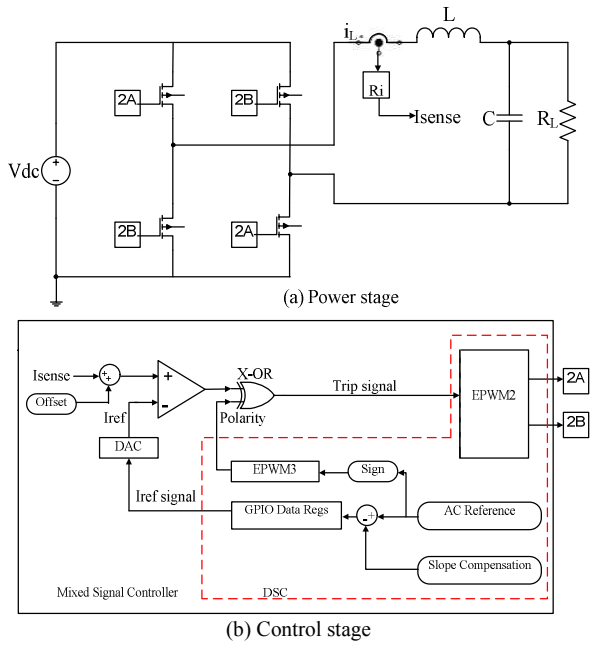


Fig. 1. Peak-valley current mode control circuit of single-phase H-bridge inverter with digital slope compensation.

due to its poor dynamics. Hysteretic controllers have very fast and stable dynamics, however there would be a high bandwidth of the harmonic spectrum. This makes designing and implementation of the filters a tedious process. Whereas, in peak current mode control, the duty cycle is controlled by comparing the instantaneous peak of the inductor current to the sinusoidal reference in a cycle-by-cycle basis. Hence, implementing peak current controller is the better option based on control perspective. However, peak current mode controllers have an inherent problem of the presence of sub-harmonic oscillations [4-5]. This problem can be solved by the addition of slope compensation.

So far, most of the implementations of peak current control for DC-AC inverters have been exclusively analog in nature. Previous analog implementation has been used for buck converter topology with an unfolding circuit for photovoltaic-sourced stand-alone applications [6]. Analog implementation lacks flexibility and durability which can be offered in digital implementation. With radical improvements in the processing speed and cost reduction of digital signal controllers (DSC), digital implementation of control circuits becomes a more practically-viable option [7-11]. For grid-connected single-stage PV inverters, predictive methods of the peak current control have been digitally implemented in a simple manner [12]. In the predictive method using one or two samples during each switching cycle, the duty cycle is predicted using the mathematical models of the inverter for unipolar switching. Therefore, a variant of the peak current control with predictive slope compensation is achieved by this method. Systems with predictive methods lack real time cycle-by-cycle current limitation and also have computational delays which results in degraded audio-susceptibility [13].

To achieve the dynamics of cycle-by-cycle current limiting for single-phase H-bridge inverter with a digital compensation and peak-valley mode change is the objective of this paper. Using a DSC with very high bandwidth analog-to-digital converter (ADC) for high frequency sampling of inductor current is not an efficient method of control. Furthermore, it becomes impossible to achieve this for high frequency applications. A solution using a mixed-signal implementation for DC-DC converters has been discussed in [14]. However, for DC - AC applications, the inverter requires a peak-to-valley control-mode transition in every swing cycle. This paper proposes the implementation strategy for DC-AC single phase inverters, employing significant improvements by an efficiently-organizing method. The chosen DSC for this work is TMS320F28335 from Texas Instruments. The device is available to control multiple high-frequency power stages for power electronics industrial applications [15-18].

Section II discusses the operating principles of the newly developed digital peak-valley current mode controller in detail. Section III explains how to analyze and design the digital slope compensation required in order to nullify the oscillations of the peak current mode controller. Section IV describes an adaptive slope compensation for a unipolar switching method of H-bridge inverter. Section V explains the hardware verification followed by conclusion in Section VI.

2. Operating Principle

2.1 Circuit configuration

The main purpose of the peak current controller is to limit the instantaneous peak of the inductor current according to the given reference in cycle-by-cycle basis. Fig. 1 depicts the proposed circuit which includes the power stage and control logic circuit for implementing peak-valley current-mode control of single-phase H-bridge inverter with bipolar switching. In a typical analog controller the inductor current is sensed by a current sensor with gain (R_i) in Fig. 1(a). In conventional analog controllers, the peak (valley) value of the sensed current signal is detected with respect to the reference signal using a comparator, and then accordingly the duty cycle is changed with the help of the S-R flip flop. The current loop becomes an inner loop when multiple feedback control loops are used. Then a compensator present only in the voltage loop known as the outer loop. In order to effectively implement this in the digital mode, the comparator which detects the peak of the sensed current is kept outside the DSC. This is a more efficient method which saves the computing power necessary for the implementation of outer loop and also to

control other plants in a multi-plant system if necessary. The EPWM2 module in the DSC which provides the PWM signals to the inverter switches is programmed to operate in a cycle-by-cycle basis and changes the duty-cycles based on the trip signal when it goes low.

The distinct challenge for implementing peak current mode control in DC-AC inverters is the AC movement of output waveforms in both of the positive and the negative regions. The controller should be able to track the reference perfectly in both regions. To achieve the AC control in positive and negative regions, a novel control circuit has been proposed in this paper. In Fig. 1, the sensing signal (I_{sense}) with offset is compared with the AC reference (I_{ref}) coming from the DSC. The reference is generated by combining the sine reference with slope compensation. The DSC provides the reference in a form of 150 kHz PWM signal (see Fig. 1(b)).

The reference signal from the DSC must be converted into an analog signal before connecting it to the comparator. This is achieved by an external 12-bit DAC IC chip. The reference signal in the DSC is scaled in a way that the slope compensation ramp at the input of the comparator is active. The reference PWM produced by the DSC ranges from 0 to 3.3V. Therefore, an offset voltage which exactly matches the offset present in the reference is added to the sensed current before comparing it to reference. In addition to the comparator, which serves to detect the peak of the inductor current an X-OR gate is inserted between the lines. The purpose of adding XOR logic is to ensure the peak current mode operation during the positive region and the valley current mode operation during the negative region by the trip signal. If peak current mode operation is implemented during both the positive and the negative regions, it will result in an undesirable DC offset in the inductor current. A PWM signal based on the polarity of the reference waveform ('polarity' in Fig. 1) is connected to the other input of X-OR gate, which helps to detect the valley point during the negative region. Cycle-by-cycle trip action is enabled for the EPWM2 module. Unlike dc/dc converter, the output of the H-bridge inverter swings from positive to negative region continuously. So the trip action is setup in such a way that during the positive region it commands EPWM2A to go low and EPWM2B to go high and vice-versa. This ensures peak current limitation occurs during the positive region and valley current limitation occurs during the negative region. In this method of digital implementation, bipolar switching is applied to the single phase H-Bridge inverter.

3. Slope Compensation

3.1 Operating principles

In this paper, the peak-current mode control modulation strategy is referred as a kind of constant-frequency, trailing-edge type modulation. Fig. 2(a) and 2(b) show the sensor outputs compared to the reference signal, with and without slope compensation respectively. As shown in the Fig. 2(a) the dotted line is the perturbation given to the instantaneous inductor current waveform. Initially, the inductor current is perturbed by the amount of ΔI_0 and the perturbation amount increases during consecutive switching cycles as denoted by ΔI_1 and ΔI_2. If no external ramp is added to the reference signal, the current in the circuit will oscillate at half the switching frequency. These oscillations are commonly referred as sub-harmonic oscillations. These sub-harmonic oscillations are produced due to the sample-and-hold effect inherent with the peak current mode control [19]. Fig. 2(b) shows the effect of external ramp compensation. With the same amount of initial perturbation ΔI_0 applied to the inductor current, the amount perturbation decreases during consecutive cycles. As in the case of DC-DC converters, application of the slope compensation can be used to reduce the sub-harmonic oscillations in full-bridge DC-AC inverters, as well. When the duty cycle is greater than 0.5, sub-harmonic oscillations are formed in the DC-DC converter circuits. Besides, the inductor current is influenced by the input voltage and the output voltage, which makes the PWM modulator highly nonlinear and hard to model [20]. Actually, the previous DC-DC criterion for buck-converter is not applicable for H-Bridge inverter with bipolar switching, because the sub-harmonics happen throughout the whole cycle, different from a buck converter. The oscillating principle is as follows.

As discussed in [5], in the discrete time domain, the equation representing the stability criteria is given by:

$$\alpha = (s_f - s_e)/(s_n + s_e) \tag{1}$$

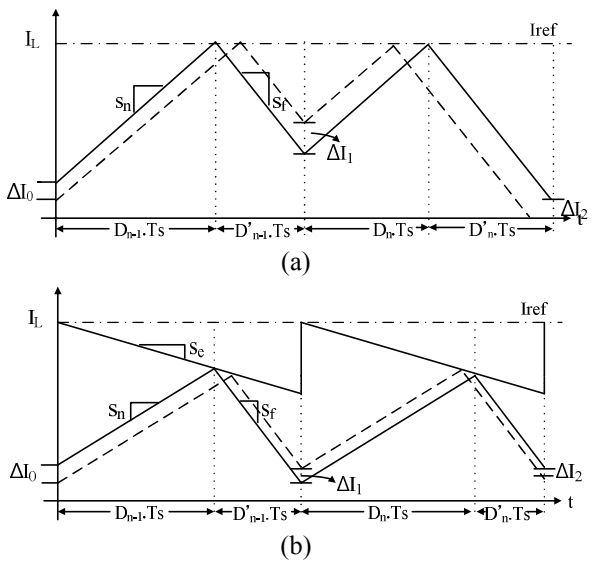


Fig. 2. On-time and off-time slopes of the inductor current waveform: (a) without external slope compensation; (b) with external slope compensation.

When no external ramp is added to the system, it is considered stable if the parameter α, which is defined as the ratio of off-time slope (s_f) to the on-time slope (s_n), is less than unity. For a bipolar-switching H-bridge inverter, the magnitude of the inductor current slope during on-time (s_n) is given by:

$$s_n = (V_{in} - V_{out}) R_i / L \tag{2}$$

Similarly, the magnitude of the inductor current slope during off-time (s_f) is given by:

$$s_f = (-V_{in} - V_{out}) R_i / L \tag{3}$$

which is totally different from the equation of the buck.

From the above mentioned equations, it is clear that α is always greater than the unity except during zero-crossing of output voltage. Hence, the slope compensation is an absolute necessity for stable operation in the H-Bridge inverter with bipolar switching. It is shown that the benefits of peak current mode control are not significantly affected even with application of large external ramps [4].

3.2 H-bridge inverter slope compensator design

According to the mathematical model developed to analyze the stability of slope compensation in [6], the parameter k which is the ratio of inductor current down-slope to the down-slope of the current reference for single phase H-bridge inverter is given by

$$k = \tan\beta \cdot \tan\delta \tag{4}$$

where

$$\tan\beta = \frac{L}{(-V_{in}(t) - V_{out}(t))}, \tag{5}$$

and δ is the angle of current reference with slope compensation. The stability criterion in order to make the system unconditionally stable is derived as:

$$k > 0.5 - \frac{L \cdot \tan\theta}{D \cdot (-V_{in}(t) - V_{out}(t))} - \frac{1-D}{2D} \tag{6}$$

where, θ is angle between inductor current and the horizontal line in the model. Since the output filter inductor is very small, the parameter k must be equal to or greater than 0.5. In order to make the system unconditionally stable the external slope compensation (s_e) applied must be equal to or greater than half of s_f [21]. This can be theoretically verified by plotting the frequency response curve for the current loop gain in H-Bridge inverter. Fig. 3 depicts the small signal model for the closed-loop current-mode control. Using this model and implementing small-signal analysis for the H-Bridge inverter, current loop gain for the system can be derived as follows:

$$T_i = T_1 - T_2 \tag{7}$$

where

$$T_1 = F_m \cdot G_{id} \cdot R_i \cdot H_e \tag{8}$$

$$T_2 = F_m \cdot G_{vd} \cdot K_r \tag{9}$$

Using state-space averaging technique, the expressions for frequency-domain transfer functions for control-to-output voltage (G_{vd}) and control-to-inductor current (G_{id}) of the H-bridge topology are derived as follows:

$$G_{vd} = \frac{\frac{2V_{in}}{LC}}{s\left(s + \frac{1}{RC}\right) + \frac{1}{LC}}. \tag{10}$$

$$G_{id} = \frac{\frac{2V_{in}}{LCR} + \frac{2V_{in} \cdot s}{L}}{s\left(s + \frac{1}{RC}\right) + \frac{1}{LC}}. \tag{11}$$

In case of constant-frequency, trailing-edge modulation, the feed-forward gain from the on-time inductor voltage to control (k_f') is derived as:

$$k_f' = -\frac{DT_s R_i}{L}\left(1 - \frac{D}{2}\right). \tag{12}$$

Similarly, the feed-forward gain from the off-time voltage across the inductor to control (kr') is derived as:

$$k_r' = D'^2 \frac{T_s R_i}{2L} \tag{13}$$

From (12) and (13), the feed-forward gain from output voltage to control (k_r) for full-bridge inverter is derived as:

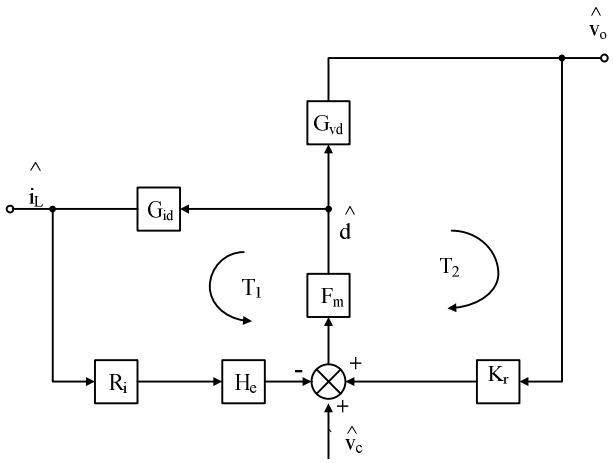
$$k_r = -k_f' - k_r' \tag{14}$$

$$k_r = -\frac{T_s R_i}{2L}(2D^2 - 4D + 1) \tag{15}$$

The expression for F_m is dependent on the current-mode control which is used in the circuit. In case of the constant-frequency, trailing- edge modulation is,

$$F_m = \frac{1}{(s_n + s_e)T_s} \tag{16}$$

From the above equations, the frequency response of current loop gain is plotted as shown in Fig. 4. The



H_e : Equivalent sampling-gain in current feedback
k_r : Feed-forward gain from output voltage to control
T_S : Switching period
R_i : Current- sensing gain
F_m : Duty ratio modulator gain

Fig. 3. Small-signal block diagram for the closed current loop.

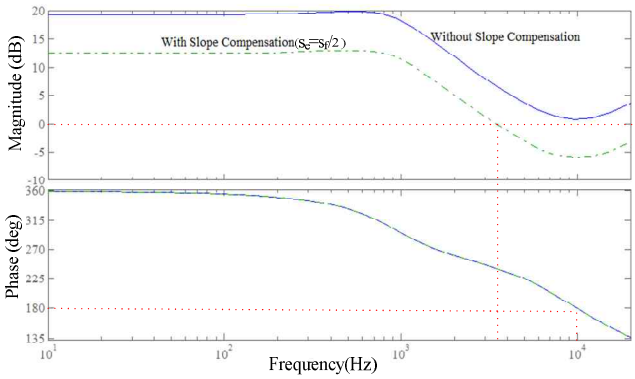


Fig. 4. Frequency response of a current loop gain from the averaged analytic model without and with compensation (where $s_e = s_f/2$).

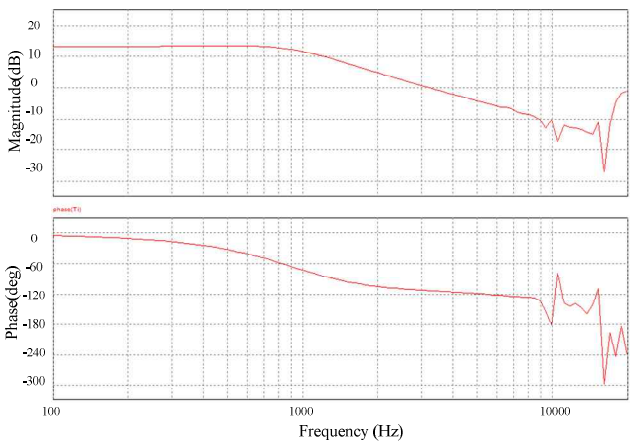


Fig. 5. Frequency response of a current loop gain with slope compensation from the exact PWM switching model by PSIM.

simulation parameters are the same as those of the hardware prototype used in next section. From the frequency response plot, it is evident that without slope compensation, there is no cross over frequency for current loop gain, therefore resulting in an unstable system. The current loop gain can be reduced with an addition of the external slope compensation in the system. The cross over frequency of the current loop with slope compensation is 3.3 kHz with a good phase margin of 65°. Fig. 5 shows the frequency response of the current loop gain with the exact model by PSIM. The exact plot with slope compensation exactly matches with the derived average model, therefore it proves the accuracy of the derived average model.

4. Compensation with Unipolar PWM Switching

4.1 H-bridge inverter slope compensator design

Unipolar PWM switching method has several inherent advantages compared to the bipolar switching. Apart from the cancellation of even order harmonics in the output, unipolar switching has a unique advantage in peak current mode control with regards to sub-harmonic oscillation. In case of unipolar switching, the 50% duty cycle criterion is applicable for the presence of sub-harmonic oscillations. The down-slope of inductor current in unipolar PWM switching is given by,

$$s_f = -V_{out}(R_i / L) \tag{17}$$

This down-slope is similar to buck converter topology. This results in system characteristics similar to the DC-DC converters when peak current controller is implemented. This also helps in reduction in the application of external slope compensation, therefore resulting in better loop gain compared to bipolar switching method. Also in unipolar switching method two of the inverter switches operate in line- frequency, therefore total switching losses are reduced in the power stage.

In case of unipolar switching method, the top switches in the both legs of the inverter operate in the switching frequency, while the bottom switches operate in fundamental frequency of the output. Hence the PWM strategy used in DSC coding becomes complicated compared to bipolar method. In unipolar method, the trip-zone feature is activated only in the top switches of the inverter leg. Fig. 6 shows the circuit diagram of the two-loop peak-current controller (PCC) with a unipolar switching scheme using the DSC. The changes from bipolar switching scheme are evident from the signals given to the switches in the full-bridge circuit. Instead of using just two PWM signals (2A and 2B), three PWM signals (2A, 2B and 3A. 3B is inversion of 3A) are used to control the switches. An outer feedback loop of the load voltage is also realized in the same digital controller. The

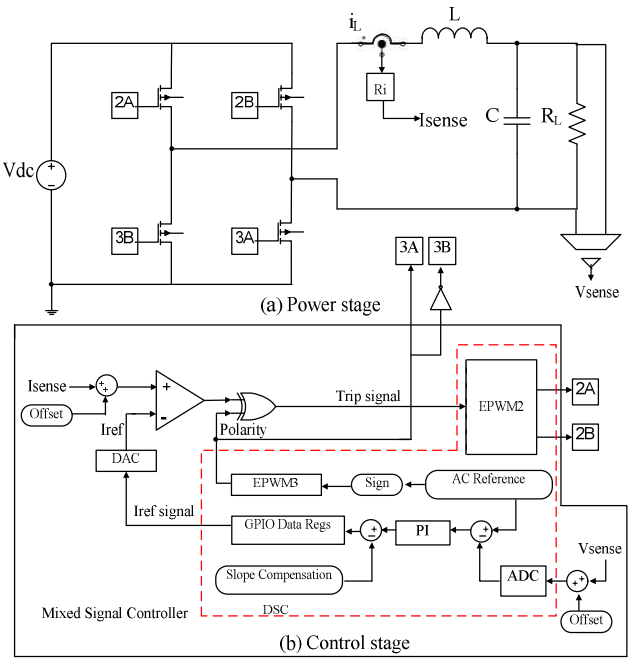


Fig. 6. Circuit diagram of two-loop PCC using unipolar switching which includes PWM 3A.

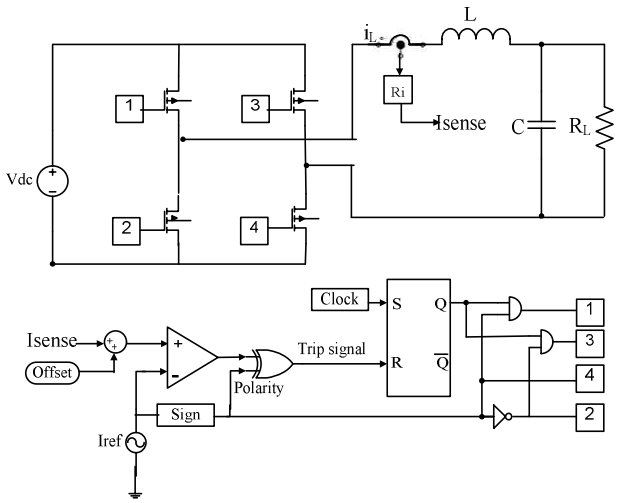


Fig. 7. Single-loop PCC circuit diagram using a unipolar switching.

output of the outer loop PI compensator is merged to the slope compensator to make the inner loop reference. Fig. 7 shows the simulation file of the single-loop PCC using unipolar switching in PSIM, which differs from the bipolar in terms of the PWM switching signals. Fig. 8 also shows the simulation results of unipolar implantation. It can be seen that sub-harmonics does not appear in the region of low duty-cycle, but only around the peak, which is a clear difference from the result of the bipolar.

4.2 Adaptive slope compensation

As aforementioned, the slope compensation required

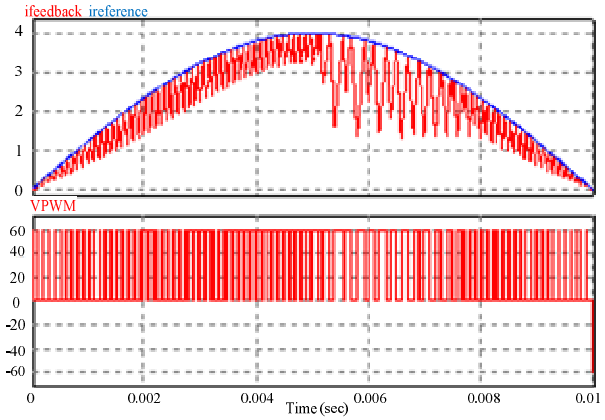


Fig. 8. Results for single-loop PCC using unipolar switching without slope compensation, inductor current and the reference (top), PWM switching waveform (bottom).

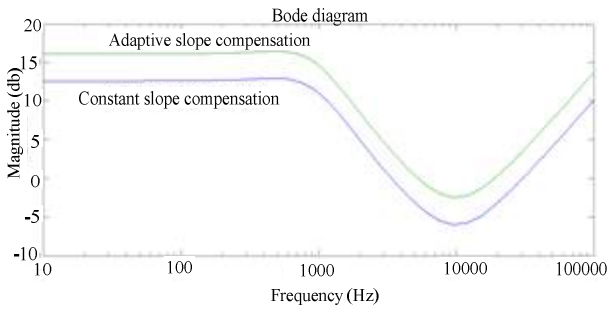


Fig. 9. Current loop gain with unified and adaptive slope compensation.

to remove sub-harmonic oscillations from the output is greater than the half of the inductor current down slope. From equation (17), it can be seen that the down slope of inductor current is proportional to the output voltage. Therefore, by the feedback of the output voltage through ADC channel, we can calculate the exact value of the down slope of inductor current. This value is used to instantaneously change the compensation of external slope in every switching cycle, based on the output voltage. This method of implementing slope compensation is known as adaptive slope compensation. In case of the unipolar switching scheme, the adaptive slope compensation is preferred to the previous constant-slope compensation, because the slope compensation is not necessary in unipolar when the duty-cycle is less than 50%. Since the constant slope throughout the full cycle affects the current loop-gain of the peak current controller, it would be better to remove or attenuate the compensation whenever it is allowed. Fig. 9 shows the frequency response of the current loop gain with the adaptive slope compensation versus the unified slope compensation when the output (load) voltage is 10V, around zero-crossing. Unlike the constant slope compensation, the low voltage loop-gain is higher than the peak voltage conditions due to the change of the external slope compensation parameter.

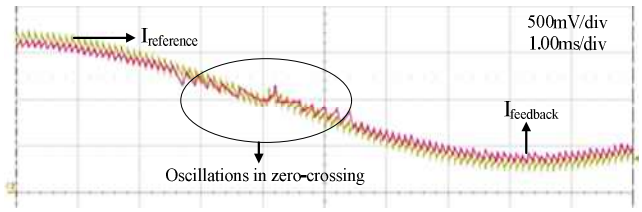


Fig. 10. Constant slope compensation, Ireference (C1), Ifeedback (C2).

Not only the degradation of loop gain, there is a critical reason that the adaptive is preferred. When the constant slope is used in this digital implementation, the external slope compensation near the zero crossing region becomes equal to the down-slope of inductor current such as:

$$s_e = s_f \tag{18}$$

Under this condition, the trip signal in the switching cycle stays low and it causes the PWM signals to stay low during the several consecutive cycles. This causes low frequency oscillations near zero crossing regions as shown in Fig. 10. From the aforementioned reasons, implementing adaptive slope compensation is one of the optimal solutions for unipolar switching scheme.

5. Hardware Implementation

The circuit shown in Fig. 1 was developed and tested for the verification of the analysis. The chosen parameters were Vin=75V, L=2.8mH, C=10μF, RL=12Ω, Ri=0.2, Iref=4A and switching frequency 20 kHz. In order to implement the digital to analog conversion (DAC) for the reference, a 12bit R-2R ladder circuit DAC IC AD7247 was used. The output is connected to the comparator where it is compared with the feedback current. The output of the comparator is combined with EPWM3 using an X-OR gate. This final signal is connected to the trip zone pin GPIO12 of the DSC. In the EPWM2 module, which drives the switches with 20 kHz PWM, inherent dead time of 2μsec is added between 2A and 2B to prevent the cross conduction. Fig. 11 shows the hardware prototype used for the experiment along with the DSC.

Fig. 12 shows the inductor current waveforms with and without slope compensation. The slope compensation reduces the sub-harmonic oscillations occurring especially during the peak region of inductor current waveform. In

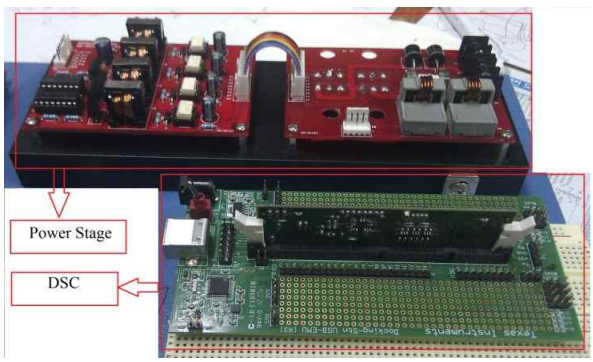


Fig. 11. Single-phase H-Bridge inverter (top) connected to 200W load along with the DSC (bottom).

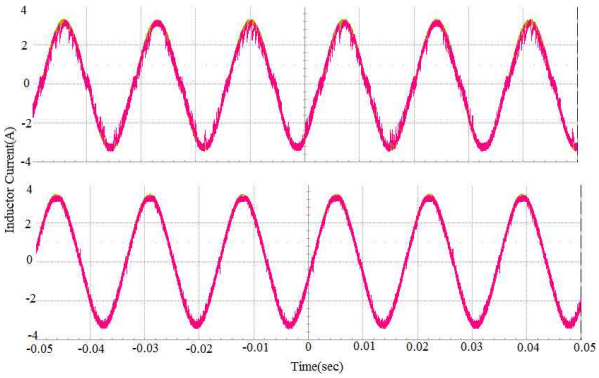
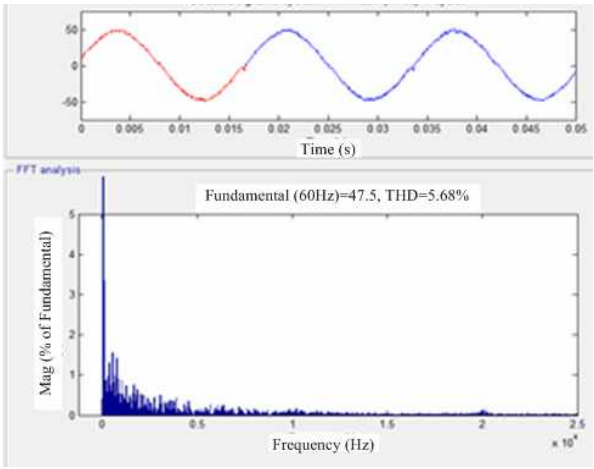
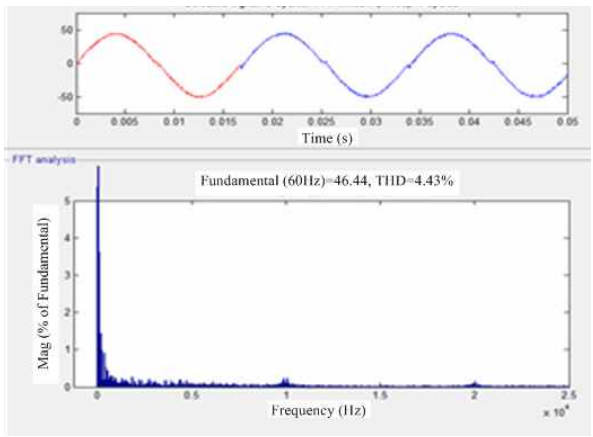


Fig. 12. Inductor current waveforms without slope (top) and with constant slope compensation (bottom).



(a)

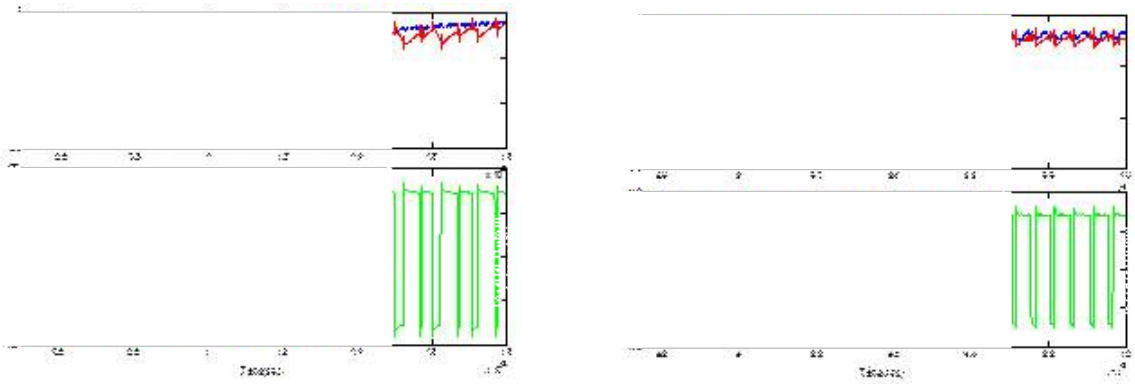


(b)

Fig. 13. FFT scope for load voltage: (a) without slope compensation and (b) with slope compensation.

Fig. 13, the hardware data of the load voltage is collected and FFT analysis is done in MATLAB. The reduction of THDs which is more than 1% with the introduction of slope compensation can be clearly seen in the FFT scope. The presence of the sub-harmonics in the system is prominent when slope compensation is not used. Slope compensation helps reduce these oscillations in the system and thereby making the system stable. Fig. 14 shows the reduction of the oscillations due to the introduction of slope compensation. The hardware waveforms were redrawn by MATLAB through the data collections.

The programming efficiency of this method of



(a) Without slope compensation. (b) With slope compensation.

Fig. 14. Inductor current and inverter voltage waveforms: (a) without slope; (b) with constant slope compensation.

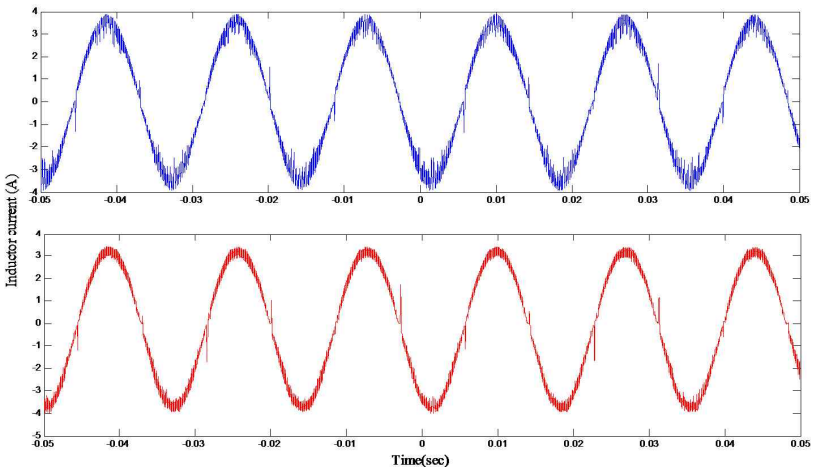
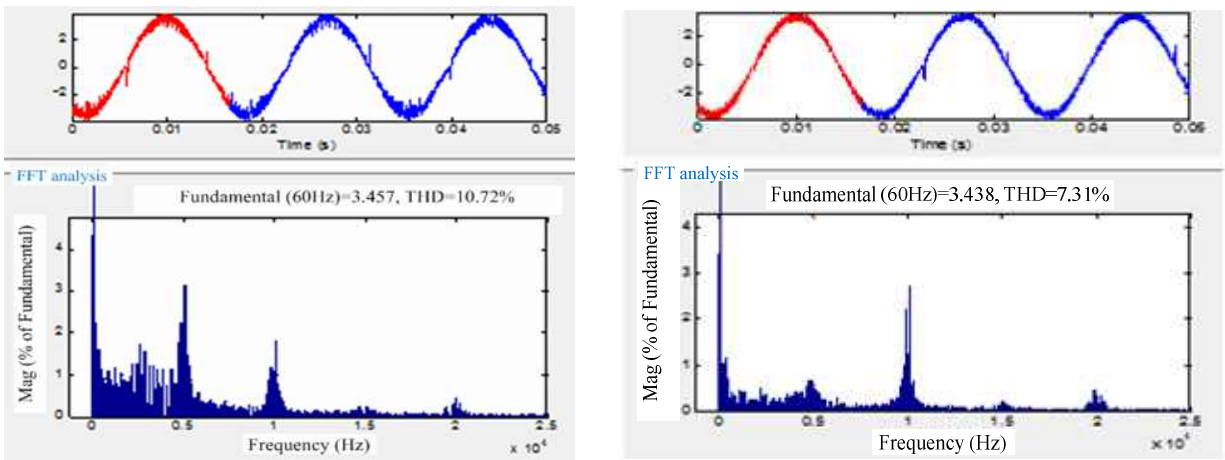


Fig. 15. Inductor current waveforms (top) without slope (bottom) with adaptive slope compensation.



(a) Without slope compensation (b) With adaptive slope compensation

Fig. 16. MATLAB FFT scope for inductor current: (a) without slope; (b) with adaptive slope compensation.

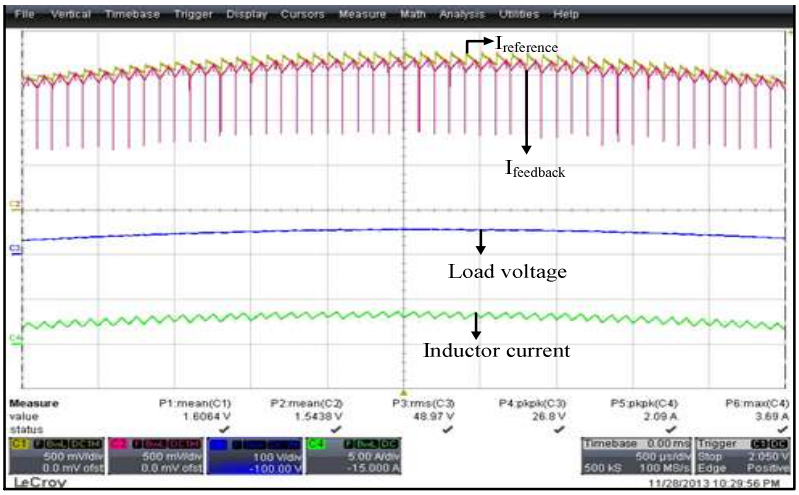
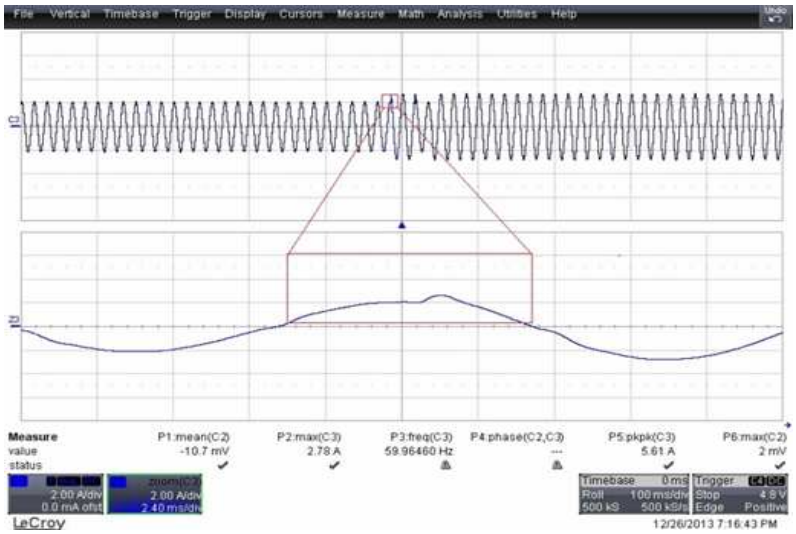
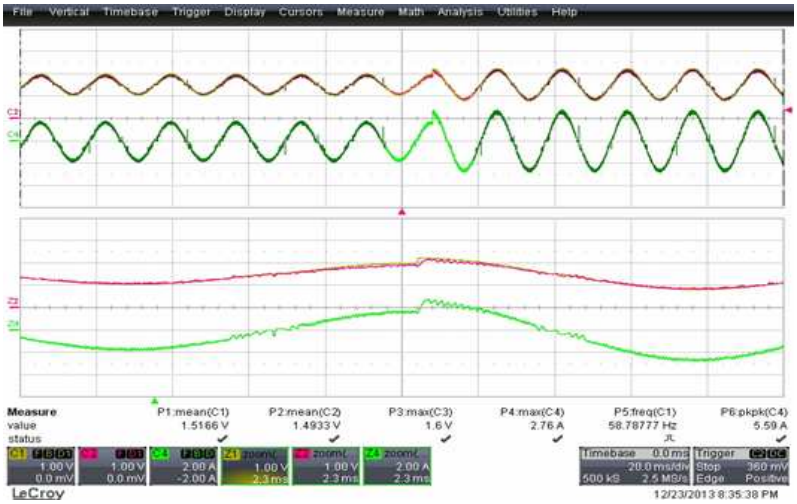


Fig. 17. Adaptive slope compensation implemented in the reference signal Ireference(C1), Ifeedback (C2), load voltage (C3) and inductor current (C4).



(a) Inductor current waveform during step-change test for PI controller (100ms/div.)



(b) Inductor current waveform during step-change test for PCC (20ms/div.)

Fig. 18. Dynamic comparison between a conventional PI controller and a peak-current mode controller (PCC) by a step-change in load.

implementing peak current controller can be known from the execution speed of the DSC code and the remaining part of the DSCs computational part available for other tasks. Using CCS "Profiler" and checking the code in single step, the execution time for the complete ISR was found to be 1450nsec. Hence, only 22% of the high frequency EPWM1 ISR has been utilized in the code. The available computing power can used to implement the outer loop and also to control multiple power plants required especially in stand-alone renewable energy systems as shown in [22].

Also, the circuit shown in Fig. 6 was developed and tested for the verification of the analysis. Fig. 15 shows the reduction in sub-harmonic oscillations in the inductor current when adaptive slope compensation is applied in unipolar switching scheme. Fig. 16 is used to show the removal of sub-harmonic oscillations using adaptive slope compensation. The MATLAB FFT scope shows more than 2% reduction in harmonics around half the switching frequency. Fig. 17 clearly shows the cycle-by-cycle variation in the amount of slope compensation in the reference signal. By the comparison of the sawtooth in C1 between the low and high region, the slope of the sawtooth seems to change continuously in every switching cycle.

For comparison with a conventional PI controller, an inductor current waveform of a conventional PI controller is shown in Fig. 18. The dynamic performance of the PI controller was tested by providing a step change in the load and compared with PCC method. It can be seen that the PI controller takes more time to reach steady state compared to PCC method.

In the proposed scheme, when the reference moves from positive region to negative region, the PWM pattern and trip action is modified in the ePWM2 & ePWM3 modules. Because of the delay between the trip action input from the comparator and PWM interrupt during zero crossing region for one switching cycle miss-match occurs between trip action and PWM pattern. This can be solved by either disabling the trip action during zero crossing region using blanking method or implementing PCC in a complete digital loop with very high sampling instead of the proposed mixed-signal scheme. Even though the THDs of the proposed scheme with zero crossing distortion satisfy the desired limit, we have included the result of the elimination of this distortion using blanking method in bipolar switching in Fig. 19 of the manuscript, as shown below.

A rectifier load was added to the hardware prototype which shares 15% of the output power, to test the effectiveness of the proposed scheme under non-linear load conditions. Fig. 20 shows the load voltage and the current flowing to the rectifier load. The load voltage is able to track the reference despite the effect of the rectifier load. The MATLAB FFT scope for the obtained load voltage shows THD (4.25%) was within the permissible limits as in Fig. 21.

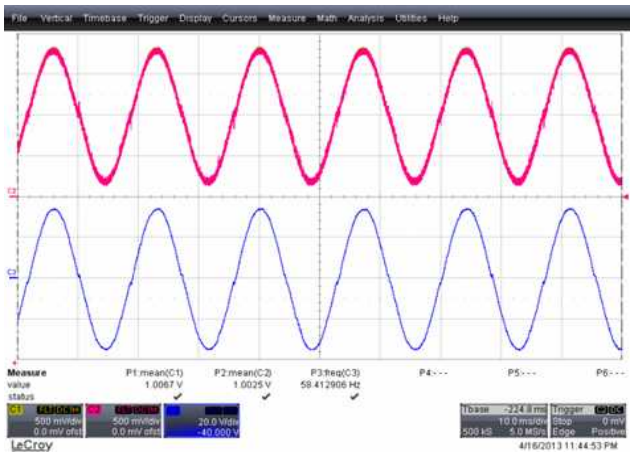


Fig. 19. Peak-current mode controller waveforms eliminating the zero-crossing distortion: (a) inductor current (top); (b) output voltage (bottom).

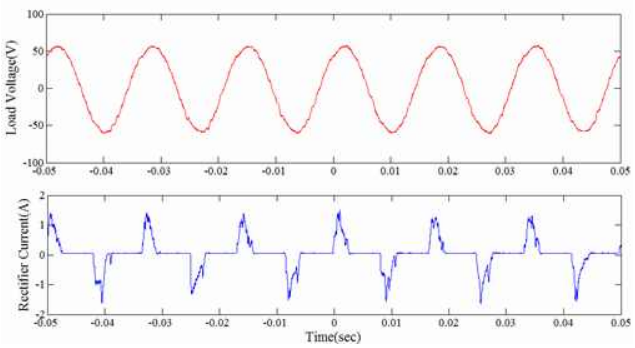


Fig. 20. Load voltage(top) and current flowing to the rectifier load(bottom).

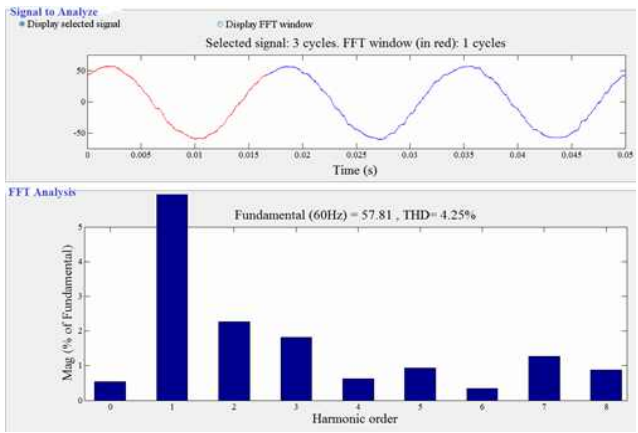


Fig. 21. MATLAB FFT scope of the load voltage with additional rectifier load.

6. Conclusion

In this paper, a novel cycle-by-cycle current control method by peak-valley current-mode controller with digital slope compensation has been proposed for an H-bridge

inverter. Different from the current control for DC-DC, DC-AC requires the control-mode transition from peak to valley or vice versa in every swing cycle. The extraordinary operation was efficiently implemented by a single Exclusive-OR gate. From the small-signal models for feed-forward and sampling gain terms of the peak current mode control method, the current loop gain transfer function for the H-bridge inverter has been derived. The frequency response of the derived average model for the current loop gain was found to be in correlation with the exact PWM switching model.

The inherent problem of sub-harmonics in peak current control has been reduced with the external slope compensation. The effectiveness of the slope compensation has been shown by the reduction in THDs of the load voltage and the stable inductor current waveform. Also, by using the mixed signal comparator and cycle-by-cycle trip action, the performance of this controller and effective usage of the digital controller has been ensured. The implementation of peak current controller with a unipolar switching scheme was also done with adaptive slope compensation. The digital controller contributes to the instantaneous slope compensation change, and the analysis shows that the adaptive one is more effective to the unipolar switching inverter than the constant slope compensation. Simulation and experimental verification have been done with a 200W hardware prototype of an H-bridge inverter.

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