JPE 15-5-20

http://dx.doi.org/10.6113/JPE.2015.15.5.1338
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

DC Injection Control for Grid-Connected Single-Phase Inverters Based on Virtual Capacitor

Wei Wang†, Ping Wang*, Taizhou Bei*, and Mengmeng Cai*

†,*Smart Grid Key Laboratory of Ministry of Education, Tianjin University, Tianjin, China

Abstract

DC injection is a critical issue in transformerless grid-connected inverters. DC injection control based on virtual capacitor has the advantages of low cost, low loss, high accuracy and easy implementation. In this paper, the principle of DC injection control based on virtual capacitor was analyzed. In addition, the applicable conditions, working process, steady state error and advantages were also discussed in detail. The design of the control parameters based on virtual capacitor was proposed in a grid-connected inverter with LCL filter. The robustness of the control parameters was also discussed. Simulation and experimental results verify the validity of the analysis and demonstrate that this research has a certain value in engineering applications.

Key words: DC injection control, Design of parameters, LCL filter, Robustness, Virtual capacitor

I. INTRODUCTION

In recent years, there has been an increase in the number of small-scale generators connected to the distributed power network. Typically, a current-controlled inverter is utilized to provide the grid-connected interface [1]. In early days, the transformer was usually installed between the inverter and the grid for voltage matching and electrical isolation. However, the transformer has disadvantages in terms of volume, weight and efficiency. Non-isolated grid-connected inverters have advantages over isolated grid connected inverters in terms of economy and technology, and they are widely used in small power applications. When the isolation transformer is removed, the DC injection becomes a big problem [2]. The DC current being injected into the grid must be less than 0.5% of the rated current according to IEEE Std. 929-2000.

The Spanish scholar V. Salas pointed out that the DC injection phenomena exists in many PV grid-connected inverters [3]. The main reasons for DC injection are: asymmetry in the switching of the semiconductor devices, which is caused by imbalance in the turn-on and turn-off times of the semiconductor switches; and pulse width imbalance in the pulse width modulation (PWM) process, or possible mismatch in the alignment of the gate drive signals. The offset drift in the current measurement also creates unwanted DC component in the inverter output current [4]. The instruction current especially produced by analog devices, may contain unwanted DC component. DC injection results in many problems. It may lead to saturation of the transformer, accelerate the corrosion of the network cabling, threat the safety of the power equipment, and make the AC motor generate torque ripple or heat, and so on [5].

Scholars have put forward many solutions to this problem. These solutions can be divided into three categories. The first, some inverter topologies are naturally capable of preventing DC current components, such as the half bridge inverter [6] or three-level diode-clamped inverter [7]. The common characteristic of these topologies is that there is one capacitor present in the current path, hence blocking the DC current. However, the former requires a higher DC link voltage, resulting in higher voltage stress and more loss. The latter requires more switching devices and capacitors, which increases the size and cost of the inverter. In addition, the presence of a decoupling capacitor is the major factor limiting the life of the inverter. The second, detection and compensation method, such as the auto-calibrating DC link current sensing technique [4], the parallel transformer detection method [8], the two stage RC circuit detection method [9], and the magnetic saturation detection method [10]. However, since the DC current is quite small, the above methods are either too dependent on the current sensor

Manuscript received Aug. 18, 2014; accepted Apr. 5, 2015
Recommended for publication by Associate Editor Sung-Yeul Park.
†Corresponding Author: weiwang19891116@126.com
Tel: +86-022-27404101, Fax: +86-022-27404101, Tianjin University
*Smart Grid Key Lab. of Ministry of Education, Tianjin Univ., China

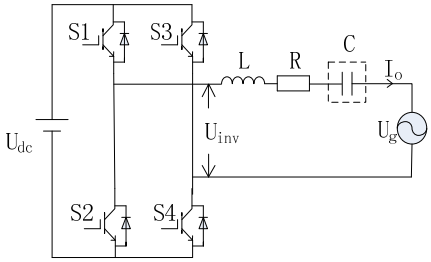

Fig. 1. Single-phase grid-connected inverters with DC-block capacitor.

accuracy or the control algorithm is too complex. In addition, the detection circuit increases the complexity and volume of the system. The third, DC block capacitor method. A capacitor is put right at the output end of the inverter to block the DC current. Depending on whether the capacitor exists or not, this kind of method is divided into the DC-block capacitor method and the virtual capacitor method. When the DC-block capacitor method is used, there is a real capacitor in series in the circuit. Although this method effectively blocks the DC current, the capacitor must present a low reactance at the fundamental frequency (50Hz) for a small voltage drop across the capacitor. As a result, the capacitance is large, and the system volume and cost increases. What is worse, the dynamic response becomes bad and the power loss is inevitable [4]. Since the DC-block capacitor method has many disadvantages, the virtual capacitor method is proposed [2]. In this paper, DC injection control based on virtual capacitor is analyzed in a single-phase grid-connected H-bridge inverter. In addition, its application conditions, work process, and steady state error are discussed in detail. The design of the control parameters based on virtual capacitor is proposed in the inverter with a LCL filter. Simulation and experimental results demonstrate the validity of the analysis and show that this research has a certain value in engineering applications.

II. STRATEGY DESCRIPTION

A. The Concept of Virtual Capacitor

To explain this concept clearly, a grid-connected single -phase H-bridge inverter with L filter is firstly analyzed. As shown in Fig. 1, where U_{dc} is provided by renewable energy source, since this research focuses on DC injection control in the current loop, constant value U_{dc} is just put here. The inverter connects to the grid through the L filter. The current regulator makes the grid current I_o the same frequency and phase as the grid voltage U_g, which is unity power factor operation.

When the switching frequency of the system is high enough, the H-bridge inverter in Fig. 1 can be simplified as a linear ratio of K_{PWM}. U_{inv} is the output voltage of the inverter. L and C are the filter inductance and DC-block capacitor, respectively. R is the equivalent resistance of the filter

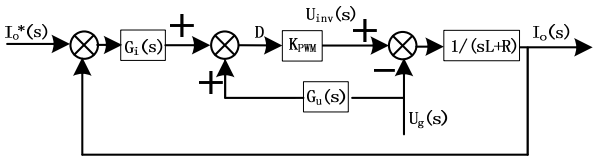

Fig. 2. Control model of grid-connected inverters without DC-block capacitor.

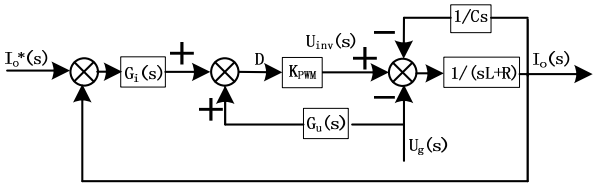

Fig. 3. Control model of grid-connected inverters with DC-block capacitor.

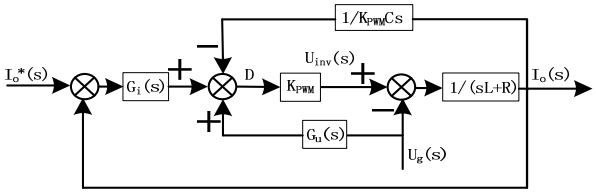

Fig. 4. Control model of grid-connected inverters with virtual capacitor.

inductance. Since the grid voltage is equivalent to the interference for the control of the grid current, the voltage feedforward control is used to alleviate the burden of the current regulator $G_i(s)$. Let $G_u(s) = 1/K_{PWM}$. Suppose that the main reasons for DC injection are equivalent to the instruction current $I_o^*(s)$ containing the DC component. It is easy to get control model of grid-connected inverters without and with DC-block capacitor, as shown in Fig. 2 and Fig. 3.

The loop transfer function product remains unchanged through the transformation according to the principle in the control theory. In Fig. 4, the transfer function of $1/K_{PWM}Cs$ is put feedforward to the duty ratio D instead of the transfer function of the DC-block capacitor 1/Cs in Fig. 3. Although the transfer functions of the whole system in Fig. 3 and Fig. 4 are the same, in the system represented by Fig. 4, the current is measured through the current sensor, then numerical integration is done in the controller, and the integral result is calculated with the output of the current regulator $G_i(s)$. It has exactly the same effect as the DC-block capacitor. However, because it is not objective existence, it is called virtual capacitor. Considering the voltage feedforward function, the transfer function of closed loop with DC block capacitor and virtual capacitor system are written in Eq. (1) and Eq. (2), respectively.

$$\frac{I_o(s)}{I_o^*(s)} = \frac{K_{PWM}G_i(s)}{K_{PWM}G_i(s) + sL + R} \tag{1}$$

$$\frac{I_o(s)}{I_o^*(s)} = \frac{K_{PWM}G_i(s)Cs}{LCs^2 + RCs + K_{PWM}CG_i(s)s + 1} \tag{2}$$

B. The Principle of DC Injection Control Based on Virtual Capacitor

Replace s with jω in Eq. (1) and Eq. (2). The closed loop frequency responses of the two systems are derived and the DC gain for the closed loop system is derived when ω=0. As can be seen, the transfer function in Eq. (2) has one more zero located at the origin than that in Eq. (1). This is due to the presence of virtual capacitor, which makes it possible to block the DC component. It is obvious that the current regulator $G_i(s)$ will influence the system closed loop transfer function. Proportional integral (PI) and Proportional resonant (PR) current regulators, which are commonly used in grid-connected inverters, will be analyzed, and the applicable conditions, working process and steady state error will be discussed. The transfer functions of PI regulator and PR regulator are shown in Eq. (3) and Eq. (4), respectively.

$$G_i(s) = \frac{k_p s + k_i}{s} \tag{3}$$

$$G_i(s) = k_p + \frac{k_r s}{s^2 + \omega_0^2} \tag{4}$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), Eq. (5) and Eq. (6) are derived, respectively.

$$\frac{I_o(s)}{I_o^*(s)} = \frac{K_{PWM}k_pCs + K_{PWM}k_iC}{LCs^2 + (R + K_{PWM}k_p)Cs + K_{PWM}k_iC + 1} \tag{5}$$

$$\frac{I_o(s)}{I_o^*(s)} = \frac{(K_{PWM}k_pCs^2 + K_{PWM}k_iCs + K_{PWM}k_p\omega_0^2C)s}{LCs^4 + (R + K_{PWM}k_p)Cs^3 + (LC\omega_0^2 + K_{PWM}k_iC + 1)s^2 + (R + K_{PWM}k_p)\omega_0^2Cs + \omega_0^2} \tag{6}$$

For Eq. (5), the PI current regulator itself contains a pole located at the origin. This cancels out the zero located at the origin which is introduced by virtual capacitor. As a result, it loses the ability to block the DC component. For Eq. (6), the PR current regulator does not have a pole located at the origin. Therefore, the zero that located at the origin remains, and the system still has the ability to block the DC component. The applicable conditions of DC injection control based on virtual capacitor: Make sure the current regulator does not contain a pole located at the origin.

Since the working process of an inverter with virtual capacitor is similar to that of the DC-block capacitor, the working process is discussed on the basis of the DC-block capacitor below. Then the advantage that virtual capacitor has over DC-block capacitor in blocking DC component is explained through comparison. Assume that the current regulator is PR, the instruction current $I_o^*(t)$ contains DC component I_{dc}. In fact, most of the factors causing DC component can be equivalent to this. As shown in Eq. (7):

$$I_o^*(t) = I_{ac}\sin(\omega_0 t) + I_{dc} \tag{7}$$

Due to the DC component in the instruction current, the inverter output voltage U_{inv} inverter has DC component under the control of the current regulator when the system starts. The output current is sinusoidal alternating current with DC component. It is the DC current charging that makes the average value of the capacitor voltage U_{c_ave} increases, after a dynamic process, the steady state average value of the capacitor voltage comes to a constant value $U_{c\_ave\_stable}$. The DC voltage presented in the inverter output voltage U_{inv} is offset by this constant value and the DC current is blocked. The process above does not stop until the DC component in the grid current becomes zero. As a result, the steady state error of this method is zero. In the steady state, the average value of the DC-block capacitor voltage $U_{c\_ave\_stable}$ is determined by Eq. (8); and the peak to peak voltage of the DC-block capacitor $U_{c\_pp\_stable}$ is determined by the fundamental component of the instruction current and the capacitance of the DC-block capacitor, as shown in Eq. (9):

$$U_{c\_ave\_stable} = k_p I_{dc} K_{PWM} \tag{8}$$

$$U_{c\_pp\_stable} = 2I_{ac} * \frac{1}{\omega_0 C} \tag{9}$$

There are several problems when the inverter works with DC-block capacitor from the above analysis. First of all, in order to reduce the steady-state voltage across the capacitor $U_{c\_pp\_stable}$, the capacitance of the DC-block capacitor should be as large as possible. However, a big capacitance means a bad dynamic response in blocking the DC component and the contradiction between the two is very difficult to reconcile. Secondly, the average value of the DC-block capacitor voltage $U_{c\_ave\_stable}$ should not be too large due to electrical insulation, so that the choice of k_p in the PR current regulator should not be large, which limits the system bandwidth and a bad dynamic response occurs. In addition, a small open loop gain usually increases the steady state current error in the fundamental frequency. Finally, although the DC component in the grid current is blocked, the inverter voltage U_{inv} still contains DC component, which increases the loss of the switching devices. At the same time, the DC-block capacitor itself has power loss.

The working process of the inverter with virtual capacitor is very similar to that of DC-block capacitor. However, there are several different points. First, the integral action of the output current is not by the DC-block capacitor charging but by numerical integration of the measurement value of the current, namely capacitor virtualization. Second, because the equivalent transformation increases the proportional coefficient $1/K_{PWM}$, the voltage of the virtual capacitor is just $1/K_{PWM}$ as that of the DC-block capacitor. Third, since the integral action is put forward to the duty ratio D, just before the inverter, the inverter voltage U_{inv} contains no DC component.

C. The Advantage of Virtual Capacitor

DC injection control based on virtual capacitor is essentially a detection and compensation method. The DC component in the output current is derived through numerical integration of the measurement values of the current, and then the feedback control is used to prevent the DC current

injection into the grid system. This strategy has many advantages. First, since the capacitor voltage has become a numerical integration in the controller, the electrical insulation or power loss of the capacitor is not a problem. In addition, the capacitance can be smaller to improve the dynamic response and k_p can be larger to increase the system open loop gain and bandwidth. Second, since the inverter voltage U_{inv} contains no DC component, the loss of the switching devices is significantly reduced. Third, when the system works, as long as DC component exists in the output current, the numerical integration and the feedback control works. Therefore, the steady state error of this strategy is zero and it can effectively block the DC component caused by asymmetry in the switching of the semiconductor devices or the undesirable instruction current. Therefore, all of the factors above can be equivalent to Eq. (7). In addition, even small DC component can be easily detected due to the numerical integration. As a result, it is less dependent on sensor accuracy. Fourth, since the strategy can be realized in software and requires no additional hardware, the realization is simple and low-cost.

III. COMBINED THE VIRTUAL CAPACITOR WITH LCL FILTER

A. Inverters with LCL Filter and Virtual Capacitor

In recent years, grid-connected inverters have been increasingly adopting LCL filter to reduce the inductance, increase the attenuation ability of high frequency harmonics, and achieve a good dynamic response. However, the resonance of LCL filter may cause instability of the system. Therefore, it is necessary to take effective measures to increase the damping. Common solutions to the resonance problem are the active damping method and the passive damping method. Although the active damping method can eliminate the loss, the control method is complex and sensitive to the circuit parameters. In addition, it usually requires an additional current sensor. A resistor in series with the capacitor is a commonly used passive damping method. This can effectively reduce the amplitude of the LCL resonance and have relatively low loss. The strategy is adopted in this scheme. DC injection control based on virtual capacitor and LCL filter is combined in the single-phase grid-connected inverter system. The main circuit is shown in Fig. 5. The design of the control parameters is discussed in the following part as an example to illustrate the advantages of the proposed strategy.

B. The Design of the Control Parameters

The basic parameters of the system are as follows: rated power: P_n=5kW, grid voltage: U_g=220V/50Hz, DC link voltage: U_{dc}=380V, and switching frequency: f_c=10kHz. The control model of grid-connected inverters with LCL filter and

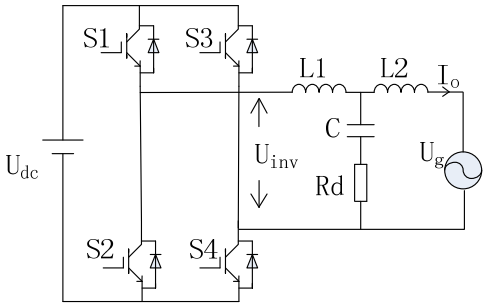

Fig. 5. Single-phase grid-connected inverters with LCL filter.

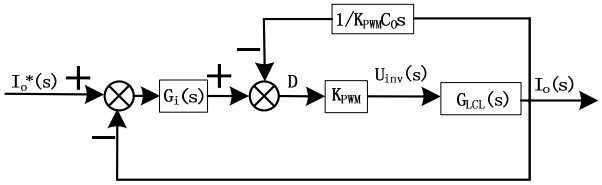

Fig. 6. Control model of grid-connected inverters with LCL filter and virtual capacitor.

virtual capacitor is shown in Fig. 6. In order to simplify the control model, $G_{LCL}(s)$ is used to represent the LCL filter in the circuit. In addition, the voltage feedforward control is omitted in Fig. 6, despite the fact that it really exists in the controller. Since the current regulator PR has very high gain at the fundamental frequency and the voltage feedforward control is used, the impact of the grid voltage can be temporarily ignored. The LCL parameter are as follows: L_1=2.5mH, L_2=0.5mH, C=15uF, and R_d=10Ω. $G_{LCL}(s)$ in Fig. 6 is shown in Eq. (10).

$$G_{LCL}(s)=\frac{R_dCs+1}{L_1L_2Cs^3+R_dC(L_1+L_2)s^2+(L_1+L_2)s} \tag{10}$$

The traditional PR controller is heavily dependent on the element accuracy or word length of the digital controller. Although the gain at the fundamental frequency is infinite, once the grid frequency changes slightly, it declines rapidly. Therefore, a quasi-proportion resonant, namely Quasi-PR, is used in this paper. It retains the high gain at the fundamental frequency and reduces the influence of frequency change. The Quasi-PR current regulator is shown in Eq. (11). The parameters of the system to be designed are as follows: the virtual capacitor C_0, k_p, k_r, ω_c.

$$G_i(s)=k_p+\frac{2k_r\omega_c s}{s^2+2\omega_c s+\omega_0^2} \tag{11}$$

First of all, the design of the virtual capacitor C_0 is discussed. The responses of the L, LCL and LCL with R_d are almost the same before the resonance frequency [11]. A Bode diagram of the L, LCL and LCL with R_d is shown in Fig. 7. When the LCL with R_d and the LCL are compared, due to the passive damping, the resonance peak is greatly decreased. Of course, the attenuation of the high frequency harmonics declines. However it is still in the acceptable range. According to Fig. 7, at the harmonic of 20kHz, which caused

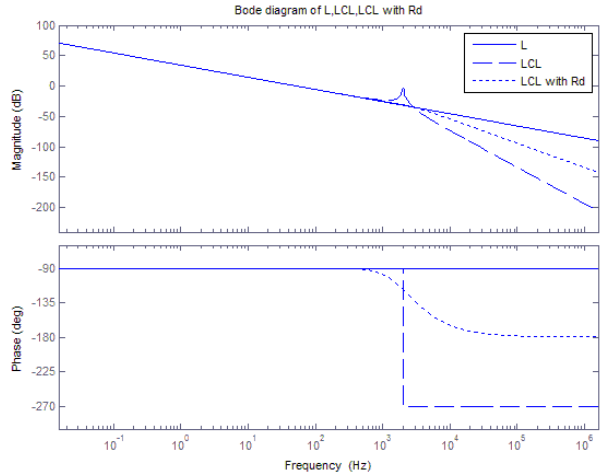

Fig. 7. Bode diagram of L, LCL, LCL with R_d.

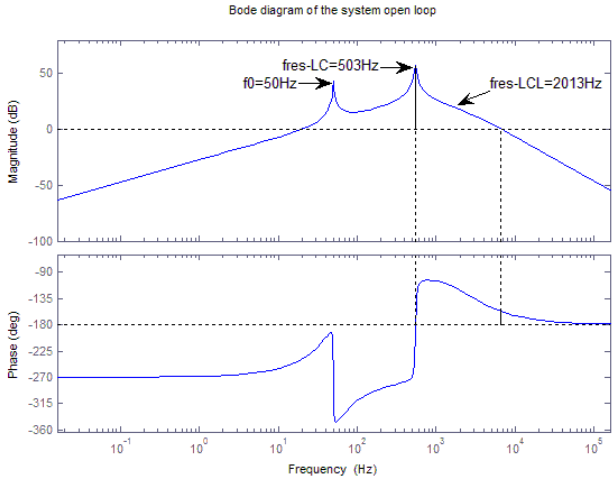

Fig. 8. Bode diagram of the system open loop.

by the switching frequency, the magnitude of the LCL is -91.3dB and that of the LCL with R_d is -65.8dB. Since the LCL with R_d is similar to the L before the resonance frequency, when the virtual capacitor is applied in the inverter, the LC series resonance appears.

Assume that the LC series resonance frequency is f_{res_LC}, the resonance frequency of the LCL filter is f_{res_LCL}, and the resonance frequency of the current regulator is f_0. Expression of f_{res_LCL} and f_{res_LC} are shown in Eq. (12) and Eq. (13). On the one hand, f_{res_LC} must be smaller than f_{res_LCL} and a considerable margin must be set aside, otherwise it will damage the attenuation of the high frequency harmonic. In addition, if f_{res_LC} is too large, which means that C_0 is too small, two poles of the system will be too close to the imaginary axis no matter what k_p and k_r are. As a result, the system is difficult to stabilize. On the other hand, f_{res_LC} must be larger than f_0. If f_{res_LC} is too small, which means that C_0 is too large, the dynamic response of the system is bad. The parameter C_0 is determined by Eq.(14) after the tradeoff. C_0=33.32uF is derived after the calculation. Bode diagram of the system open loop is shown in Fig. 8.

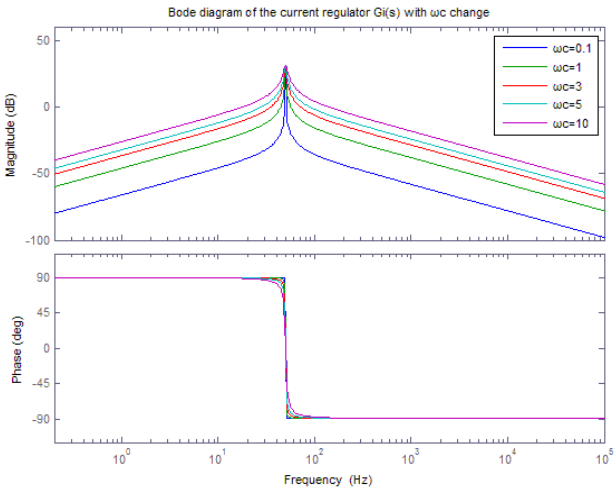

Fig. 9. Bode diagram of the current regulator $G_i(s)$ with ω_c

$$f_{res\_LCL} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{12}$$

$$f_{res\_LC} = \frac{1}{2\pi\sqrt{(L_1 + L_2)\ C_0}} \tag{13}$$

$$f_{res\_LC} \approx \frac{1}{4} f_{res\_LCL} \approx 10\, f_0 \tag{14}$$

There are 3 parameters to be designed (k_p, k_r and ω_c) in the current regulator $G_i(s)$. Secondly, the parameter ω_c is designed. Suppose that k_p=0, k_r=40 and ω_c =0.1, 1, 3, 5, 10. Then observe the change of $G_i(s)$ with ω_c. Bode diagram of the current regulator $G_i(s)$ with ω_c change is shown in Fig. 9. According to Fig. 9, ω_c affects the gain and bandwidth of $G_i(s)$. Suppose that the frequency fluctuation is ±0.5Hz in the grid, which requires that the bandwidth of $G_i(s)$ be 2π rad/s around the fundamental frequency. ω_c=3 can meet the above requirements after trying.

$$G_{LCL\_C0}(s) = \frac{(R_d C s + 1) C_0 s}{L_1 L_2 C C_0 s^4 + R_d C C_0 (L_1 + L_2) s^3 + (L_1 + L_2) C_0 s^2 + R_d C s + 1} = \frac{N}{M} \tag{15}$$

$$D(s) = 1 + K_{PWM} G_i(s) G_{LCL\_C0}(s) \tag{16}$$

$$1 + k_p \frac{K_{PWM} N(s^2 + 2\omega_c s + \omega_0^2)}{2K_{PWM} k_r \omega_c s N + M(s^2 + 2\omega_c s + \omega_0^2)} = 0 \tag{17}$$

Finally, the parameter k_p and k_r are designed. k_p and k_r are two free variables. k_p is the proportional gain that determines both the dynamics of the system, such as bandwidth, and the steady state performance of the system in terms of stability, phase and gain margin, steady state error and total harmonic distortion (THD). k_r mainly affects the open loop gain around the fundamental frequency. In order to take into account the performance of the system dynamic and the steady state, the root locus of the whole system is made to select appropriate value for k_p and k_r. Combine the integral transfer function of virtual capacitor with the transfer function LCL filter, and $G_{LCL\_C0}(s)$ is derived, as shown in Eq. (15). The characteristic equation of the system closed loop is shown in Eq. (16).

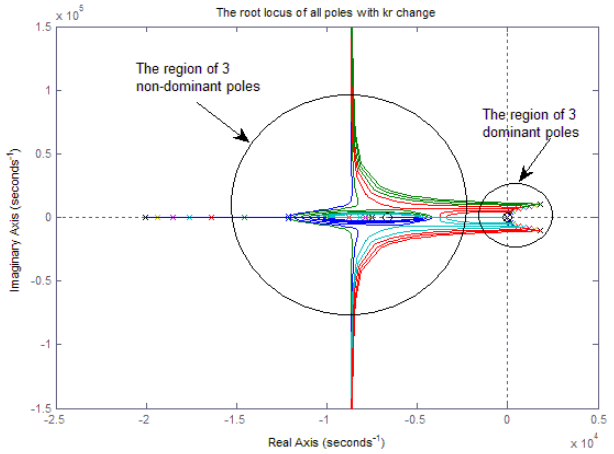

Fig. 10. The root locus of all poles with kr change.

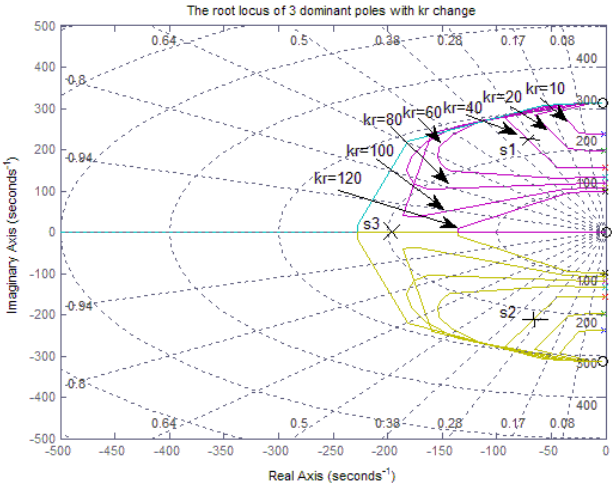

Fig. 11. The root locus of 3 dominant poles with k_r change.

According to Eq. (16) the parameter root locus of the whole system closed loop is derived, as shown in Eq. (17). It is to be noted that the meanings of M and N in Eq. (17) are the same as those in Eq. (15). When k_r=10, 20, 40, 60, 80, 100, 120, a group of root locus are derived, as shown in Fig.10. It is obvious that the system closed-loop transfer function is a 6 order system, with 6 poles, 4 finite zeros and 2 infinite zeros. There is a zero located at the origin, which is introduced by the virtual capacitor strategy. This proves the validity of the analysis in section II. In the 6 poles, there are 3 non-dominant poles whose real values are less than -10^3 and their distance from the imaginary axis is more than 5 times as far as that of the other 3 dominant closed-loop poles. As a result, their influence on the system can be ignored when compared with the other 3 dominant closed-loop poles.

A zoom in the group of root locus and the root locus of 3 dominant poles with k_r change is shown in Fig. 11. The 3 dominant closed-loop poles mainly affect the performance of the system, including 2 poles located symmetrically on both sides of the real axis while the other one is located on the real axis. In order to give a clear description, they are numbered as s1, s2, s3, respectively. First, according to Fig. 10, if k_p is too small, there will be poles on the right half plane of the root locus and the system is not stable. Second, the system performance is mainly determined by s1, s2 and s3. With the increase of k_r, s1 and s2 first move away from the imaginary axis, and then come close to the imaginary axis while s3 moves more and more far away from the imaginary axis. The system open loop gain at the fundamental frequency becomes larger and the steady state error becomes smaller. However, the bandwidth decreases, the overshoot becomes larger and the settling time becomes longer. After many simulation tests, it is concluded that in order to obtain a good system performance, the damping ratios of s1 and s2 should be about 0.2-0.4 and the real value of s3 should be about 2-4 times that of s1 and s2. k_r=40 is the final choice. Third, the root locus with k_r=40 is observed to investigate the effect that k_p has on the system performance. On the one hand, it is desired that the dominant poles be quite far from the imaginary axis to guarantee the stability of the system. On the other hand, it is better for the system to have underdamped oscillation to get a good dynamic performance. With the increase of k_p, s1 and s2 first move away from the imaginary axis, and then come close to the imaginary axis, while s3 comes close to the imaginary axis all the time. s1 and s2 are finally selected near the inflection point of the root locus, with k_p=0.75, s1,2=−67.1±j215, and s3=-197. The bandwidth of the system is 7401Hz (15.6Hz to 7416.6Hz). At this time, all the poles are in the left half plane of the root locus and the dynamic response has a slightly underdamped oscillation with a small overshoot and a short settling time. In addition, the attenuation of the high frequency harmonic is still quite strong.

C. Robustness Analysis

Inverters are connected to the grid. However, in a weak grid, the grid impedance change is relatively large, which usually requires an online inductance detection method and an adjustment of the control parameters [12], otherwise the system may become unstable or the THD of the grid current will become large. The control parameters designed in this paper are verified in the case of the grid impedance changes.

Assume that the grid impedance L_g=0, 0.5mH, 1mH and 2mH. Then, the root locus of the closed loop system is shown in Fig. 12 and Fig. 13. Fig. 12 is the root locus of 3 dominant closed poles with L_g change. The 3 dominant closed-loop poles (s1, s2, s3) change little with L_g change. e.g. s1,2=−67.1±j215, s3=-197 at L_g=0 and s1,2=−71.3±j190, s3=-198 at L_g=2mH. It is to be noted that the root locus at L_g=0.5mH and 1mH are so closed that only one label is made in Fig.12. Fig.13 is the root locus of all poles with L_g change. There are two closed loop poles which gradually come close to the imaginary axis with the increase of L_g. The bandwidth and phase margin of the system decrease. However, even when L_g=2mH, the two poles are at $-758 \pm j2.23 \times 10^4$, which can still be ignored when compared with the 3 dominant

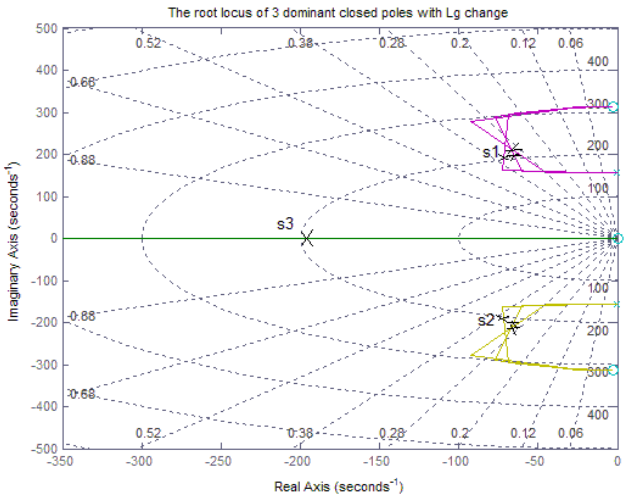

Fig. 12. The root locus of 3 dominant closed poles with L_g change.

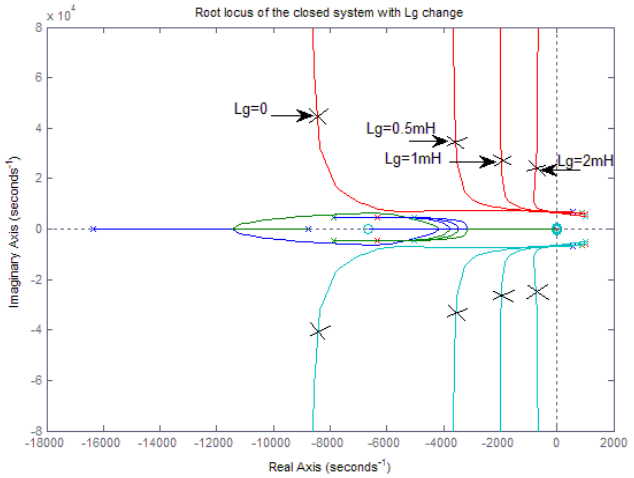

Fig. 13. The root locus of all poles with L_g change.

closed-loop poles. All the system closed-loop poles are on the left half plane of the root locus and the system performance is mainly determined by the 3 dominant closed-loop poles which change little as L_g ranges from 0 to 2mH. Therefore, the control parameters designed in this paper are robust in a certain range. This guarantees the stability of the system and eliminates the grid impedance detection device.

IV. Simulation and Experiment Results

A. Simulation Results

In this paper, the simulation is established based on MATLAB/Simulink. The simulation parameters are shown in Table I. The instruction current is $I_o^*(t) = 32.1\sin(\omega t) + 1(A)$. The unipolar modulation method is applied.

The simulation voltage waveform of virtual capacitor when the system starts is shown in Fig. 14. In the steady state, U_1=8.81V and U_2=-7.31V according to Fig. 14. It is obvious that $U_{c\_ave\_stable}$=0.75V and $U_{c\_pp\_stable}$=16.12V. In addition, when the virtual capacitor strategy is used, the results can be

TABLE I
Simulation Parameters

Parameter	Value	Parameter	Value
P_n	5kW	k_r	40
U_{dc}	380V	k_p	0.75
f_c	10kHz	L_1	2.5mH
U_g	220V/50Hz	L_2	0.5mH
C_0	33.32uF	C	15uF
ω_c	3	R_d	10Ω

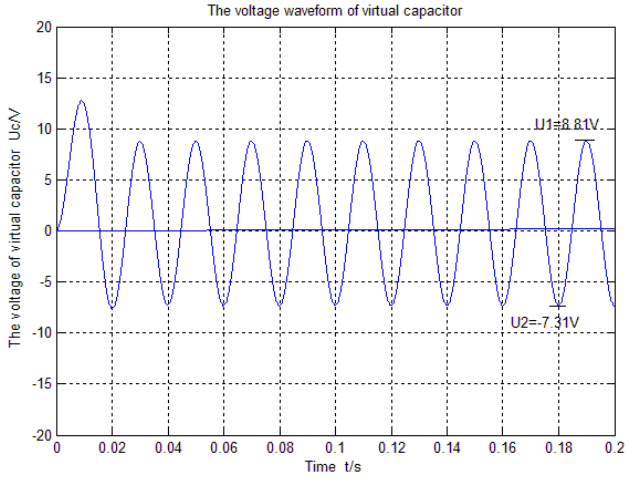

Fig. 14. The simulation voltage waveform of virtual capacitor.

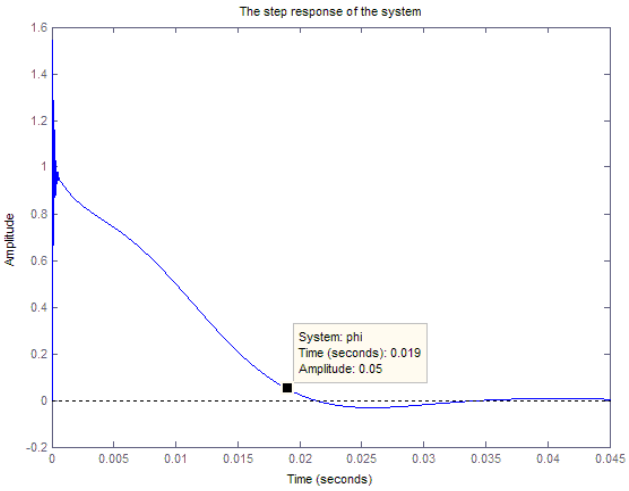

Fig.15. The step response of the system

derived from Eq. (8) and Eq. (9) divided by K_{PWM}. The analysis results are 0.75V and 16.14V and the simulation results verify the correctness of the analysis in section II.

Fig. 15 is the step response of the system. The dynamic response of the system in blocking DC component is so good that the settling time is 0.019s, which is about 1 grid cycle. The settling time is shorter than that achieved in reference [2] (0.05s). Fig. 16 is the simulation waveform of the grid voltage and grid current. According to Fig. 16, when the system starts, the grid current quickly tracks the fundamental

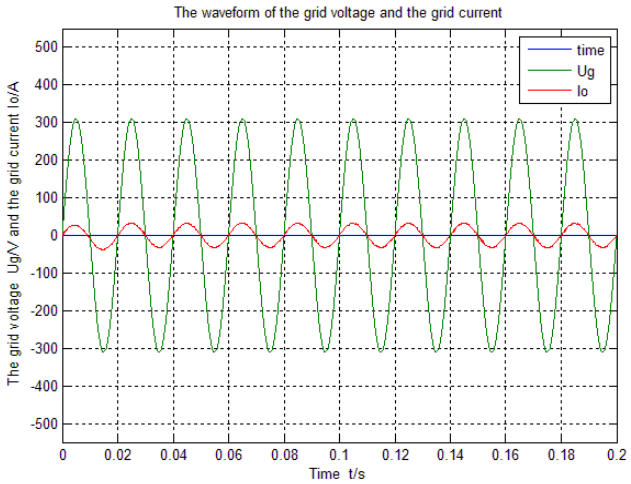

Fig. 16. The simulation waveform of grid voltage and grid current.

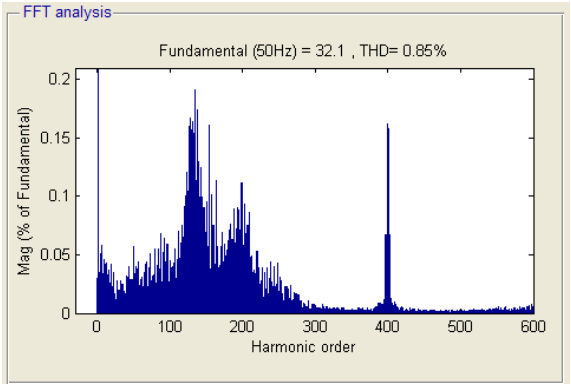

Fig. 17. The simulation FFT analysis of the grid current.

component of the instruction current and the DC component completely disappears at about 0.02s, which verifies the correctness of Fig. 15.

Fig. 17 is the simulation FFT analysis of the grid current (5 cycles, 0.1s-0.2s). According to Fig.17, the DC component disappears in the grid current, which verifies the effectiveness of the strategy. Of course, the attenuation of the switching frequency harmonics declines because of the damping resistor R_d. However, the 400-order harmonic is less than 0.2% and the THD is only 0.85%, which conforms to IEEE Std.929-2000.

B. Experimental Results

A 1-kW DSP-controlled grid-connected single-phase inverter was built to verify the proposed strategy based on virtual capacitor. The main circuit is shown in Fig.5 and the control parameters are shown in Table I. The instruction current is $I_o^*(t)$ =6sin (ωt)+0.2(A). 0.2A is used to represent the factors causing the DC component.

Fig. 18 is the waveform of the grid voltage and grid current without virtual capacitor. The waveforms of the grid voltage and grid current have almost the same frequency and phase, which is unity power factor operation. The conversion ratio of the current sensor is 2.5A/V and the Y-axis of the grid

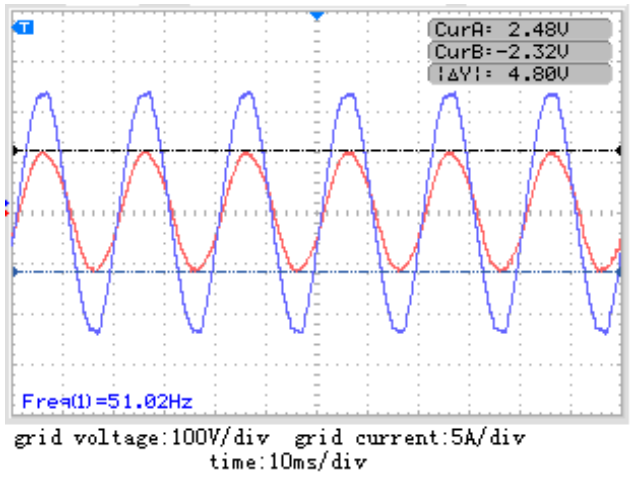

Fig. 18. The steady waveform of grid voltage and grid current without virtual capacitor.

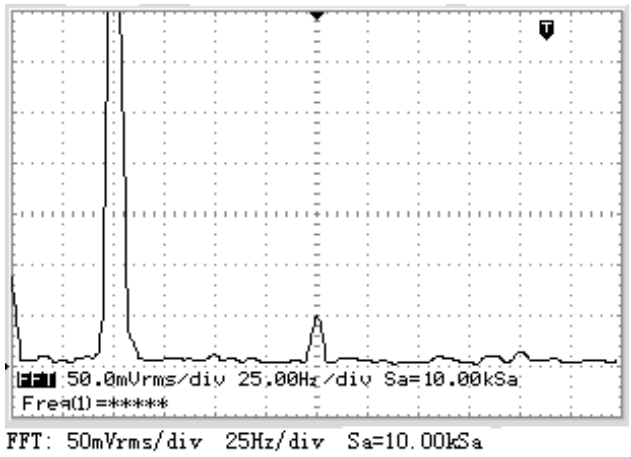

Fig. 19. The FFT analysis of the grid current without virtual capacitor.

current is 2V/div, namely 1div=2V=5A. The Y-axis of the grid voltage is 100V/div. The positive peak of the grid current is 2.48V, namely 6.2A, while the negative peak is at -2.32V, namely -5.8A. The DC component is about 0.08V, which represents 0.2A. Fig. 19 is the FFT analysis of the grid current without virtual capacitor. As can be seen from Fig.19, the DC component at 0Hz is about 86.1mVrms, which is close to the result in Fig. 18. It is to be noted, the grid current contains the 3-order harmonic, which significantly increases the THD, because the U_{dc} provided by renewable energy sources is not constant but contains double-frequency ripples.

Fig. 20 is the waveform of the grid voltage and grid current with virtual capacitor. The positive peak and negative peak are both 2.4V, which represents 6A. Fig. 21 is the FFT analysis of the grid current with virtual capacitor. The DC component at 0Hz is about 6.4mVrms, which is 0.016Arms. This means that the DC injection control based on virtual capacitor works effectively. The DC component is about 0.38% of the rated current, which conforms to IEEE Std.929-2000.

Fig. 22 is the waveform of the grid voltage and grid current

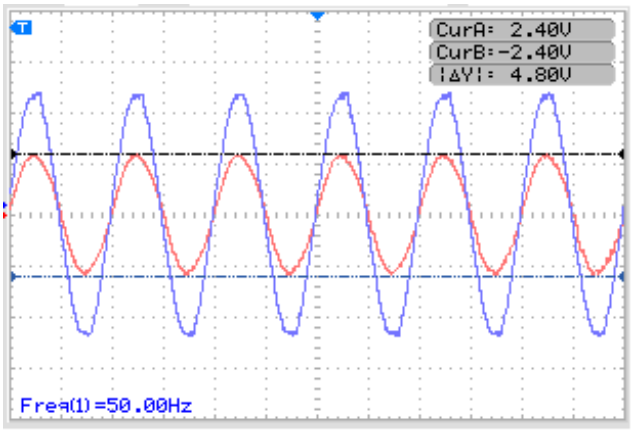

Fig. 20. The steady waveform of grid voltage and grid current with virtual capacitor.

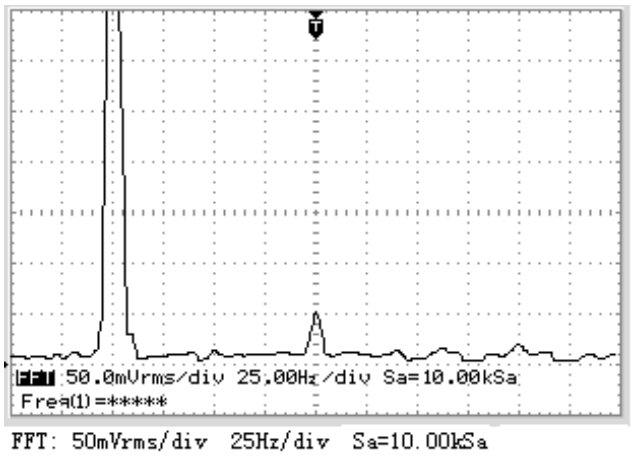

Fig. 21. The FFT analysis of grid current with virtual capacitor.

with L_g =2mH. As can be seen, in a weak grid, when L_g=2mH, the THD of the current increases and the stability decreases due to the reduction of the bandwidth and phase margin. However the parameters designed in this paper can guarantee the stability of the system which verifies the robustness of the control parameters.

Fig. 23 is the dynamic voltage waveform of virtual capacitor. The dynamic experiment condition is that the instruction current changes from $I_o^*(t)$ =6sin (ωt) to $I_o^*(t)$ =6sin (ωt) +0.2(A). The virtual capacitor voltage U_c, namely the numerical integration in the DSP register, is output by a DA (Digital to Analog) and it is shown in Fig. 23. Firstly, $I_o^*(t)$ =6sin (ωt), the virtual capacitor voltage does not contain DC component. When the dynamic process begins, namely $I_o^*(t)$ =6sin (ωt) +0.2(A), the virtual capacitor voltage contains DC component, which blocks the DC component in the instruction current. The dynamic response time is about 2 grid cycles, which is a little longer than the results shown in Fig. 15 and Fig. 16. It is due to the fact that in Fig. 15 and Fig. 16, U_{dc} is constant. However, in practical experiment, U_{dc} is not constant.

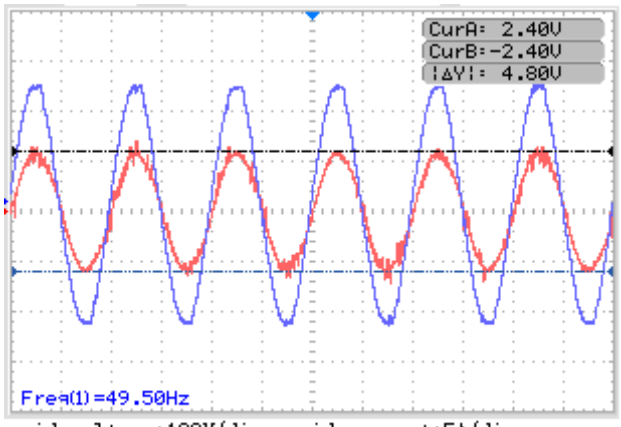

Fig. 22. The waveform of grid voltage and grid current with L_g=2mH.

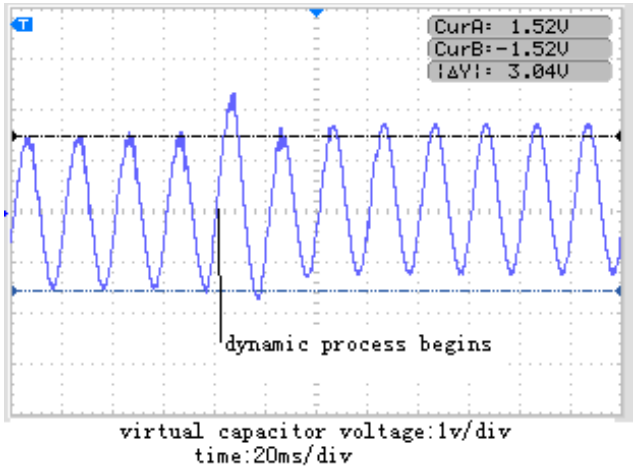

Fig. 23. The dynamic voltage waveform of virtual capacitor.

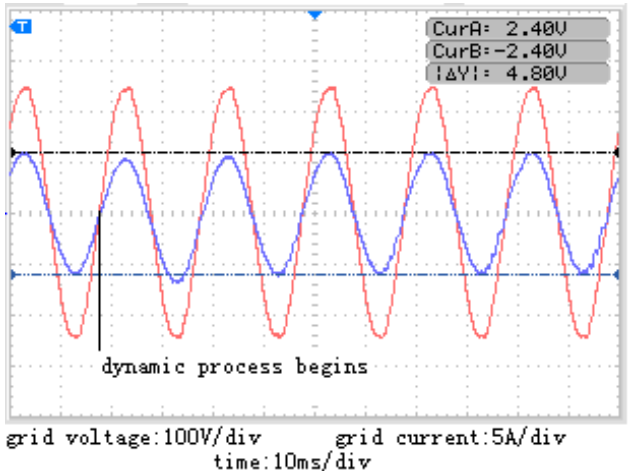

Fig. 24. The dynamic waveform of grid voltage and grid current with virtual capacitor.

Fig. 24 is the dynamic waveform of the grid voltage and grid current with virtual capacitor. The experiment condition is the same as that in Fig. 23. The dynamic response time is about 2 grid cycles. When the dynamic process ends, the DC component in the grid current disappears.

V. CONCLUSION

In this paper, DC injection control based on virtual capacitor is discussed, including the applicable conditions, working process and steady-state error. The proposed strategy has the advantages of low cost, low loss, high accuracy and simple implementation. The proposed strategy is applied in a single-phase grid-connected inverter with a LCL filter. The design of the control parameters is discussed in detail. The robustness of the control parameters is also discussed. The simulation and experimental results verify the validity of the analysis and show that this study has a certain value in engineering applications.

ACKNOWLEDGMENT

This work is supported by the Specialized Research Fund for the Doctoral Program of Higher Education of China (No. 20120032110070); The National Program of International S&T Cooperation (2013DFA11040); National Natural Science Foundation of China (61172014); Natural Science Foundation of Tianjin (12JCZDJC21300).

REFERENCES

[1] X.-Q. Guo, W.-Y. Wu, H.-R. Gu, and G.-C. San, "DC injection control for grid-connected inverters based on virtual capacitor concept," in *International Conference on Electrical Machines and System*, pp. 2327-2330, 2008.

[2] B.-C. Wang, X.-Q. Guo, Q. Mei, X.-F. Sun, and W.-Y. Wu, "DC injection control for transformerless PV grid-connected inverters," in *Proc. the Chinese Society for Electrical Engineering*, Vol. 29, No. 36, pp. 23-28, Dec. 2009.

[3] V. Salas, E. Olías, M. Alonso, F. Chenlo, and A. Barrado, "DC current injection into the network from PV grid inverter," in *Conference Record of the 2006 4th World Conference on Photovoltaic Energy Conversion,* pp. 2371-2374,2006.

[4] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, "Auto-Calibrating DC link current sensing technique for transformerless, grid connected, H-bridge inverter systems," *IEEE Trans. Power Electron.*, Vol. 21, No. 5, pp. 1385-1393, Sep. 2006.

[5] L. Zhou, B. Yang, K. Guo, H.-X. Li, and Z.-M. Zhang, "The progress and development trend of the DC injection issue in PV grid-connected systems," *Power System Protection and Control*, Vol. 40, No. 6, pp. 147-155, Mar. 2012.

[6] R. González, J. López, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 693-697, Mar. 2007.

[7] O. Lopez, R. Teodorescu, F. Freijedo, and J.D. Gandoy, "Leakage current evaluation of a single-phase transformerless PV inverter connected to the grid," in *Applied Power Electronics Conference*, pp. 907-912, 2007.

[8] R. Sharma, "Removal of DC offset current from transformerless PV inverters connected to utility," in *40th International Universities Power Engineering Conference*, pp. 1230-1234, 2005.

[9] L. Bowtell and A. Ahfock, "Direct current offset controller for transformerless single-phase photovoltaic grid-connected inverters," *IET Renewable Power Generation*, Vol. 4, No. 5, pp. 428-437, Sep. 2010.

[10] G. Buticchi, G. Franceschini, E. Lorenzani, C. Tassoni, and A. Bellini, "A novel current sensing DC offset compensation strategy in transformerless grid connected power converters," in *Energy Conversion Congress and Exposition*, pp. 3889-3894, 2009.

[11] G.-Q. Shen, X.-C. Zhu, J. Zhang, and D.-H. Xu, "A new feedback method for PR current control of LCL-filter-based grid-connected inverter," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, pp. 2033-2041, Jun. 2010.

[12] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp. 263-272, Jan. 2006.

Wei Wang was born in Anhui, China. He received his B.S. degree in Electrical Engineering from Anhui University, Hefei, China, in 2012, and his M.S. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2015. His current research interests include photovoltaic grid-connected power conditioning system and the effects of digital control on grid-connected inverters.

Ping Wang was born in Tianjin, China, in 1959. She received her B.S., M.S. and Ph.D. degrees in Electrical Engineering from Tianjin University, Tianjin, China, in 1981, 1991 and 2005, respectively. Since 1981, she has been working as a teacher and researcher in Tianjin University. Her current research interests include power electronic control of renewable energy sources, PWM converters, and intelligent detection and control.

Taizhou Bei was born in Shandong Province, China, in 1984. He received his B.S. degree in Automation from the Liaoning University of Technology, Jinzhou, China, in 2008, and his M.S. degree in Control theory and Control Engineering from Xinjiang University, Urumqi, China, in 2012. He is presently working toward his Ph.D. degree in Electrical Engineering at Tianjin University, Tianjin, China. His current research interests include power electronic control of renewable energy sources, power conversion circuits and photovoltaic systems.

Mengmeng Cai was born in Hunan, China. She received her B.S. degree in Electrical Engineering from Hunan University, Changsha, China, in 2012, and her M.S. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2015. Her current research interests include photovoltaic grid-connected inverters and LCL filters.