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An Improved SVPWM Control of Voltage Imbalance in Capacitors of a Single-Phase Multilevel Inverter

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Abstract

This paper presents a modified Space Vector Pulse Width Modulation Technique (SVPWM), which solves the well-known problem of voltage imbalance in the capacitors of a single-phase multilevel inverter. The proposed solution is based on the measurement of DC voltage levels at each capacitor of the inverter DC bus. The measurements are then used to adjust the size of the active vectors within the SVPWM algorithm to keep the voltage waveform sinusoidal regardless of any voltage imbalance on the DC link capacitors. When a voltage deviation exceeds a predetermined hysteresis band, the correspondent voltage vector is restricted to restore the voltage level to an acceptable threshold. Hence, the need for external voltage regulators for the voltage capacitors is eliminated. The functionality of the proposed algorithm is successfully demonstrated through simulations and experiments on a grid tied application.

Key words: Capacitor Voltage Balancing, Multilevel Inverter, Single-phase inverter, Space Vector Modulation

I. INTRODUCTION

Multilevel inverter topologies have been considered as a viable solution for applications where the quality of the voltage waveform is a critical parameter [1]. These devices are based on the implementation of a larger number of switching devices to deliver the AC voltage waveform in small discrete steps [2]. These voltage steps are then used to construct a staircase waveform with a reduced Total Harmonic Distortion (THD) among other important advantages, such as a nearly sinusoidal output, a lower output filter is required, reduced current ripple, reduced dv/dt stress on the switching devices, and an important reduction of Electromagnetic Interference (EMI) [1]-[8].

Various multilevel inverter topologies have been proposed. Among them are the diode-clamped inverter, the flying capacitor inverter, and the cascaded H-bridge with multiple DC sources, which all stand as the most important topologies [4], [5], [9], [10].

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These topologies present an increased number of switching devices, separate gate drivers, DC capacitors, and/or separate DC sources [11]. They also need additional components that mean increased cost and complexity of the power converter.

Moreover, the aforementioned advantages of the multilevel inverters are heavily dependent on the voltages of the series-connected DC bus capacitors [12], [13]. Non-uniform voltages on the DC capacitors will translate to a distorted AC waveform, or in case of total capacitor depletion, may lead to the loss of a complete voltage level [14]. To overcome this problem, most multilevel inverters rely on isolated DC sources and/or complex voltage balancing circuits. Some multilevel inverters allow the use of complex modulation techniques that give the system capacitor voltage control, thus the system is kept without added components [13].

A seven-level single-phase inverter topology was proposed and developed in [4], based on a conventional H-bridge structure and two bidirectional switches composed by an Insulated Gate Bipolar Transistor (IGBT) and a high-speed diode rectifier. This inverter topology has the additional advantage of requiring a reduced number of components when compared with other multilevel inverters. Hence, it represents an important advantage on reliability and cost reduction. However, the reduced number of components of

the seven-level inverter analyzed on this document implies a lack of redundant states. Thus, the usage of the inverter along with a redundant voltage selector for the balancing the DC bus is not a feasible solution.

Several Pulse Width Modulation (PWM) techniques exist today; among them are the Selective Harmonic Elimination PWM (SHEPWM) and the Sinusoidal PWM (SPWM) techniques [11], [13], [15]. These techniques have been the subject of intensive research. SPWM remains a widespread technique because it is easy to implement and may be adapted to multilevel inverter topologies with little effort. SPWM is commonly implemented in multilevel inverters using the multicarrier principle, and has been successfully used in this multilevel topology [4]. SPWM is based on the comparison of the desired voltage waveform with multiple carrier signals. Each carrier corresponds to a specific DC voltage level. The voltages and positions of each level are represented by the amplitude and DC offset of its corresponding carrier signal, respectively. If the DC voltages deviate from their nominal values, the carrier positions will no longer be valid and the resultant AC signal will become distorted. The SPWM lacks the ability to adjust the voltage deviations in the DC link capacitors to keep a sinusoidal waveform because the carrier amplitude and offset may not be easily adjusted in real time accordingly to the instantaneous DC voltages.

In recent years, advanced PWM techniques such as the Space Vector PWM (SVPWM) have appeared**.** SVPWM is a computer intensive algorithm that offers important advantages such as a low harmonic profile, higher DC bus utilization, and a wide linear operation region. It can also be easily adapted to different inverter topologies and control strategies [16]-[18].

In this paper, an improved SVPWM algorithm with a voltage balancing algorithm and waveform compensation for a multilevel grid-connecter single-phase inverter is presented. The space vector representation of the AC voltage levels allows considering the actual values of DC voltages during the synthesizing of the AC waveform. Thus, keeping a sinusoidal voltage under deviated DC voltages is possible. Moreover, the space vector approach makes it feasible to compensate for the elimination of a particular voltage level as its equivalent voltage may be synthesized using its consecutive levels. If the aforementioned SVPWM advantages are considered, balancing the capacitor voltages by the temporal elimination of certain voltage levels is possible.

SVPWM is based on the measurement of the DC voltage levels of the inverter; such measurements are then used to adjust the size of the active vectors used on the SVPWM algorithm to keep the voltage waveform sinusoidal regardless of any voltage imbalance in the capacitors of the inverter DC supply. When a voltage deviation is considered excessive on a given capacitor, the corresponding voltage vector is restricted to restore the voltage level into an acceptable threshold. Thus,

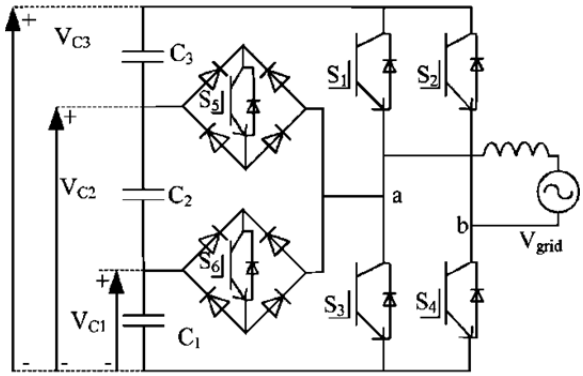

Fig. 1. Single-phase multilevel inverter.

the need for external voltage regulators is eliminated. To demonstrate the validity of the algorithm, the system is simulated and experimentally tested in both open loop and in a grid-connected application. Synchronization to the grid is achieved by means of a based Phase Locked Loop (PLL), which is a popular alternative for grid phase estimation [19]-[21]. The Park PLL is used to generate the signals necessary to drive the reference frame transformations needed for the Voltage Oriented Control (VOC), which is used to regulate the grid current. The voltage command generated by the VOC is then used to drive the proposed capacitor voltage balancing SVPWM algorithm.

II. SVPWM WITH CONTROL CAPACITOR VOLTAGE BALANCING AND COMPENSATED WAVEFORM

The multilevel inverter topology used in this work is depicted in Fig. 1, and is composed of a conventional H bridge and a number of bidirectional switches connected to the capacitor voltage divider. This inverter topology was selected because of its reduced number of switches and capacitors when compared with other multilevel topologies. Thus, it represents a good starting point when a low cost system is needed. The seven-voltage level synthesized by the inverter may be arranged in a one dimensional space vector, as presented in Fig. 2. The magnitudes of the active voltages in terms of voltage levels are given in Table 1. Six of them are active states while the center of the space vector arrangement corresponds to a null value where the two load terminals are tied to the same potential point.

The instantaneous voltage output of the inverter is determined by a command vector (**V**). This vector oscillates between the six operating regions at the same frequency of the desired voltage waveform at the inverter output. The peak value of the output voltage is determined by the maximum value of the command vector during these oscillations (V_{peak}). Whenever the command vector lies between two state vectors, a vector sum is carried out to obtain the desired voltage. This sum is given by (1):

$$V = k_H V_H + k_L V_L \quad (1)$$

where V_H and V_L are the higher and lower consecutive state vectors, respectively, and k_H and k_L are the coefficients of the linear combination used to synthesize *V*. These coefficients represent the percentage of the modulation period assigned to each active voltage. Hence, the magnitudes of k_H and k_L can be related by (2):

$$k_H + k_L = 1 \quad (2)$$

By solving for k_H and k_L using (1) and (2), obtaining k_H and k_L in terms of **V**, V_H, and V_L is possible. Thus, (3) is obtained:

$$\left.\begin{aligned} k_H &= \frac{V - V_L}{V_H - V_L} \\ k_L &= 1 - k_H \end{aligned}\right\} \quad (3)$$

In an ideal converter, the capacitor voltages are balanced and their individual voltages are fixed to one third of the DC bus; creating levels at 0, $1/3V_{cc}$, $2/3V_{cc}$, V_{cc}, and their negative counterparts [4]. Therefore, (3) could be simplified as (4):

$$\left.\begin{aligned} k_L &= 3(V_H - V) \\ k_H &= 3(V - V_L) \end{aligned}\right\} \quad (4)$$

Nevertheless, on a real inverter, the current drawn from every capacitor is not the same. Thus, the voltage on the nodes of the capacitor divider becomes asymmetrical. Therefore, the length of the different sectors on the space vector becomes variable, creating a distorted signal at the output of the inverter. To keep the voltage output as sinusoidal as possible, the actual voltages measured from the capacitive voltage divider are used to calculate the duty cycles for the different sectors. The magnitudes used as V_H and V_L along with the switching devices associated to those voltages are presented in Table II. Once the voltage components are calculated, they are transformed into the commutation times required to drive the inverter. Conversion from voltages to commutation times is achieved by multiplying the constants by the commutation period of the inverter; this yields Eqn. (5):

$$\left.\begin{aligned} T_H &= k_H T \\ T_L &= k_L T = 1 - T_H \end{aligned}\right\} \quad (5)$$

where T is the period of the commutation frequency, and T_H and T_L are the amounts of time during the commutation period where the high and low voltages are applied to the load, respectively. The modulation index (M) for this particular SVPWM is given by (6):

$$M = \frac{V_{peak}}{V_{cc}} \quad (6)$$

where V_{cc} is the total DC bus voltage. When *M* is smaller than the magnitude of Sectors 1 and 4 (V_{C1} and $-V_{c3}+V_{C2}$, respectively), the synthesized voltage waveform will be composed of two voltage levels, as a normal inverter would do. As *M* increases, more levels are added to the waveform.

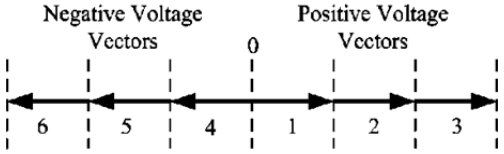

Fig. 2. Space vector arrangement.

When *M* becomes greater than 1, the inverter enters the over modulation region and the voltage output is fixed to its maximum voltage output (V_{cc} and $-V_{cc}$) as the inverter approaches the square mode operation.

A. Capacitor Voltage Balancing

As the inverter is operating, the differences on the current demands over the DC voltage levels create an unbalance on the voltage level of the DC capacitors. Moreover, if that situation is left unattended, it may end up depleting the charge on any of the capacitor voltages.

Thus, two levels from the AC waveform per each depleted capacitor are effectively eliminated. To overcome the aforementioned issue, a hysteresis based Sector Elimination (SE) charge and discharge control is implemented within the SVPWM. Such an algorithm actively regulates the voltages of C_2 and C_1, as C_3 will consequently be kept in its voltage level. The measured capacitor voltages V_{C2} and V_{C1} are referenced with respect to the DC bus voltage (V_{C3}). Afterward, they are compared against their desired voltage ($1/3\ V_{cc}$).

When the measured voltage of the capacitor is considered deviated beyond a predetermined threshold, one of the vectors is eliminated until the capacitor voltage reaches an acceptable voltage. When a capacitor voltage is found below its desired value, its corresponding voltage sector is removed from the modulation, as it is the moment when charge is taken from the capacitors' node. By contrast, if a capacitor voltage increases over its desired value, its negative voltage sector will be removed to allow the capacitor to discharge until it reaches a more desirable value. The Hysteresis Band (HB) may be adjusted by the user accordingly to the rate of charge and discharge of the capacitors because the capacitor voltage deviation is highly load dependent. Capacitor charge statuses, along with their correspondent sector removal, are shown in Table III.

III. SIMULATION ANALYSIS

The proposed modulation technique was first evaluated using simulation analysis in MATLAB/Simulink. The system was simulated as part of a grid tied inverter. The block diagram of the control structure is presented in Fig. 3. The current delivered to the electric grid is controlled using the Fictive Axis Emulation (FAE) based Voltage Oriented Control (VOC) as it stands out because of its low THD current, low sensitivity to frequency variations, compatibility with

TABLE I
VOLTAGE MAGNITUDES

Output Vector	Vector Magnitude	Switching Devices
0	0	S3 and S4 or S1 and S2
1	V_{C1}	S6 and S4
2	V_{C2}	S5 and S4
3	$V_{C3} = V_{CC}$	S1 and S4
4	$-V_{C3}+V_{C2}$	S2 and S5
5	$-V_{C3}+V_{C1}$	S2 and S6
5	$-V_{C3}$	S2 and S3

TABLE II
VOLTAGE MAGNITUDES

Neighboring Vectors	V_H	V_L
1 and 0	V_{C1}	0
2 and 1	V_{C2}	V_{C1}
3 and 2	V_{CC}	V_{C2}
4 and 0	0	$-V_{C3}+V_{C2}$
5 and 4	$-V_{C3}+V_{C2}$	$-V_{C3}+V_{C1}$
6 and 5	$-V_{C3}+V_{C1}$	$-V_{C3}$
1 and 0	V_{C1}	0

TABLE III
VECTOR ELIMINATION ACCORDING WITH CAPACITOR CHARGE

Capacitor Status	Vector Removed from SVPWM
C1 low	1
C1 high	2
C2 low	5
C2 high	4

advanced modulation techniques, and capability for a decoupled active and reactive power control [22]. The FAE VOC is based on the generation of a fictive current waveform (I_β) that is orthogonal to the grid current (I_α). Both signals are used to emulate the fixed reference frame of a three-phase system. The current, I_β, is synthesized by applying the difference between a fictive orthogonal voltage signal generated by the PLL ($V_{mag}\sin(\Theta)$) and the voltage reference, V_β, from the synchronous generator into the current transfer function of the low pass filter ($F_g(s)$) as expressed by (7):

$$I_\beta = \left(V_\beta - V_{mag} sin(\theta)\right) F_g(s) \quad (7)$$

The grid voltage measurement drives the PLL as it generates the $V_{mag}\sin(\Theta)$ signal used for synthesizing the current component I_β, and the $\sin(\theta)$ and $\cos(\theta)$ signals are used in the reference frame transformations.

Afterward, the current components are transformed into the synchronous frame. Thus, they become DC values that can be easily controlled with PI controllers. In the synchronous frame, the AC current is split into I_d and I_q components. I_d and I_q determine reactive and active powers, respectively. Therefore, the power components can be controlled independently. The unity power factor condition is met when the line current vector becomes aligned with the q axis.

Once the V_d and V_q voltage commands have been obtained, they are used to calculate the V_α, and V_β voltage commands. Voltage V_α drives the modulation algorithm while V_β is used for the generation of the orthogonal current component.

The parameters of the simulated system are: DC link capacitors of 3300 μF, line inductor of 8 mH, inductor resistance 0.8 Ω, and a commutation frequency of 6 kHz. The current command was set to a magnitude of 4 A on the direct axis. The waveform of the current delivered to the grid is presented in Fig. 4, where a quasi-sinusoidal waveform may be observed.

The synthesized waveform of the inverter is shown in Fig. 5, where the elimination of voltage Vector 2 may be appreciated; nevertheless, the current waveform remains unchanged.

The elimination of voltage sectors is done accordingly to the voltages of the DC capacitors and rules shown in Table III. When voltage V_{C2} decreases beyond the hysteresis threshold, Sector 2 is eliminated to allow the recharging the capacitor and is used again when the voltage level of C_2 is restored. The voltages of the DC link capacitors are shown in Fig. 6. These voltages are not fixed to 1/3 and $2/3V_{cc}$ conversely, and remain oscillating around this voltage level. The amplitude of these oscillations is equal to the controller HB. However, because the SVPWM algorithm considers these variations, the current waveform is kept sinusoidal while the DC voltages fluctuate within the pre-established levels. This allows the system to effectively keep its multilevel capacity.

The grid side inductor represents a coupling between the inverter and the grid while eliminating the high frequency components of the PWM modulation. Thus, a sinusoidal current waveform is achieved as the inductance is increased, and the ripple of the current is decreased. Nonetheless, the impedance between the inverter and the grid is also increased and the current flow is limited. The design rule used, which considers the maximum value of the AC side inductor, is derived by the analysis presented in [23], [24] (8):

$$L < \frac{V_{dc} - \sqrt{2}\, V_{AC\,rms}}{\omega_{grid}\, I_{ld}} \quad (8)$$

where V_{dc} is the DC bus voltage, V_{ACrms} is the grid side voltage, ω_{grid} is the angular frequency of the grid voltage, and I_{ld} is the desired current.

During the elimination of a voltage sector, the current ripple is expected to increase. The system was evaluated using 2, 6, 8, and 12 mH AC inductors. THD (with 150 harmonics) increased by approximately 1% when a voltage sector was removed. This indicates that continuing the use of the same inductor without a detriment to the system performance is possible.

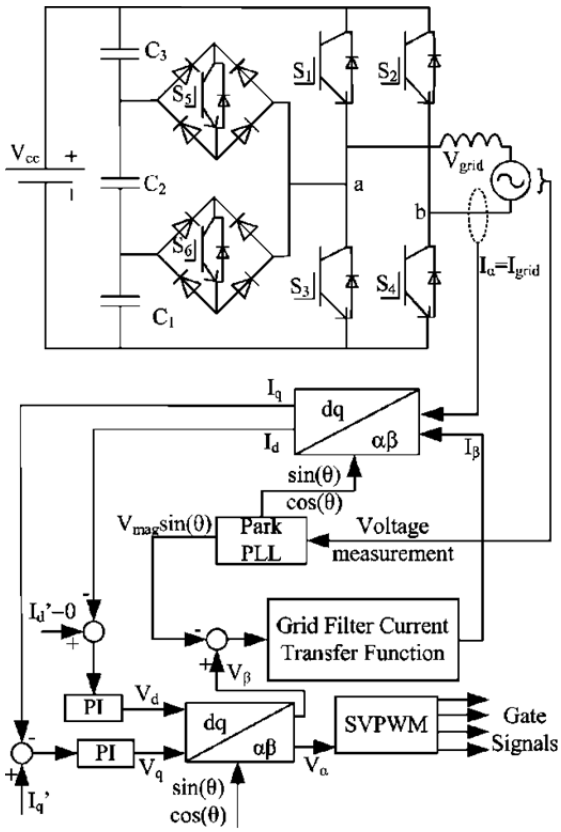

Fig. 3. Single-phase multilevel inverter and VOC algorithm.

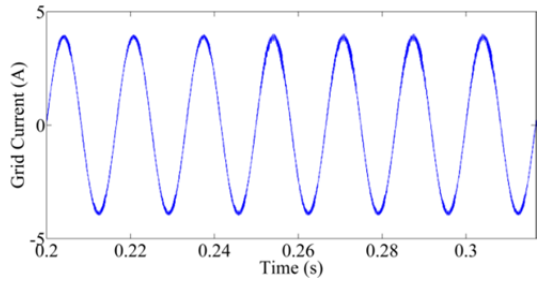

Fig. 4. Simulated grid current multilevel waveform.

IV. Comparison with Other Balancing Methodologies

There are different approaches when it comes to the voltage balancing of the DC capacitors on multilevel inverters. Some of these methodologies are highly dependent on inverter hardware topology. The proposed algorithm in this paper is compared through simulation analysis with other common balancing techniques that are compatible with the aforementioned multilevel topology, such as the employment of Independent Voltage Sources (IVS), a Resonant Converter (RC) stabilizer, usage of passive elements, and the proposed SE algorithm.

The implementation of IVS for the generation of the voltages used by the inverter is a commonly used solution. Although this is a highly effective approach, it increases the

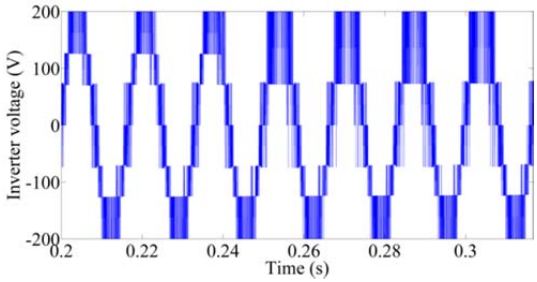

Fig. 5. Simulated multilevel inverter voltage waveform.

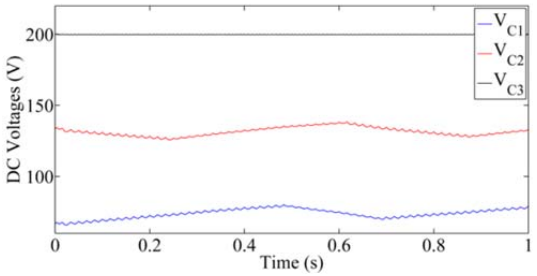

Fig. 6. Simulated DC bus voltages.

complexity and cost of the overall system. This approach was evaluated using the full-bridge DC-DC converter, which is a well-known topology and is suitable for medium to large power applications. It has an isolated output and undergoes switching devices to lessen electric stress. The switching frequency of the full-bridge converter is set to 20 kHz.

An alternative for balancing the DC voltages is the usage of an equalization network. Such a network may be comprised by active and/or passive elements. Passive equalization networks usually consist of an arrangement of series resistors connected to the DC capacitors, which is a simple and straightforward solution. Nevertheless, it implies power losses, as the value of the resistors must be kept small enough for the capacitor voltages to remain balanced. An active equalization network composed of an LC represents a suitable alternative for maintaining CD voltages without the need for bulky inductors [25]. Such an approach may be easily adapted for the proposed topology by arranging the capacitor and the LC resonant circuits in a similar way as if they were part of a three-phase inverter (Fig. 7). The circuit is made of three half bridges and the resonant elements Lr and Cr. The terminals of the half bridges are connected to the capacitors of the DC bus. Any imbalance on the DC voltages will affect the power flow through the LC circuit, thus restoring voltage balance to the DC capacitors. The switching frequency of the devices must be larger than the LC resonant frequency. Hence, the resonant will behave as an inductive element [26]. The passive elements C_r and L_r used on the simulation analysis are 10 μf and 10 μH, respectively, while the balancing half-bridges are switched at 30 kHz.

Even though there are other alternatives available, they were not considered, as the hardware topology of the inverter may not be compatible with them. Other solutions would

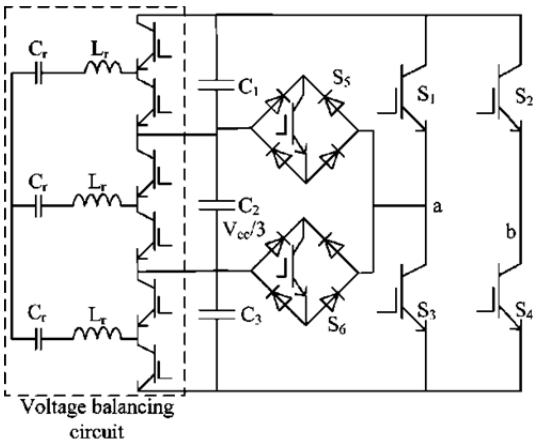

Fig. 7. Multilevel inverter equipped with a resonant converter voltage equalizer.

TABLE IV
DC VOLTAGE EQUALIZATION TECHNIQUES COMPARISON

Balancing Technique	DC Voltage Deviation	External Elements	Current THD
RC	5%	6 IGBTS, 3 LC Circuits	1.8%
IVS	0%	3 Voltage Sources	0.29%
SE	+/- HB (10%)	None	0.25%

imply a decreased quality of the inverter synthesized voltage waveform. The aforementioned methodologies are compared with the proposed technique through the simulation analysis of a grid tied converter. The DC voltage of one of the inverter capacitors is presented in Fig. 8. The DC voltage is kept at the desired value when an IVS is employed, while the RC keeps the voltage waveform within a fixed 5% deviation from the set point. The proposed SE methodology keeps the voltage oscillating around the desired value.

The amplitude of these oscillations may be controlled by adjusting the HB used on the SE regulator. Nonetheless, as the SVPWM is designed to consider the actual magnitude of the DC voltage levels, the harmonic distortion of the current delivered to the grid is kept to a minimum, as shown in Table IV. Thus, a reliable system that keeps the current THD to a minimum and fixes the DC voltages within the acceptable levels is achieved without the need for external converters that increase overall system cost and complexity while diminishing power efficiency.

V. EXPERIMENTAL EVALUATION

The experimental implementation of the proposed SVPWM algorithm was implemented in a 40 MIPS dsPIC33FJ128MC802 DSC. The capacitor and grid voltages were measured using HPCL7800 isolation amplifiers and the grid current was measured using a CSLA2CD Hall effect current sensor. The power stage is composed of IRGB4064DPbF IGBTs and high-speed

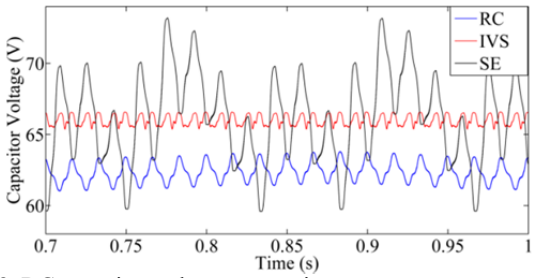

Fig. 8. DC capacitor voltage comparison.

FES16JT diodes. IGBTs were driven using single IR2121 and IR2127 gate drivers. These devices were selected because of the flexibility offered by the individual management of each IGBT.

A. Open Loop Experimental Comparison

The SVPWM algorithm was first evaluated against the sinusoidal modulation technique without any current controller. This test was done with and without the balancing block of the SVPWM to evaluate the capacity of the SVPWM to operate under unbalanced voltage conditions independent of the current controller used with the algorithm. Both systems were tested using a 95% modulation index and a RL resistive load.

The THD current for the SVPWM with capacitor voltage balancing is shown in Fig. 9, while the SVPWM without the voltage balancing SE block and the sinusoidal algorithms current THD are portrayed in Figs. 10 and 11, respectively. The SVPWM algorithm presents a much better current response, as it is not affected by the problem of the voltage-balancing present in the conventional sinusoidal modulation.

B. Closed Loop Experimental Comparison

This section presents the implementation of the proposed SVPWM algorithm on a vector-controlled single-phase grid-connected multilevel inverter. The parameters of the experimental setup are given in Table V. The experiment is depicted in Fig. 12. The DC link voltages along with the grid side voltage and current were sampled at a frequency of 6 kHz. Grid voltage is employed to drive the Park PLL. The estimated angle obtained from the PLL is used to generate the necessary signals to drive the reference frame transformations (sinθ and cosθ). The measured current is fed to the reference Park transformation to generate the I_d and I_q current components. Afterward, these signals are delivered to the current controller, where the SVPWM command voltage is generated. Then, the SVPWM algorithm sends the signals to the driver where they are properly conditioned and sent to the VSI IGBT gates. The experimental I_{dq} current components and the grid current are portrayed in Figs. 13 and 14. These

Fig. 9. SVPWM experimental THD current obtained the capacitor voltage-balancing algorithm.

Fig. 10. SVPWM experimental THD current without the capacitor voltage algorithm.

Fig. 11. SPWM experimental current THD.

TABLE V
EXPERIMENTAL SYSTEM PARAMETERS

Symbol	Parameter	Magnitude
C	DC Level capacitor	3300 uF
L	Filter inductance	8 mH
R	Filter resistance	0.8 Ω
N	Transformer ratio	5 (120 V/24 V)
V_{cc}	DC bus voltage	60 V
F	Grid frequency	60 Hz
F_c	Commutation frequency	6 kHz
F_s	Sampling rate	6 kHz
d_t	Commutation dead time	2 uS

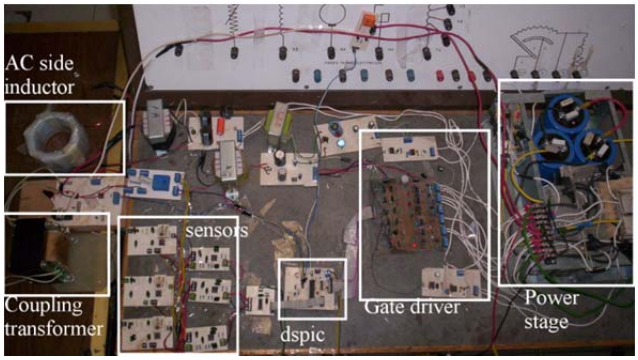

Fig. 12. Experimental setup that shows the AC side inductor, sensors, coupling transformer, drivers, controller, and power stage.

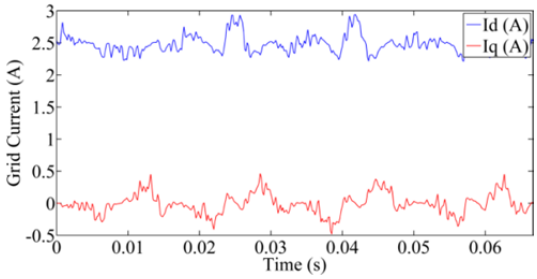

Fig. 13. Experimental I_d and I_q currents.

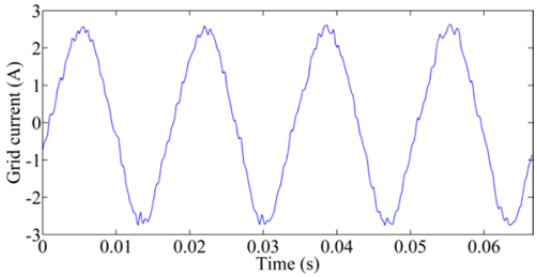

Fig. 14. Experimental current waveform.

Fig. 15. Experimental closed loop current THD.

waveforms were obtained from the DSC memory using the data monitor control interface [27].

The delivered current presents a quasi-sinusoidal waveform. The above is confirmed in Fig. 15, where a 2.3% THD is reported despite the temporary elimination of voltage vectors because of DC voltage leveling (Fig 15). The experimental

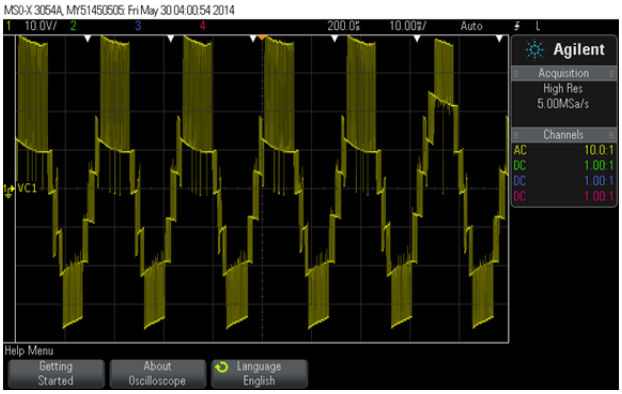

Fig. 16. Experimental inverter voltage (10 V/div, 10 ms/div).

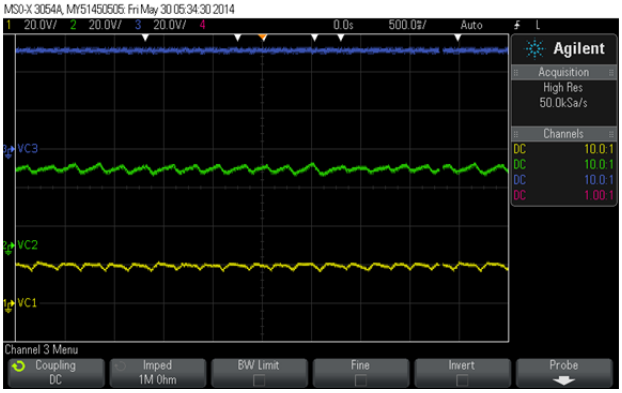

Fig. 17. Experimental DC bus voltages (20 V/div 500 ms/div).

DC voltages are depicted in Fig. 16, where the regulation of the capacitors may be observed as the voltage oscillates around the desired value.

VI. CONCLUSION

The design, simulation, and development of an improved SVPWM algorithm with capacitor voltage balancing and AC voltage asymmetry compensation for a single-phase seven-level inverter have been presented in this paper. The proposed SVPWM algorithm offers important advantages, such as a low harmonic profile under unbalanced conditions and the ability to keep the DC capacitor voltages within a desired threshold. The validity of the proposed SVPWM was demonstrated by a simulation analysis and through experiments. The current THD might be kept on a level comparable as when using IVS (<1%) without the need for additional components and DC sources. The aforementioned is achieved without compromising the quality of the synthesized waveform. The proposed SVPWM algorithm, the Park PLL, and the VOC control algorithm were programmed and successfully executed in a digital signal controller. The SVPWM algorithm has the capacity to compensate any asymmetry in the capacitor voltages, leading to a reduced THD when compared with the conventional sinusoidal modulation that is commonly used on multilevel topologies. Moreover, the proposed algorithm was tested experimentally alongside an advanced current control algorithm, such as the VOC, without reaching the DCS real-time calculation capacity. The system delivered a quasi-sinusoidal current waveform independent of the cancelation of some voltage vectors during the balancing of the capacitor voltages.

Finally, the proposed voltage SVPWM is a feasible solution for the control of the seven-level single-phase multilevel inverter with bidirectional switches, where the need for extra power converters or complex equalization networks is avoided.

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