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A ZVS Resonant Converter with Balanced Flying Capacitors

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Abstract

This paper presents a new resonant converter to achieve the soft switching of power devices. Two full-bridge converters are connected in series to clamp the voltage stress of power switches at $V_{in}/2$. Thus, power MOSFETs with a 500V voltage rating can be used for 800V input voltage applications. Two flying capacitors are connected on the AC side of the two full-bridge converters to automatically balance the two split input capacitor voltages in every switching cycle. Two resonant tanks are used in the proposed converter to share the load current and to reduce the current stress of the passive and active components. If the switching frequency is less than the series resonant frequency of the resonant tanks, the power MOSFETs can be turned on under zero voltage switching, and the rectifier diodes can be turned off under zero current switching. The switching losses on the power MOSFETs are reduced and the reverse recovery loss is improved. Experiments with a 1.5kW prototype are provided to demonstrate the performance of the proposed converter.

Key words: Resonant converter, Soft switching, Three-level converter

I. INTRODUCTION

Three-level converters or inverters have been proposed for high voltage applications such as high speed railway electrical systems [1], three-phase high power factor correction converters, ship electric power distribution systems [2], reactive power compensators [3]-[5] and AC motor systems [6]-[8]. Three-level converters/inverters [3]-[8] with a neutral-point diode clamp, a capacitor clamp or series H-bridge topologies have been proposed and developed to decrease the voltage stress of power devices and to increase the switching frequency. As a result, the size of the passive components can be decreased. For modern power converters, a compact size, high power density and high circuit efficiency are normally required. Thus, three-level converters [9]-[14] with zero voltage switching (ZVS) have been proposed to reduce the switching losses on power devices at a desired load range. Based on the resonant behavior due to the leakage inductance and resonant capacitance, the power switches can be turned on under ZVS during the transition interval. However, the ZVS range of power switches depends on the load power and input voltage conditions. Thus, it is very difficult to design a ZVS three-level converter with a wide range of load conditions. Recently, resonant converters [14]-[16] have received a lot of attention due to their essential advantages in terms of a high conversion efficiency and a wide ZVS range of the load condition. If the switching frequency is less than the series resonant frequency, the rectifier diodes at the secondary side are operated under zero current switching (ZCS) and the power switches are operated under ZVS turn-on. Thus, the reverse recovery losses of the diode rectifier are improved and the switching losses of the power switches are reduced. However, the voltage stress of the power switches in a conventional resonant converter is equal to the input voltage. In conventional three-level resonant converters [17], [18], the input split voltages cannot be balanced automatically in every switching cycle.

This paper presents a new resonant converter with the functions of a low voltage stress of the power switches, low switching losses and balanced input capacitor voltages in every switching cycle. Two full-bridge resonant converters are connected in series at the high voltage side to limit the voltage stress of the power switch at $V_{in}/2$. The secondary sides of the two full-bridge converters are connected in

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parallel to share the load current and to reduce the size of the active and passive components. In order to balance the two input capacitor voltages, two flying capacitors are connected between the AC sides of the two full-bridge converter legs. Thus, the input capacitor voltages can be automatically balanced in each switching cycle. Pulse frequency modulation is adopted to regulate the output voltage. The input impedance of the resonant converter is controlled as an inductive load at the switching frequency. Thus, the power switches can be turned on under ZVS with a wide range of load conditions. If the switching frequency is lower than the series resonant frequency, the rectifier diodes can be turned off under ZCS. The system analysis, circuit characteristics and a design example of the prototype circuit are discussed in detail. Finally, experiments are provided to demonstrate the performance of the proposed converter.

II. Proposed Converter

Fig. 1(a) shows a block diagram of a general two-stage AC/DC converter. The front stage is a three-phase power factor corrector (PFC) to achieve a high power factor and to obtain a stable DC bus voltage V_{in}. The second stage is a DC/DC converter to provide a stable output voltage against load current variations. Fig. 1(b) shows a circuit diagram of a conventional three-phase bidirectional PFC. In this circuit, energy can be transferred from an AC source to a DC load or from a DC load to an AC source. The output DC voltage V_{in} of a three-phase PFC is normally regulated at 750V-800V. Fig. 1(c) presents a circuit diagram of the proposed new DC/DC converter. Two full-bridge resonant converters are connected in series at the high voltage side to reduce the voltage stress of the power switches and to achieve high circuit efficiency due to ZVS turn-on for each power switch. The secondary sides of these two converters are connected in parallel in order to reduce the current stress of the passive and active components. In order to automatically balance the two input split capacitor voltages v_{Cin1} and v_{Cin2}, two flying capacitors C_{f1} and C_{f2} are connected at the AC terminal points (a, c) and (b, d). Thus, the two split capacitor voltages and the two flying voltages are automatically balanced, $v_{Cin1}=v_{Cin2}=v_{Cf1}=v_{Cf2}=V_{in}/2$, in a switching cycle. C_{in1} and C_{in2} are input split capacitances. S_1-S_8 are power MOSFETs. L_{r1} and L_{r2} are resonant inductances. C_{r1} and C_{r2} are resonant capacitances. C_1-C_8 are the output capacitances of S_1-S_8, respectively. D_1-D_4 are the rectifier diodes at the output side. L_{m1} and L_{m2} are the magnetizing inductances of the transformers T_1 and T_2, respectively. C_o is output capacitance. The first resonant converter includes C_{in1}, S_1-S_4, C_1-C_4, C_{r1}, L_{r1}, T_1, D_1, D_2 and C_o. The components of the second resonant converter are C_{in2}, S_5-S_8, C_5-C_8, C_{r2}, L_{r2}, T_2, D_3, D_4 and C_o. C_{f1} and C_{f2} are used to balance v_{Cin1} and v_{Cin2} in every switching cycle. The voltage stress of each power switch is clamped at

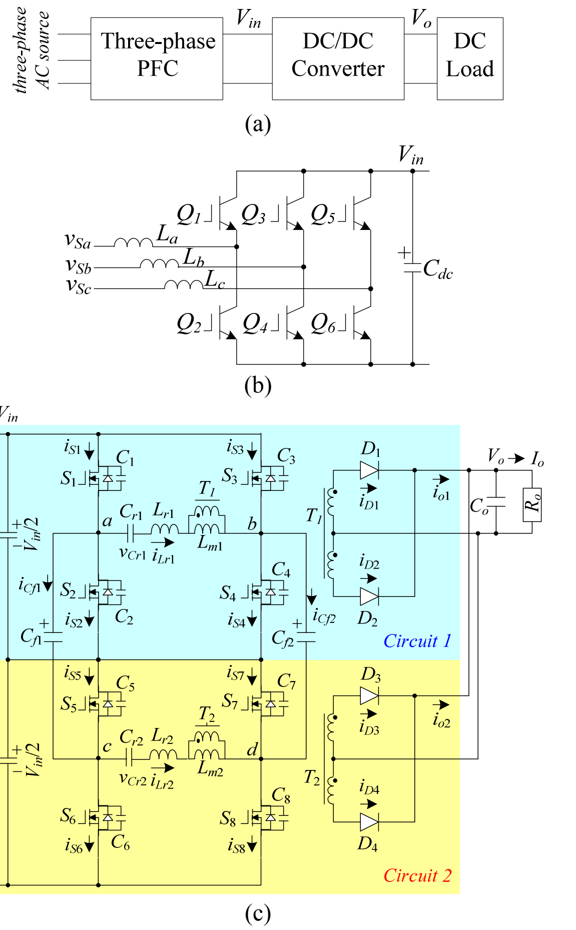


Fig. 1. Circuit diagram. (a) Two-stage AC/DC converter. (b) Front stage with a general three-phase PFC. (c) Proposed ZVS DC/DC converter with two full-bridge resonant circuits and two flying capacitors.

$V_{in}/2$. Therefore, MOSFETs with 500V or 600V of voltage stress can be used at the 800V input voltage condition. The pulse frequency modulation scheme is adopted to regulate the output voltage. If the switching frequency is less than the series resonant frequency at the full load and maximum input voltage case, the power switches S_1-S_8 are turned on at ZVS and the rectifier diodes D_1-D_4 are turned off at ZCS. Thus, the switching losses of the power switches are reduced and the reverse recovery losses of the rectifier diodes are improved.

III. Operation Principles

In this section, the system analysis and operation principle of the proposed converter are discussed assuming the following assumptions. 1) The transformers T_1 and T_2 have the same magnetizing inductances $L_{m1}=L_{m2}=L_m$ and turns ratios $n=n_p/n_{s1}=n_p/n_{s2}$, 2) S_1-S_8 are ideal and have the same output capacitances $C_1=\ldots=C_8=C_{oss}$, 3) the diodes D_1-D_4 are ideal, 4) the resonant inductances $L_{r1}=L_{r2}=L_r$, 5) the resonant capacitances $C_{r1}=C_{r2}=C_r$, 6) C_o is large enough that V_o is a constant voltage, 7) $V_{Cin1}=V_{Cin2}=V_{Cf1}=V_{Cf2}=V_{in}/2$, and 8)

$C_{in1}=C_{in2}$ and $C_{f1}=C_{f2}$. Pulse frequency modulation is adopted to change the input impedance of the proposed converter so that the output voltage is regulated at a desired voltage value against different input voltage and load conditions. Based on the on/off states of S_1-S_8 and D_1-D_4, six operating modes can be derived in a switching period. Fig. 2 shows the key PWM waveforms of the proposed converter. The duty cycle of S_1-S_8 is 0.5. S_1, S_4, S_5 and S_8 have the same PWM waveforms. In the same manner, S_2, S_3, S_6 and S_7 have the same PWM waveforms. However, the PWM waveforms of S_1 and S_2 are complementary each other. The equivalent circuits of each operation mode are shown in Fig. 3. Before time t_0, S_1-S_8, D_2 and D_4 are all in the off-state. The capacitors C_1, C_4, C_5 and C_8 are discharged, and C_2, C_3, C_6 and C_7 are charged.

Mode 1 [t_0 - t_1]: At t_0, C_1, C_4, C_5 and C_8 are discharged to zero voltage. Since i_{Lr1} and i_{Lr2} are both negative, the anti-parallel diodes of S_1, S_4, S_5 and S_8 are conducting. Therefore, S_1, S_4, S_5 and S_8 can be turned on at this moment to achieve ZVS. The flying capacitor voltages $v_{Cf1}=V_{Cin1}$ and $v_{Cf2}=v_{Cin2}$. The voltage stresses of S_2 and S_3 are equal to V_{Cin1}, and the voltage stresses of S_6 and S_7 are equal to V_{Cin2}. In resonant circuit 1, $i_{Lr1}>i_{Lm1}$ and the diode D_1 conducts. Thus, $v_{Lm1}=nV_o$ and i_{Lm1} is increasing in this mode. C_{r1} and L_{r1} are resonant with the initial voltage $V_{in}/2$-nV_o-$v_{Cr1}(t_0)$. Similarly, C_{r2} and L_{r2} are resonant with the initial voltage $V_{in}/2$-nV_o-$v_{Cr2}(t_0)$ in the second resonant circuit, and i_{Lm2} is also increasing. The input power is transferred to the output load through (S_1, L_{r1}, T_1, S_4, D_1) in resonant circuit 1 and (S_5, L_{r2}, T_2, S_8, D_3) resonant circuit 2. Thus, the resonant inductor currents and the capacitor voltages in this mode are expressed as:

$$i_{Lr1}(t)=\frac{V_{in}/2-nV_o-v_{Cr1}(t_0)}{Z_{r1}}\sin\omega_{r1}(t-t_0)+i_{Lr1}(t_0)\cos\omega_{r1}(t-t_0) \quad (1)$$

$$i_{Lr2}(t)=\frac{V_{in}/2-nV_o-v_{Cr2}(t_0)}{Z_{r1}}\sin\omega_{r1}(t-t_0)+i_{Lr2}(t_0)\cos\omega_{r1}(t-t_0) \quad (2)$$

$$v_{Cr1}(t)=V_{in}/2-nV_o-[V_{in}/2-nV_o-v_{Cr1}(t_0)]\times\cos\omega_{r1}(t-t_0)+i_{Lr1}(t_0)Z_{r1}\sin\omega_{r1}(t-t_0) \quad (3)$$

$$v_{Cr2}(t)=V_{in}/2-nV_o-[V_{in}/2-nV_o-v_{Cr2}(t_0)]\times\cos\omega_{r1}(t-t_0)+i_{Lr2}(t_0)Z_{r1}\sin\omega_{r1}(t-t_0) \quad (4)$$

where $Z_{r1}=\sqrt{L_r/C_r}$ and $\omega_{r1}=1/\sqrt{L_rC_r}$.

Mode 2 [t_1 - t_2]: At t_1, $i_{Lr1}=i_{Lm1}$ and $i_{Lr2}=i_{Lm2}$. Then, the diodes D_1-D_4 are off in this mode. Since S_1 and S_4 are still conducting, C_{r1}, L_{r1} and L_{m1} are resonant in resonant circuit 1. In the same manner, S_5 and S_8 are still conducting so that C_{r2}, L_{r2} and L_{m2} are resonant in resonant circuit 2. Thus, i_{Lr1}, i_{Lr2}, v_{Cr1} and v_{Cr2} are expressed as:

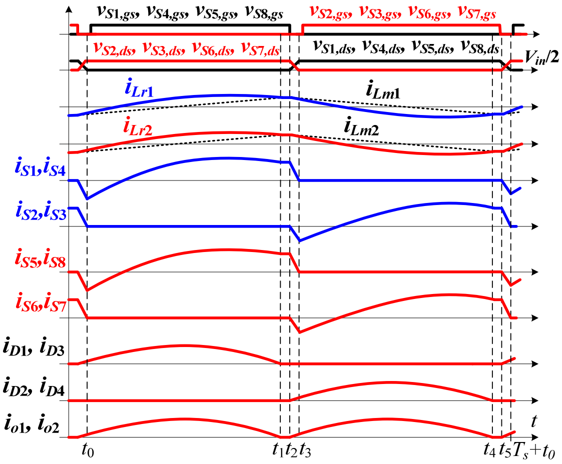


Fig. 2. Key waveforms of the proposed converter.

$$i_{Lr1}(t)=\frac{V_{in}/2-v_{Cr1}(t_1)}{Z_{r2}}\sin\omega_{r2}(t-t_1)+i_{Lr1}(t_1)\cos\omega_{r2}(t-t_1) \quad (5)$$

$$i_{Lr2}(t)=\frac{V_{in}/2-v_{Cr2}(t_1)}{Z_{r2}}\sin\omega_{r2}(t-t_1)+i_{Lr2}(t_1)\cos\omega_{r2}(t-t_1) \quad (6)$$

$$v_{Cr1}(t)=V_{in}/2-[V_{in}/2-v_{Cr1}(t_1)]\cos\omega_{r2}(t-t_1)+i_{Lr1}(t_1)Z_{r2}\sin\omega_{r2}(t-t_1) \quad (7)$$

$$v_{Cr2}(t)=V_{in}/2-[V_{in}/2-v_{Cr2}(t_1)]\cos\omega_{r2}(t-t_1)+i_{Lr2}(t_1)Z_{r2}\sin\omega_{r2}(t-t_1) \quad (8)$$

where $Z_{r2}=\sqrt{(L_r+L_m)/C_r}$ and $\omega_{r2}=\frac{1}{\sqrt{(L_r+L_m)C_r}}$.

Mode 3 [t_2 - t_3]: At t_2, S_1, S_4, S_5 and S_8 are turned off and the diodes D_2 and D_4 are conducting. Thus, $v_{Lm1}=v_{Lm2}=-nV_o$. The magnetizing currents i_{Lm1} and i_{Lm2} decrease with a slope of $-nV_o/L_m$. Since $i_{Lr1}(t_2)>0$ and $i_{Lr2}(t_2)>0$, C_1, C_4, C_5 and C_8 are charged and C_2, C_3, C_6 and C_7 are discharged.

$$v_{C1}(t)=v_{C4}(t)\approx\frac{i_{Lr1}(t_2)}{2C_{oss}}(t-t_2) \quad (9)$$

$$v_{C2}(t)=v_{C3}(t)\approx\frac{V_{in}}{2}-\frac{i_{Lr1}(t_2)}{2C_{oss}}(t-t_2) \quad (10)$$

$$v_{C5}(t)=v_{C8}(t)\approx\frac{i_{Lr2}(t_2)}{2C_{oss}}(t-t_2) \quad (11)$$

$$v_{C6}(t)=v_{C7}(t)\approx\frac{V_{in}}{2}-\frac{i_{Lr2}(t_2)}{2C_{oss}}(t-t_2) \quad (12)$$

If the energy stored in L_{r1} and L_{r2} at t_2 is greater than the energy stored in C_1-C_8, then C_2, C_3, C_6 and C_7 can be discharged to zero voltage at time t_3.

Mode 4 [t_3 - t_4]: At t_3, C_2, C_3, C_6 and C_7 are discharged to zero voltage and the anti-parallel diodes of S_2, S_3, S_6 and S_7 are conducting. Before i_{Lr1} and i_{Lr2} become negative, S_2, S_3, S_6 and S_7 can be turned on at this moment under ZVS. Since

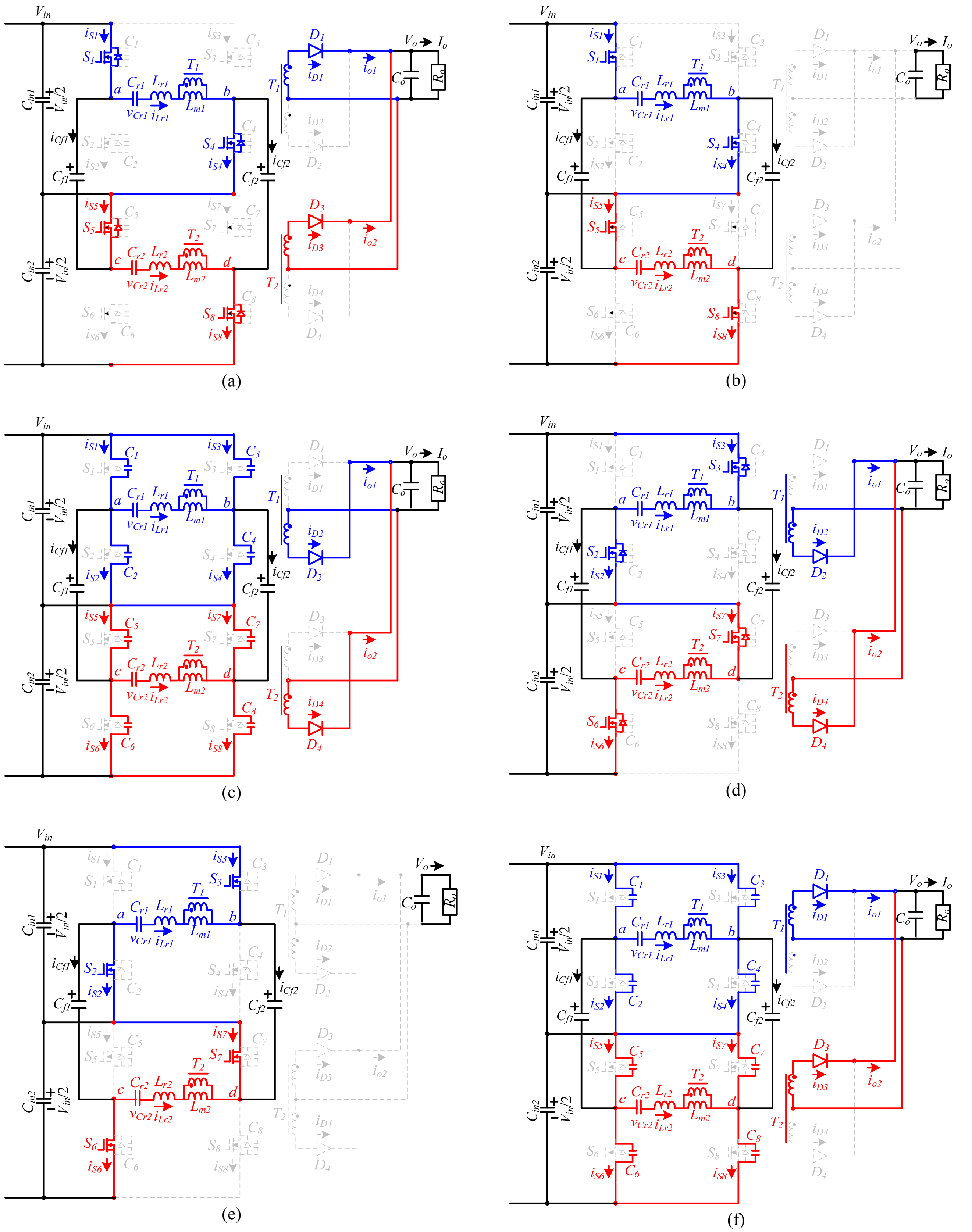


Fig. 3. Operation modes of the proposed converter in one switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

D_2 and D_4 are conducting, $v_{Lm1}=v_{Lm2}=-nV_o$. Thus, i_{Lm1} and i_{Lm2} decrease in this mode. The voltage stresses of S_1 and S_4 are equal to V_{Cin1}, and the voltage stresses of S_5 and S_8 are equal to V_{Cin2}. The flying capacitor voltages $v_{Cf1}=V_{Cin2}$ and $v_{Cf2}=v_{Cin1}$. In circuit module 1, C_{r1} and L_{r1} are resonant with the initial voltage nV_o-$V_{in}/2$-$v_{Cr1}(t_3)$. Similarly, C_{r2} and L_{r2} are resonant with the initial voltage nV_o-$V_{in}/2$-$v_{Cr2}(t_3)$ in the second resonant circuit.

$$i_{Lr1}(t)=\frac{nV_o-V_{in}/2-v_{Cr1}(t_3)}{Z_{r1}}\sin\omega_{r1}(t-t_3)+i_{Lr1}(t_3)\cos\omega_{r1}(t-t_3) \tag{13}$$

$$i_{Lr2}(t)=\frac{nV_o-V_{in}/2-v_{Cr2}(t_3)}{Z_{r1}}\sin\omega_{r1}(t-t_3)+i_{Lr2}(t_3)\cos\omega_{r1}(t-t_3) \tag{14}$$

$$v_{Cr1}(t)=nV_o-V_{in}/2-[nV_o-V_{in}/2-v_{Cr1}(t_3)]\times\cos\omega_{r1}(t-t_3)+i_{Lr1}(t_3)Z_{r1}\sin\omega_{r1}(t-t_3) \tag{15}$$

$$v_{Cr2}(t)=nV_o-V_{in}/2-[nV_o-V_{in}/2-v_{Cr2}(t_3)]\times\cos\omega_{r1}(t-t_3)+i_{Lr2}(t_3)Z_{r1}\sin\omega_{r1}(t-t_3) \tag{16}$$

The input power is transferred to the output load through S_3, L_{r1}, T_1, S_2 and D_2 in resonant circuit 1 and through S_7, L_{r2}, T_2, S_6 and D_4 in resonant circuit 2.

Mode 5 [t_4 - t_5]: At t_4, $i_{Lr1}=i_{Lm1}$ and $i_{Lr2}=i_{Lm2}$. Thus, the diodes D_1-D_4 are off. Since S_2, S_3, S_6 and S_7 are still in the on-state, C_{r1}, L_{r1} and L_{m1} are resonant in circuit 1, and C_{r2}, L_{r2} and L_{m2} are resonant in circuit 2.

$$i_{Lr1}(t)=\frac{-V_{in}/2-v_{Cr1}(t_4)}{Z_{r2}}\sin\omega_{r2}(t-t_4)+i_{Lr1}(t_4)\cos\omega_{r2}(t-t_4) \tag{17}$$

$$i_{Lr2}(t)=\frac{-V_{in}/2-v_{Cr2}(t_4)}{Z_{r2}}\sin\omega_{r2}(t-t_4)+i_{Lr2}(t_4)\cos\omega_{r2}(t-t_4) \tag{18}$$

$$v_{Cr1}(t)=-V_{in}/2+[V_{in}/2+v_{Cr1}(t_4)]\cos\omega_{r2}(t-t_4)+i_{Lr1}(t_4)Z_{r2}\sin\omega_{r2}(t-t_4) \tag{19}$$

$$v_{Cr2}(t)=-V_{in}/2+[V_{in}/2+v_{Cr2}(t_4)]\cos\omega_{r2}(t-t_4)+i_{Lr2}(t_4)Z_{r2}\sin\omega_{r2}(t-t_4) \tag{20}$$

The flying capacitor voltages $v_{Cf1}=V_{Cin2}$ and $v_{Cf2}=v_{Cin1}$ in this mode.

Mode 6 [t_5 - T_s+t_0]: At t_5, S_2, S_3, S_6 and S_7 are turned off and the diodes D_1 and D_3 are conducting. The magnetizing voltages $v_{Lm1}=v_{Lm2}=nV_o$. Thus, i_{Lm1} and i_{Lm2} increase in this mode. Since i_{Lr1} and i_{Lr2} are negative, C_1, C_4, C_5 and C_8 are discharged and C_2, C_3, C_6 and C_7 are charged.

$$v_{C1}(t)=v_{C4}(t)\approx\frac{V_{in}}{2}+\frac{i_{Lr1}(t_5)}{2C_{oss}}(t-t_5) \tag{21}$$

$$v_{C2}(t)=v_{C3}(t)\approx\frac{-i_{Lr1}(t_5)}{2C_{oss}}(t-t_5) \tag{22}$$

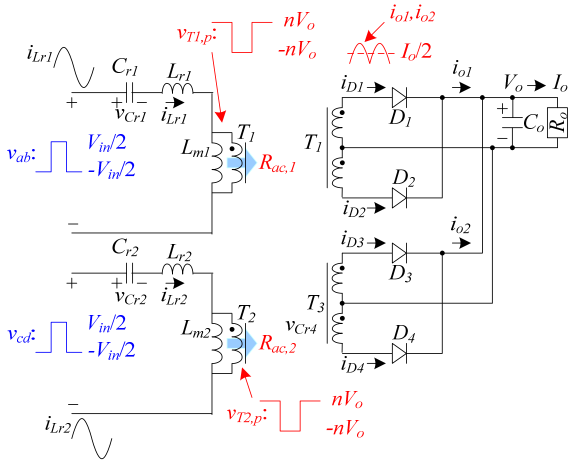


Fig. 4. Equivalent circuit of the proposed converter for the derivation of steady state model.

$$v_{C5}(t)=v_{C8}(t)\approx\frac{V_{in}}{2}+\frac{i_{Lr2}(t_5)}{2C_{oss}}(t-t_5) \tag{23}$$

$$v_{C6}(t)=v_{C7}(t)\approx\frac{-i_{Lr2}(t_5)}{2C_{oss}}(t-t_5) \tag{24}$$

If the energy stored in L_{r1} and L_{r2} at t_5 is greater than the energy stored in C_1-C_8, then C_1, C_4, C_5 and C_8 can be discharged to zero voltage at time T_s+t_0. Then, the operating modes of the proposed converter in a switching cycle are complete.

IV. Converter Performance Analysis

The output voltage of the proposed converter is based on pulse frequency modulation. Thus, the fundamental harmonic approach with a variable switching frequency is used to approximately analyze the steady state of the proposed converter. The power transfer from the input terminal to the output load through two full-bridge resonant tanks is depended on the switching frequency. All of the harmonics of the switching frequency are neglected in the following discussion. Fig. 4 shows an equivalent circuit of the proposed converter for the derivation of the steady state model. The equivalent circuit components in the two resonant tanks are identical. Each resonant tank is supplied one-half of the input power to the output load. Since the duty ratio of each power switch is equal to 0.5, the input AC voltages v_{ab} and v_{cd} of the resonant tanks are square waveforms with two voltage levels $V_{in}/2$ and -$V_{in}/2$. The AC voltages v_{ab} and v_{cd} can be expressed as the fundamental frequency term and the harmonics term.

$$v_{ac}(t)=v_{cd}(t)=\frac{2V_{in}}{\pi}\sin\omega_s t+\sum_{n=2}^{\infty}\frac{2V_{in}}{n\pi}\sin n\omega_s t \tag{25}$$

From (25), the fundamental root-mean-square (*rms*) value of v_{ab} and v_{cd} is equal to $\sqrt{2}V_{in}/\pi$. Due to the on-off states of

D_1-D_4, the fundamental *rms* value of the magnetizing voltages is expressed as $v_{Lm1,rms} = v_{Lm2,rms} = 2\sqrt{2}nV_o/\pi$. Since the average output current of each center-tapped rectifier is equal to $I_o/2$, the *rms* value of the secondary winding currents is equal to $i_{T1,s,rms} = i_{T2,s,rms} = \pi I_o/4\sqrt{2}$. Therefore, the load resistance R_o reflected to the transformer primary side can be expressed as:

$$R_{ac,1} = R_{ac,2} = R_{ac} = \frac{v_{Lm1,rms}}{i_{T1,rms,s}/n} = \frac{16n^2}{\pi^2}R_o \quad (26)$$

The resonant tank is excited by an effectively fundamental sinusoidal input voltage v_f and it drives the effective AC resistive load R_{ac}. The pulse frequency modulation (PFM) scheme is adopted to regulate the AC voltage gain of the proposed converter. The AC voltage gain of the resonant tank can be expressed as:

$$|G_{ac}(f_s)| = 1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2 + Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2} \quad (27)$$

where $f_r = 1/(2\pi\sqrt{L_rC_r})$, $Q = \sqrt{L_r/C_r}/R_{ac}$, $k=L_r/L_m$, $C_{r1}=C_{r2}=C_r$, $L_{r1}=L_{r2}=L_r$ and f_s is the switching frequency. The DC voltage gain G_{dc} of the proposed converter is given as:

$$G_{dc} = \frac{2n(V_o+V_f)}{V_{in}} \quad (28)$$

where V_f is the voltage drop on the rectifier diodes D_1-D_4. If the input and output DC voltages are given, the operating switching frequency can be obtained by $G_{dc}=G_{ac}$.

A laboratory prototype is implemented with the following specifications: V_{in}=750V-800V, V_o=48V, P_o=1500W and the series resonant frequency f_r=120kHz. The primary and secondary winding turns of the transformers T_1 and T_2 are 34 turns and 4 turns, respectively. Thus, the minimum and maximum DC voltage gains of the resonant converter are expressed as:

$$G_{dc,\min} = \frac{2n(V_o+V_f)}{V_{in,\max}} = \frac{2\times(34/4)\times(48+1.1)}{800} \approx 1.04 \quad (29)$$

$$G_{dc,\max} = \frac{2n(V_o+V_f)}{V_{in,\min}} = \frac{2\times(34/4)\times(48+1.1)}{750} = 1.11 \quad (30)$$

The AC equivalent resistance R_{ac} at the full load condition is given as:

$$R_{ac} = \frac{16n^2R_o}{\pi^2} \approx 180\Omega \quad (31)$$

In the prototype circuit, the selected inductance ratio of L_r and L_m is $k=L_r/L_m$=0.2. Based on (27), (29) and (30), the AC voltage gain curves of the proposed converter with different quality factors Q and frequency ratios F at k=0.2 are illustrated in Fig. 5. From Fig. 5, it is observed that the output voltage can be regulated if the quality factor Q≤0.5 at a full load. Therefore, Q=0.5 at a full load is selected in the prototype circuit. The AC voltage gain of the proposed converter at the no load condition (Q=0) is given as:

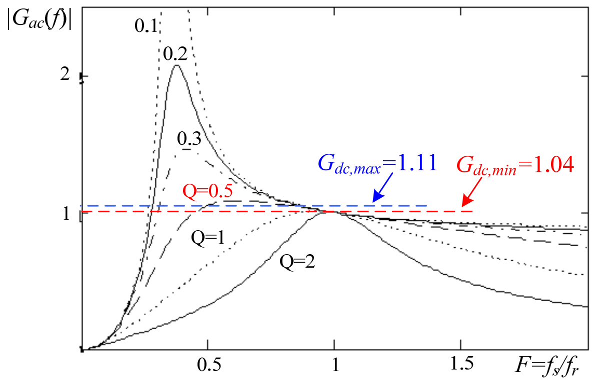


Fig. 5. Gain curves of proposed resonant converter with $V_{in,min}$=750V and $V_{in,max}$=800V.

$$|G_{ac}(f_s)|_{Q=0, f_s=\infty} \approx 1/(1+k) = 0.83 < G_{dc,\min} \quad (32)$$

Therefore, the output voltage V_o can be regulated at the no load condition. Based on the derived R_{ac}, k, Q and f_r, the resonant inductances, the magnetizing inductances and the resonant capacitances can be obtained.

$$L_r = L_{r1} = L_{r2} = \frac{QR_{ac}}{2\pi f_r} = \frac{0.5\times 180}{2\pi\times 120\times 10^3} \approx 110\mu\text{H} \quad (33)$$

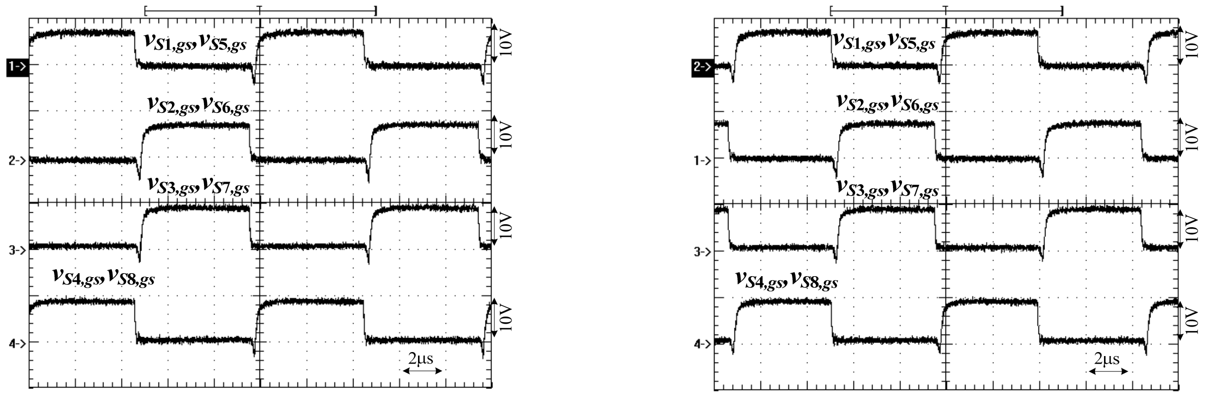
$$L_{m1} = L_{m2} = L_r/k = \frac{110\mu H}{1/5} = 550\mu\text{H} \quad (34)$$

$$C_{r1} = C_{r2} = \frac{1}{4\pi^2 L_r f_r^2} \approx 16\text{nF} \quad (35)$$

The voltage stress of S_1-S_8 is equal to $V_{in,max}/2$=400V. MOSFETs (IRFP460) with 500V/20A ratings are selected for S_1-S_8. The voltage stress and average current of D_1-D_6 are equal to $2(V_o+V_f)=98.2$V and $I_{o,\max}/4 \approx 7.8$A, respectively. Diodes (KCU30A30) with 300V/30A ratings and a 1.1V voltage drop are adopted for D_1-D_4. The adopted capacitances $C_{in1}=C_{in2}$=470μF/450V, $C_{f1}=C_{f2}$=100nF/630V and C_o=2200μF/100V.

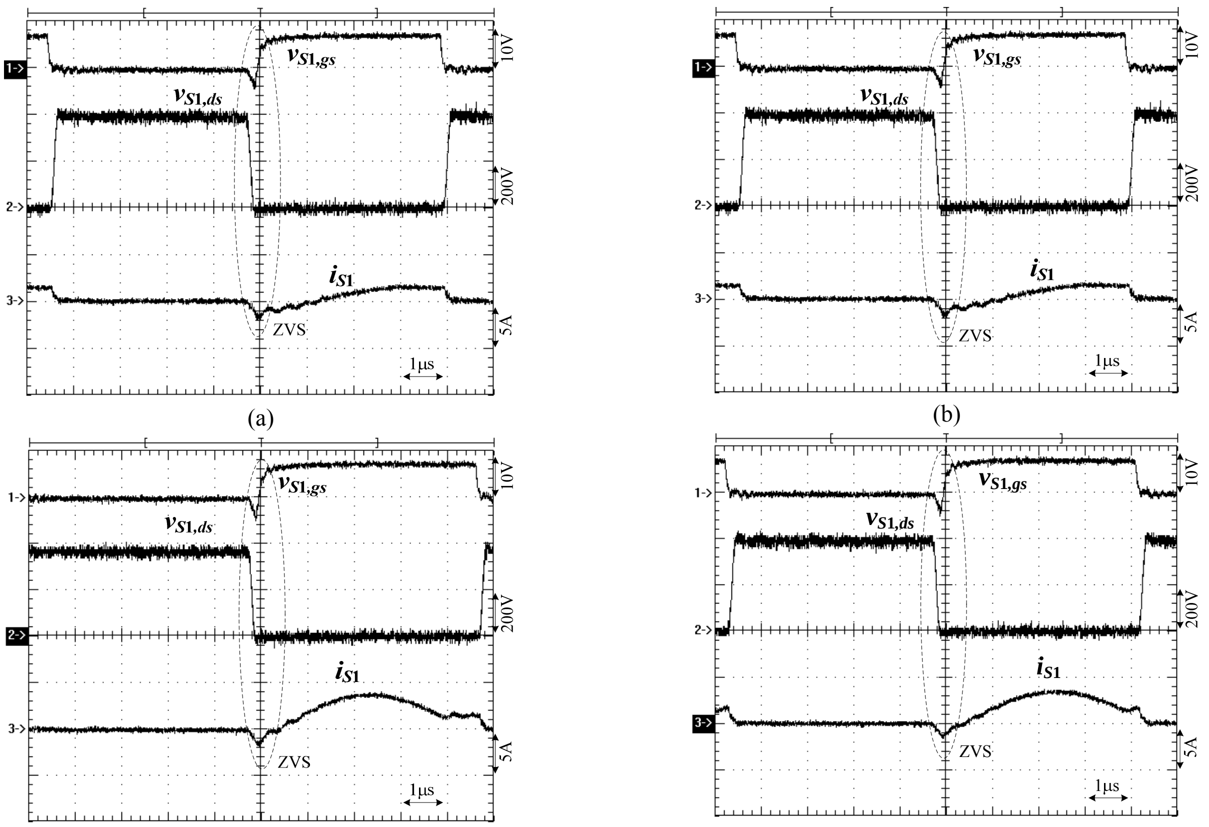
V. EXPERIMENTAL RESULTS

Experiments with a prototype circuit, with the circuit components derived in the previous section, are provided to demonstrate the performance of the proposed converter. Fig. 6 shows the measured gate voltages of S_1-S_8 at a full load with the input voltage V_{in}=750V and 800V conditions. Fig. 7 illustrates the measured gate voltage, drain voltage and switch current of S_1 at light (25%) and full (100%) loads with different input voltages. Before S_1 is turned on, i_{S1} is negative to discharge the drain-to-source capacitor of S_1. Therefore, S_1 can be turned on under ZVS when the drain voltage $v_{S1,ds}$ is decreased to zero voltage. Since S_4, S_5 and S_8 have the same PWM waveforms as S_1, it is clear that S_4, S_5 and S_8 are also turned on under ZVS from a 25% load to a full load. Fig. 8 shows the measured gate voltage, drain voltage and switch current of S_2 at light (25%) and full (100%) loads with



(a) (b)

Fig. 6. Measured gate voltages of S_1-S_8 at full load and (a) V_{in}=750V (b) V_{in}=800V.



(c) (d)

Fig. 7. Measured gate voltage, drain voltage and switch current of S_1 at (a) 25% load and V_{in}=750V (b) 25% load and V_{in}=800V(c) 100% load and V_{in}=750V(d) 100% load and V_{in}=800V.

different input voltages. S_2 is also turned on under ZVS from a 25% load to a full load. Since the PWM signals of S_3, S_6 and S_7 are identical to the PWM signal of S_2, it can be determined that S_3, S_6 and S_7 are also turned on under ZVS. Fig. 9 gives the measured results of the gate voltages, AC terminal voltages, resonant inductor currents and resonant capacitor voltages at a full load. The two inductor currents and the two capacitor voltages are balanced under the test results. Fig. 10 gives the measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at a full load. In the same manner, the measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at a full load are shown in Fig. 11. When the switches S_1 and S_5 are in the on-state and S_2 and S_6 are in the off-state, the flying capacitor voltage V_{Cf1} is equal to the input capacitor voltage V_{Cin1} with half of a switching period. Similarly, the flying capacitor voltage V_{Cf1}=V_{Cin2} when the switches S_1 and S_5 are in the off-state and S_2 and S_6 are in the on-state with half of a switching period. Therefore, both of the input capacitor voltages V_{Cin1} and V_{Cin2} are automatically balanced at $V_{in}/2$. Fig. 12 gives test results for the two input capacitor voltages v_{Cin1} and v_{Cin2} and the two flying capacitor voltages at the full

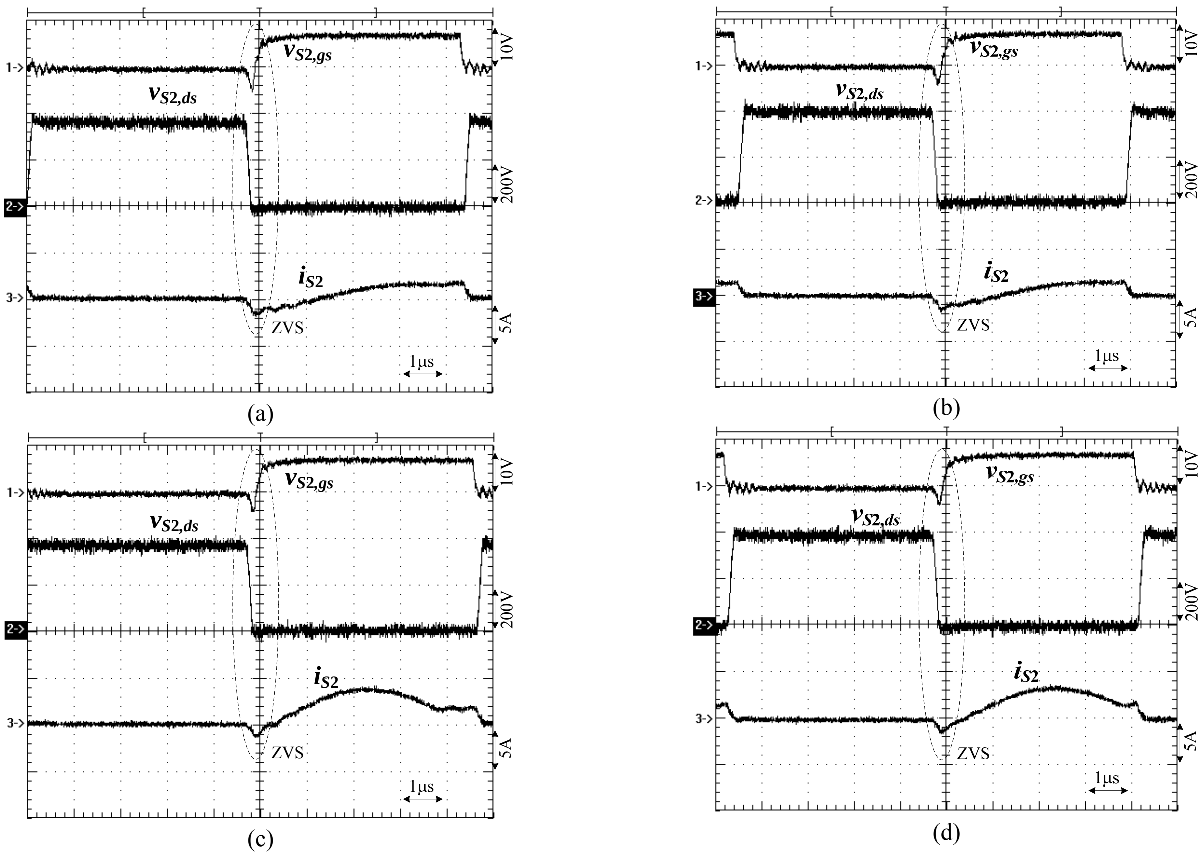


Fig. 8. Measured gate voltage, drain voltage and switch current of S_2 at (a) 25% load and V_{in}=750V (b) 25% load and V_{in}=800V(c) 100% load and V_{in}=750V(d) 100% load and V_{in}=800V.

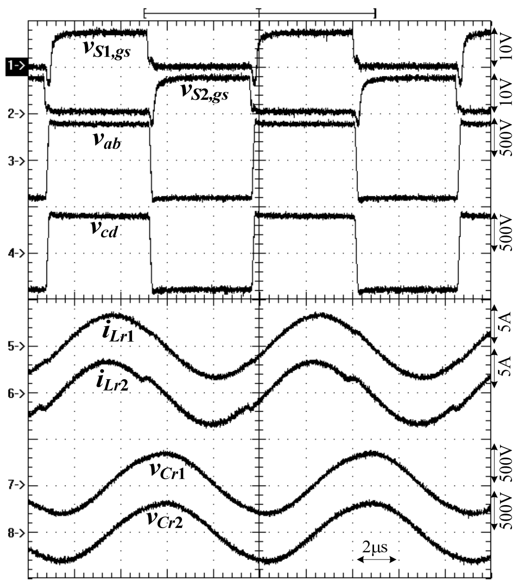


Fig. 9. Measured results of the gate voltages $v_{S1,gs}$ and $v_{S2,gs}$, AC terminal voltages v_{ab} and v_{cd}, resonant inductor currents i_{Lr1} and i_{Lr2}, and resonant capacitor voltages v_{Cr1} and v_{Cr2} at full load.

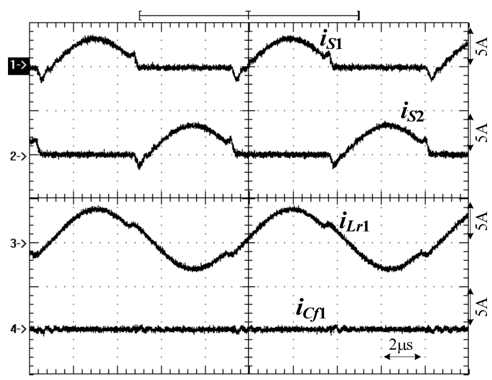


Fig. 10. Measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at full load.

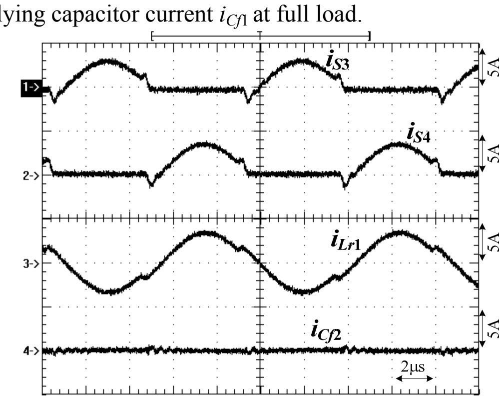


Fig. 11. Measured switch currents i_{S3} and i_{S4}, inductor current i_{Lr1} and flying capacitor current i_{Cf2} at full load.

load and 800V input voltage case. It is clear that the two input capacitor voltages v_{Cin1} and v_{Cin2} are balanced at 400V and $v_{Cf1}=v_{Cf2}=v_{Cin1}=v_{Cin2}=V_{in}/2$. Fig. 13 shows the measured diode currents and two circuit output currents at the full load

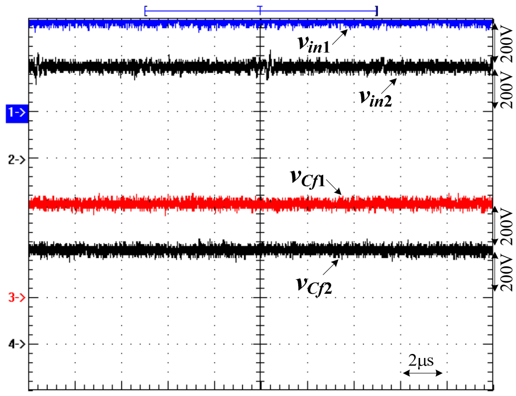


Fig. 12. Measured results of input capacitor voltages and flying capacitor voltages at full load and 800V input voltage case.

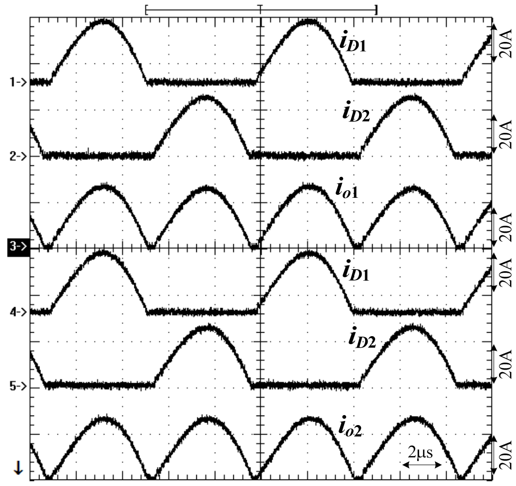


Fig. 13. Measured diode currents and two circuit output currents at full load condition.

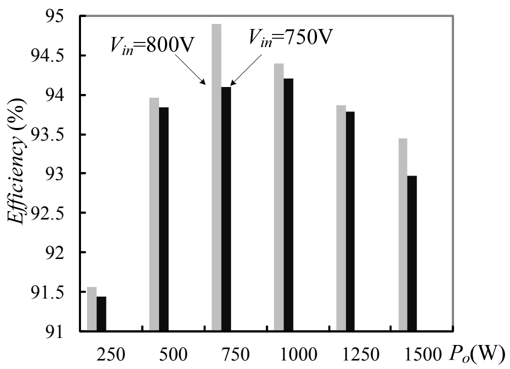


Fig. 14. Measured efficiencies of the proposed converter with different input terminal voltages and load conditions.

condition. The output currents i_{o1} and i_{o2} are balanced. Fig. 14 shows the measured circuit efficiencies of the proposed converter under different load and input voltage conditions.

VI. Conclusion

This paper presents a new full-bridge resonant converter with the characteristics of low voltages stress MOSFETs, ZVS turn-on for the MOSFETs, no reverse recovery current on the rectifier diodes, balanced two input capacitor voltages and high circuit efficiency. Two half-bridge converter legs with two spilt capacitors are adopted to reduce the voltage stress of the MOSFETs at $V_{in}/2$. Therefore, the proposed converter is suitable for use in high input voltage applications. The two flying capacitors C_{f1} and C_{f2} are used to automatically balance the two input capacitor voltages in every switching cycle. The two resonant circuits are used to increase the load power and to achieve ZVS for all of the power semiconductors. The system analysis, a design example and experiments are presented to demonstrate the effectiveness of the proposed converter.

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