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Synthesis and Implementation of a Multi-Port DC/DC Converter for Hybrid Electric Vehicles

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Abstract

A non-isolated Multiple Input Converter (MIC) with an input port, two storage ports and a load port is proposed. The synthesis of the proposed four port converter with its switch realization is presented. A steady state analysis of each operating mode with a small-signal model is derived, and a stability analysis is done. A mode selection controller is proposed to automatically choose a specific operating mode based on the voltage levels of the different source and storage units. In addition, a voltage control loop is used to regulate the output voltage. A 200W prototype is built with a TMS320F28027 DSP controller to test the feasibility of the operating modes. Simulation and experimental results show the ability of the proposed converter to handle multiple inputs either individually or simultaneously.

Key words: DSP, Hybrid Electric Vehicle, Multiple Input Converter, Stateflow model, Synthesis, Ultracapacitor

I. INTRODUCTION

With the increased attention towards energy efficiency and environmental pollution, alternatives with a small carbon footprint have found renewed interest in recent times. The traditional way to improve energy efficiency is to shift to all-electric. Transportation, a major contributing factor for greenhouse gas emissions has started to electrify its infrastructure. Electric Vehicles are the forerunners in electrified transportation and this technology is now growing by leaps and bounds. While the carbon footprint of an Electric Vehicle (EV) is actively debated [1], [2], it is seen as a promising alternative to curb fuel costs [3]. EV's have a unique power profile that has both power utilization and regeneration at different instants of its operation. Since a pure EV has a high efficiency (68%) and a low cost when compared to Fuel Cell (FC) based EVs (30%), research on the latter has been losing significance [4].

Electric vehicle growth is greatly impacted by power electronics technology with the introduction of different architectures [5], [6].

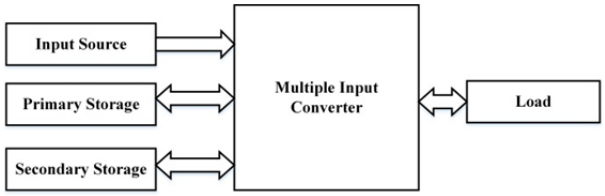

Fig. 1. Block diagram of Multiple Input Converter.

The Electric Vehicle, in the course of evolution, has included many onboard sources and storage units [7]. To quench and capture the intermittent requirements, high energy density ultra-capacitors are used in addition to a primary source [8]. The excellent performance of a battery with an ultracapacitor energy storage system has been reported in [9], [10]. This necessitates a multi-port power converter that manages power from all of the sources and delivers a regulated voltage to the load.

The multi-port converters available in the literature can be broadly classified into two major categories: Isolated and Non-Isolated Converters. Isolated converters are preferred if the voltage difference between the source and the load is high. Isolated converters show a common trend of shared secondary winding with individual primary windings for

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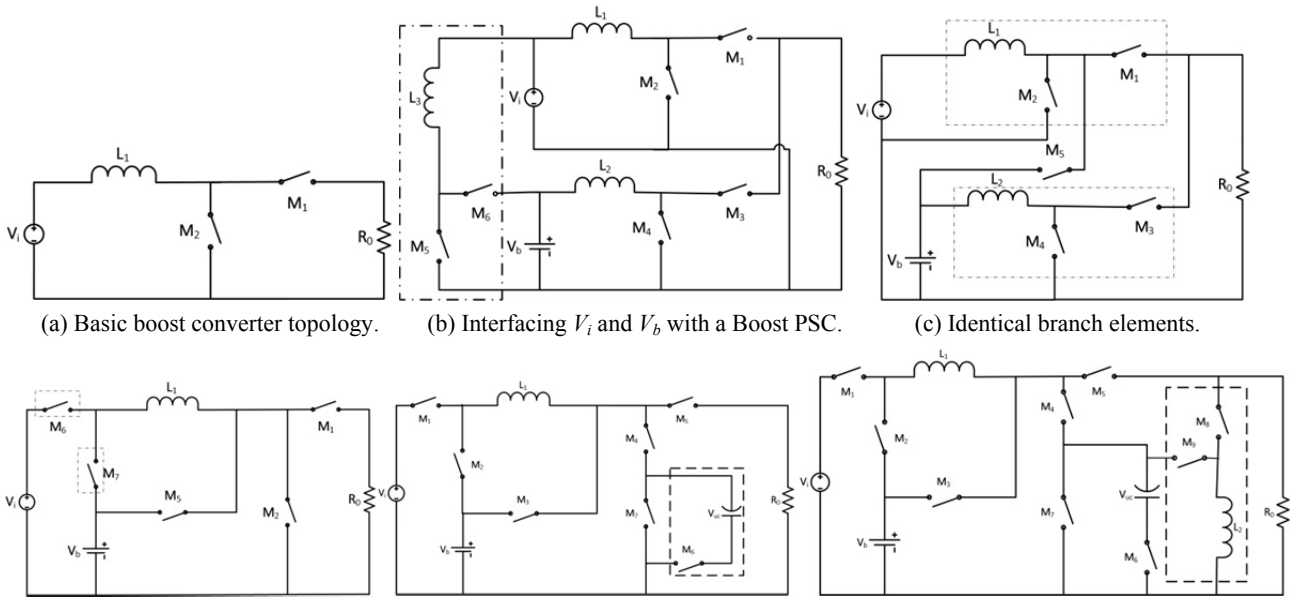


(a) Basic boost converter topology. (b) Interfacing V_i and V_b with a Boost PSC. (c) Identical branch elements.

(d) Inclusion of pre-regulating Switch. (e) Adding third port. (f) Four Port MIC with generic switches.

Fig. 2. Synthesis of Four Port Converter.

different sources [11], [12]. Although isolated converters are advantageous in output voltage control and isolation, the peripheral circuitry and multi-source operation are highly complex [13]. Several single input converters eligible for an extension to multi-port versions were proposed in [14], [15].

Non-isolated converters have the advantage of a compact structure, simple control, and low cost. As a result, there has been an increase in their usage in mobile applications. Non-isolated Multiple Input Converters (MIC) were initially paralleled primary converters with time-multiplexed operation [16], [17]. [18] analyzes a battery-ultracapacitor system with a non-isolated buck-boost converter. The concept of Pulsating Source Cells (PSC) was introduced and two families of Multiple Input Converters (MIC) were generated and analyzed in [19]. [20] extended the concept of PSC to basic non-isolated converters and proposed rules to synthesize them. Besides topology derivation, several studies have been done on the control of MICs [20]-[23] and interleaved converters [24]-[27]. On the synthesis of MIC, [28] is one of the earliest work done on the generation of DC/DC converters, and [29] extended this by proposing rules to identify basic topologies that are eligible for extension to multiple input versions. With the large variety of non-isolated converters available in the literature, a limited amount of work has been done on the simultaneous utilization of different power sources. The scenario in a renewable hybrid power system is that various intermittent power sources are ready to supply power at any given time instant. If the idea of time-multiplexing of input sources is adopted, the readily available energy from renewable sources is wasted. Among the possible sources, the most readily available one, aided by a secondary source in case of emergency, is needed.

This research work proposes a four port DC/DC converter suitable for Hybrid Electric Vehicles (HEV) with a renewable energy source port, two storage ports and a load port as shown in Fig. 1. The originality of the work lies in the utilization of an inductor as a buffer to transfer energy from two sources to a load. The synthesis of the proposed converter from the primary PSC, the switch realization, the small-signal model and its design are presented in this work.

II. Proposed Converter Topology

A Multiple Input Converter (MIC) serves the purpose of handling various input sources and delivering power to the load. In an EV, the MIC is used as a power processor. A power converter for HEV should possess the following characteristics:

1. Power available from various sources and the storageunits have to be handled individually or simultaneously.
2. Irrespective of the condition of the source/storage units, a regulated voltage has to be applied to the load.
3. Regenerated power has to be captured and stored.
4. Excess power produced by renewables under the idle condition has to be stored.
5. Deep cycling of the batteries should be avoided.
6. A low-cost rugged structure with a low volume is preferred

A. Synthesis

To synthesize the proposed converter, PSCs with generic switches are used, and the rules for the synthesis of multi-port converter proposed in [30] are utilized. The objective is to synthesize a Four Port Converter [31] with one source port

TABLE I
SWITCH REALIZATION ANALYSIS

Operating mode	Voltage across switching device								
	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
Mode1 State1	ON	V_i- V_b	V_i-V_{L1} - V_b	ON	V_i - V_{L1}	V_{uc}	ON	-	-
Mode1 State2	ON	V_i - V_b	V_i-V_{L1}- V_b	V_i-V_{L1} + V_{uc}	ON	-	-	V_i - V_{L1}	-
Mode2 State1	V_i - V_b	ON	- V_b	ON	V_b - V_{L1}	V_{uc}	ON	-	-
Mode2 State2	V_i - V_b	ON	V_b - V_0	V_b - V_{L1}	ON	V_{uc}	-	V_b - V_{L1}	-
Mode3 State1	ON	V_i - V_b	- V_b	ON	V_i - V_{L1}	ON	- V_{uc}	-	- V_{uc}
Mode3 State2	ON	V_i - V_b	V_i - V_{L1} - V_b	V_i - V_{L1}	ON	V_{uc}	-	V_i- V_{L1}	-
Mode4 State1	V_i- V_b	ON	V_i + V_b	ON	V_b - V_{L1}	ON	- V_{uc}	-	- V_{uc}
Mode4 State2	V_i - V_b	ON	V_b - V_0	V_b - V_{L1}	ON	V_{uc}	-	V_b - V_{L1}	-
Mode5 State1	ON	V_i - V_b	V_i - V_{L1} - V_b	ON	V_i - V_{L1}	V_{uc}	ON	-	-
Mode5 State2	ON	V_i - V_b	ON	V_i - V_{L1}	V_i - V_{L1}	V_{uc}	-	-	-
Mode6 State1	-	-	-	-	- V_0	-	-	ON	V_0+ V_{uc}
Mode6 State2	-	-	-	-	-	- V_{uc}	-	V_0 - V_{L2}	ON

(V_i), a primary storage port (V_b), a secondary storage port (V_{uc}) and a load port (V_0). The voltage levels are assumed to be in the following order $V_i < V_b < V_{uc}$. A generic switch model of a boost PSC is shown in Fig. 2(a). To begin the synthesis two of these boost PSC with a shared load port taken. Since there is a need to control the power from each source individually or simultaneously, the ports V_i and V_b have to be interfaced. Since the voltage V_b is greater than V_i , a boost PSC is chosen to interface these two ports as shown in Fig. 2(b). Looking from the source port V_i, the L_1−M_1 and L_3−M_5 branches have a similar structure. These two branches could be simplified into a single branch with M5 as shown in Fig. 2(c). Similarly, looking from the load port V_0, L_1−M_1−M_2 and L_2−M_3−M_4 have a similar structure as shown in Fig. 2(c). These two similar structures can be reduced to a single structure that leads to a lack of controllability in both the V_i and V_b ports. This could be improved with the inclusion of two pre-regulating switches in series with the two input ports as shown in Fig. 2(d).

B. Addition of a Third Port

The reduced converter for two ports can be extended to a three port version with the addition of a Pulsating Voltage Source Cell (PVSC). Since the third port acts as a secondary port that aids the other two input ports, it has to be included in a loop that is common to the other two input ports. Multiple PVSCs can be connected in series since this obeys Kirchoff's laws. The third port should be connected in series with the other two source ports. At the same time, if the polarity of the third port is reversed, it can aid the other sources while the common inductor is charging. A buck PVSC [19] is included in the common loop with the renumbered switches is shown in Fig. 2(e).

C. Addition of a Regeneration Path

Often in a HEV, there is a need to capture regenerated power. The power regenerated in the load port in this converter has to be routed back to a third port since it handles the intermittent power intervals. The polarity of the third port is inverted so that the interfacing PSC should be able to invert the polarity. All of the forward power flow paths are boosting, which necessitates a regenerative path to buck the voltage level. Out of the two possible PSCs (Cuk and Buck-Boost), a Buck-Boost PSC is chosen since it can do both voltage reduction and inversion. The final circuit with the switches renumbered is shown in Fig. 2(f).

D. Switch Realization

The synthesized circuit, as shown in Fig. 2(f), has generic switches (M_1-M_8). The realization of these ideal switches with semiconductor devices depends on the polarity of the voltages that the switch should block and the polarity of the current during conduction [32]. To understand the voltage across and the current through each switch, a complete knowledge of the significant operating modes with the switches (M_1-M_8) is necessary. A simplified generic switch analysis of the proposed converter is summarized in Table I. Based on this analysis, the voltage blocking capability required for each switch is ascertained and the switching devices were chosen. The switches M_2, M_3, M_4, M_6, M_8 are replaced with MOSFETs as S_1-S_5, and the switches M_1, M_5, M_7, M_9 are replaced by the diodes D_1-D_4, respectively. The resultant power circuit is shown in Fig. 3.

E. Operating Modes

Several operating modes are possible with the combination of different switches. With different combinations of sources,

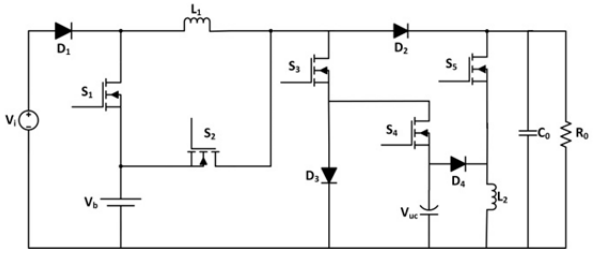
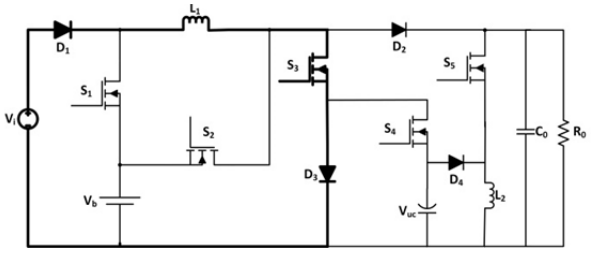
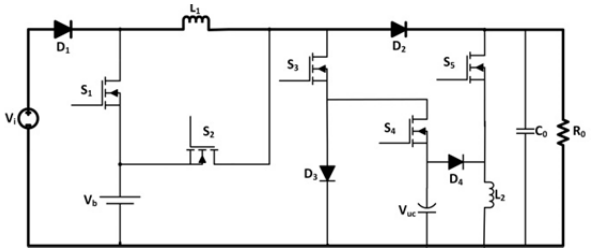


Fig. 3. Proposed Four Port MIC topology for HEV.



(a) State 1.



(b) State 2.

Fig. 4. Switching states in Mode 1.

six meaningful operating modes were identified. The operating modes are as follows:

1. Input source supplying the load
2. Primary storage supplying the load
3. Secondary storage aids the input source to supply the load
4. Secondary storage aids the primary storage to supply the load
5. Input source supplying the primary storage
6. Regeneration

III. Steady State Modeling and Mode Analysis

Each operating mode is analyzed in this section by applying the volt-second and charge-second balance [32]. All of the semiconductor switching devices are assumed to be lose-less. The duty cycle associated with each switching device is denoted by the letter *'d'* followed by the number of the corresponding switching device. Each mode consists of two switching states. The inductor current in each switching state along with the steady state equations are presented. Out of the six modes, five modes basically do the boost operation and the buck-boost operation appears in the sixth mode.

A. Mode 1

In the first mode, the primary source supplies the load. This mode has two switching states. In the first state, S_3, D_1, and D_3 are ON as shown in Fig. 4(a). The inductor current builds up and is given by:

$$\frac{di_{L1}}{dt} = \frac{V_i}{L_1} \quad (1)$$

During the second switching state, the switching devices D1 and D2 are turned ON as shown in Fig. 4(b). The inductor supplies the load and the rate of the current decrease is given by:

$$\frac{di_{L1}}{dt} = \frac{V_i - V_0}{L_1} \quad (2)$$

By applying the volt-second balance to inductor L_1:

$$\langle V_{L_1} \rangle_{T_s} = V_i \times d_3 + (V_i - V_0) \times (1 - d_3) = 0 \quad (3)$$

where d_3 is the duty cycle of the switching device S_3. Rearranging this yields:

$$V_0 = \frac{V_i}{1 - d_3} \quad (4)$$

B. Mode 2

In this mode, energy is transferred from the primary storage device (V_b) to the load. This mode is initialized when V_i drops below a prefixed threshold level. As a result, the diode D_1 is turned off. In the first state, the switching devices S_1, S_3 and D_3 are turned ON as shown in Fig. 5(a), and the rate of change of the current in the inductor L_1 is given by:

$$\frac{di_{L1}}{dt} = \frac{V_b}{L_1} \quad (5)$$

In the second state, the energy stored in the inductor is transferred to the load as shown in Fig. 5(b) The rate of change of the current in the inductor L_1 is given by:

$$\frac{di_{L1}}{dt} = \frac{V_b - V_0}{L_1} \quad (6)$$

Applying inductor volt-second balance to the inductor L1 in the steady state:

$$\langle V_{L_1} \rangle_{T_s} = V_b \times d_3 + (V_b - V_0) \times (1 - d_3) = 0 \quad (7)$$

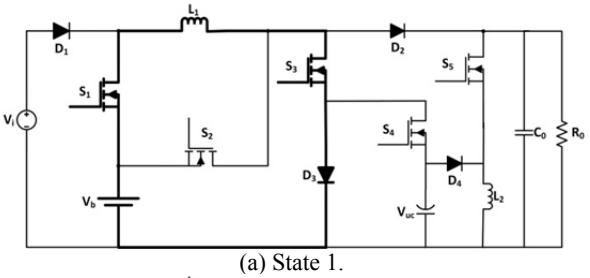
Rearranging this yields:

$$V_0 = \frac{V_b}{1 - d_3} \quad (8)$$

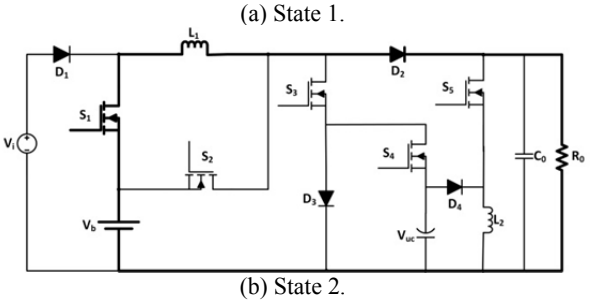
C. Mode 3

The unique feature of this topology lies in its ability to transfer energy from multiple sources to the load simultaneously. This mode is initiated when the level of the input source falls below a prefixed threshold level. In this mode, the secondary storage (V_{uc}) assists the input source (V_i). Note that the polarity of the secondary storage is reversed to ensure the voltage addition in state 1. The switching devices turned on in this state are S_3, S_4 and D_1 as shown in Fig. 6(a). The rate of change of the inductor current is given by:

$$\frac{di_{L1}}{dt} = \frac{V_i + V_{uc}}{L_1} \quad (9)$$

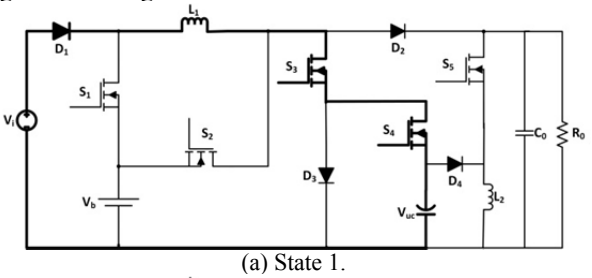


(a) State 1.

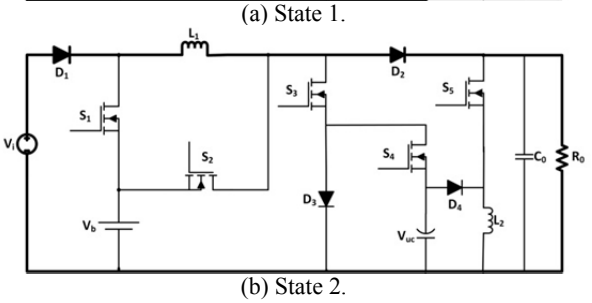


(b) State 2.

Fig. 5. Switching states in Mode 2.

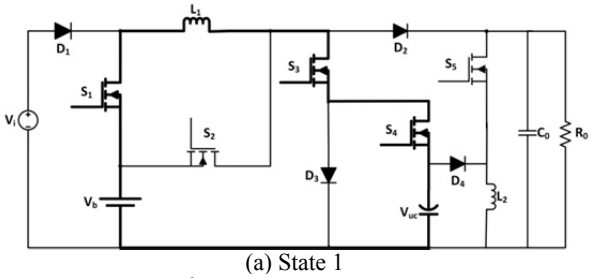


(a) State 1.

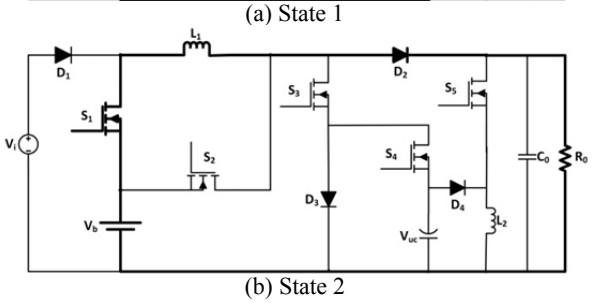


(b) State 2.

Fig. 6. Switching states in Mode 3.

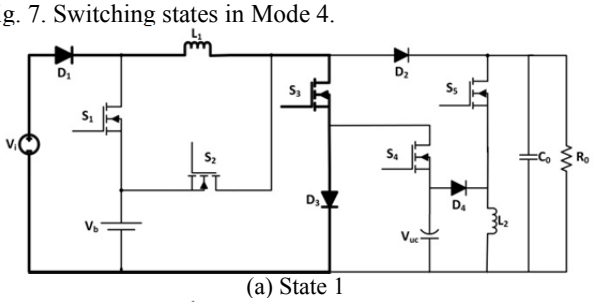


(a) State 1

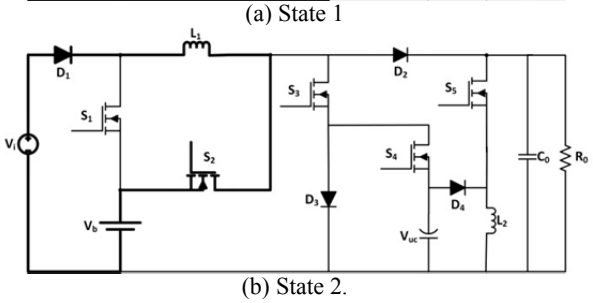


(b) State 2

Fig. 7. Switching states in Mode 4.



(a) State 1



(b) State 2.

Fig. 8. Switching states in Mode 5.

The second switching state turns the switching devices D_1 and D_2 ON as shown in Fig. 6(b). This yields:

$$\frac{di_{L1}}{dt} = \frac{V_i - V_0}{L_1} \quad (10)$$

The volt-second balance on the inductor L_1 yields:

$$V_0 = \frac{V_i + V_{uc} \times d_4}{1 - d_4} \quad (11)$$

D. Mode 4

This is another hybrid mode that facilitates simultaneous power delivery from different sources. In this mode, the secondary storage (V_{uc}) assists the primary storage (V_b) in supplying energy to the load. In state 1 the switching devices S_1, S_3 and S_4 are ON as shown in Fig.7(a), and the inductor charging current is given by:

$$\frac{di_{L1}}{dt} = \frac{V_b + V_{uc}}{L_1} \quad (12)$$

The turn-on of the switching devices S1 and D2, as shown in Fig. 7(b), delivers the energy stored in the inductor to the load, and the rate of the inductor discharging current is given by:

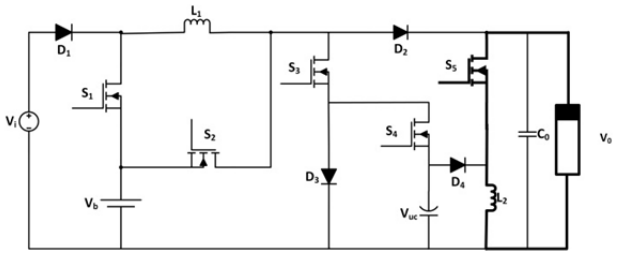
$$\frac{di_{L1}}{dt} = \frac{V_b - V_0}{L_1} \quad (13)$$

The volt-second balance on the inductor L_1 yields:

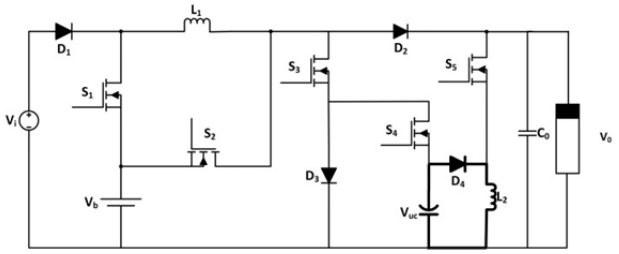
$$V_0 = \frac{V_2 + V_{uc} \times d_4}{1 - d_4} \quad (14)$$

E. Mode 5

This mode facilitates the energy transfer between different sources. If the source V_i is generating excess energy (consider the case of a solar panel with an electric vehicle at rest) that is not needed by the load, it could be stored in the primary storage device. The switching devices S_3, D_1 and D_3 are active during state1 as shown in Fig. 8(a). The rate of change



(a) State 1.



(b) State 2.

Fig. 9. Switching states in Mode 6.

TABLE II
ACTIVE SWITCHING DEVICES IN EACH MODE

Operating mode	Conducting switches	
	State I	State II
Mode 1	S_3,D_1,D_3	D_1,D_2
Mode 2	S_1,S_3,D_3	S_1,D_2
Mode 3	S_3,S_4,D_1	D_1,D_2
Mode 4	S_1,S_3,S_4	S_1,D_2
Mode 5	S_3,D_1,D_3	S_2,D_1
Mode 6	S_5	D_4

of the inductor current is given by:

$$\frac{di_{L1}}{dt} = \frac{V_i}{L_1} \quad (15)$$

The second switching state, as shown in Fig.8(b), with the active switches S_2 and D_1 transfer energy to the second port. This yields:

$$\frac{di_{L1}}{dt} = \frac{V_i - V_b}{L_1} \quad (16)$$

The volt-second balance on the inductor L_1 yields:

$$V_b = \frac{V_i}{1 - d_3} \quad (17)$$

F. Mode 6

This mode facilitates the capture of regenerated energy. Since the regenerated voltage magnitude is greater than the source voltage, a buck-boost PSC is used. The first switching state in this mode, as shown in Fig.9(a), the switch S_5 is ON. The rate of change of the inductor current i_{L2} is given by:

$$\frac{di_{L2}}{dt} = \frac{V_0}{L_2} \quad (18)$$

The energy stored in the inductor L_2 will be transferred to the secondary storage through the diode D_4 as shown in Fig. 9(b). The rate of change of the inductor current is given by:

$$\frac{di_{L2}}{dt} = \frac{V_{uc}}{L_2} \quad (19)$$

The volt-second balance on the inductor L2 yields:

$$V_{uc} = \frac{-V_0 \times d_5}{1 - d_5} \quad (20)$$

The negative sign in the volt-second balance equation denotes the voltage inversion necessary to take the voltage from the load to the polarity inverted secondary storage port. A summary of the active switching devices in each mode is shown in Table II.

IV. CONTROLLER FOR THE PROPOSED FOUR PORT CONVERTER

The four port converter proposed in this work utilizes two types of control mechanisms. While one controller decides the current mode of operation based on different operating conditions, the other regulates the output voltage.

A. Mode Selection Logic

The objective of this controller is to choose an appropriate operating mode based on the system parameters like the voltage level of the source/storage units and the load requirement. For ease of control, the modes are grouped into three different categories.

1. *Motoring*: All of the forward power flow modes are grouped under this category (Mode 1- Mode 4)
2. *Standstill Charging*: This mode facilitates the energy flow between the sources (Mode 5).
3. *Regeneration*: This mode covers the reverse power flow (Mode 6).
4. *Emergency Stop*: This is a fusing mode when the power levels of the source/storage units are almost empty (Mode 7).

The mode control algorithm supervises the system by continuously monitoring the system parameters like the voltage level of the source/storage units, the load requirements and the system status. A Stateflow chart for the proposed system is shown in Fig. 10. The system variables stated in the Stateflow chart are summarized in Table III.

A single flow cycle is explained to understand the chart. At the initial stage, the *Motoring* group is initialized as it is the default starting state. This group has four modes and the empty arrow in Mode 1 denotes the default starting state. For each group/state, the preference of the conditions is set by the numbers on the pointing arrowheads. For Mode 1, there are two possible next states (Mode 2 and Mode 3) and the number on its arrowhead denotes its preference. Once Mode 1 is initiated, a registry is set for the variable 'u' and a value is set. In the meantime, a communication is sent to the controller to be able to select a corresponding mode. All of the system parameters listed in the Table III are continuously

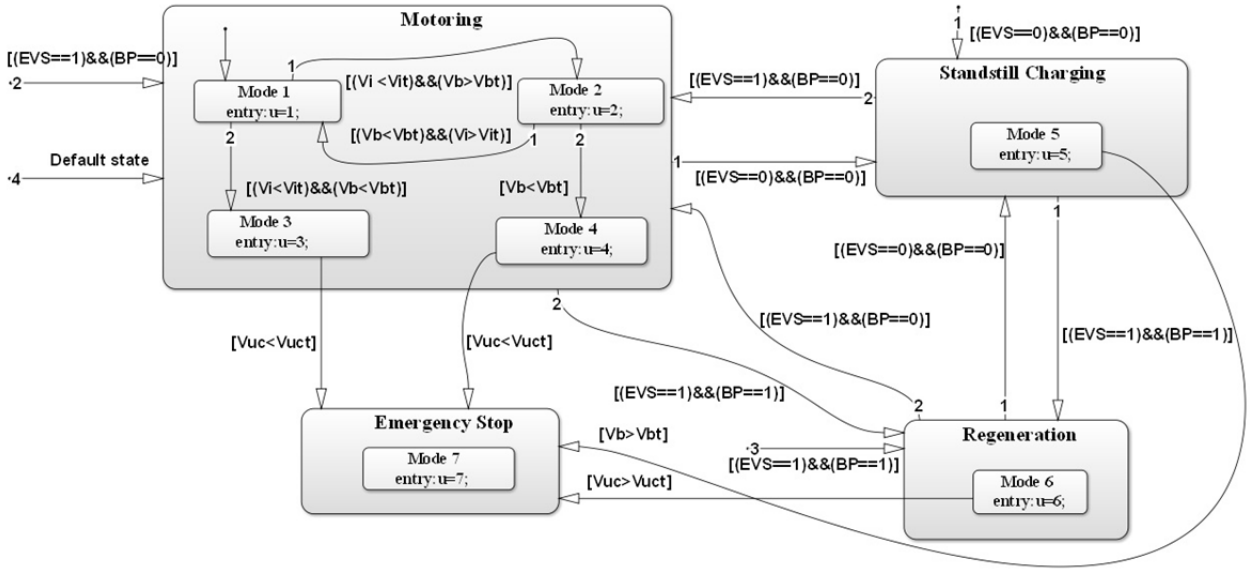


Fig. 10. State-flow diagram for mode selection.

TABLE III
VARIABLES USED IN STATEFLOW CHART

Variable Name	Description
V_i	Primary source voltage
V_b	Primary storage voltage
V_{uc}	Secondary storage voltage
V_{it}	Primary source threshold voltage
V_{bt}	Primary storage threshold voltage
V_{uct}	Secondary storage threshold voltage
EVS	Power Switch Position(on/off)
BP	Regeneration Switch Position(on/off)

acquired and monitored. When the voltage level of V_i falls below the lower threshold voltage ($V_i < V_{it}$) and the primary storage voltage is higher ($V_b > V_{bt}$), the state is changed from Mode 1 to Mode 2. Once the system enters Mode 2, it can either move on to Mode 4 when ($V_b < V_{bt}$) or it can return to Mode 1 ($V_i > V_{it}$). Upon entering the corresponding state, it communicates with the controller and commands a mode transition. Mode 4 is initiated when the battery voltage falls below a threshold (V_{bt}) and the secondary storage can aid it in supplying the load. If the secondary storage falls below a certain threshold ($V_{uc} < V_{uct}$), the emergency stop mode is initiated. This mode resets all of the measurements and begins the flowchart from the initial state. At any point in time, pressing the brake (*BP*=1), will start Mode 6. In the same way, the other state transitions can be understood with the conditions for transition associated with each arrowhead from Fig. 10.

B. Voltage Control Loop

Irrespective of the voltage levels of the source/storage units, the voltage regulator, must ensure a constant voltage delivery to the load. A PI controller is utilized for this purpose. A steady state model of the power converter is used to derive the transfer function in different operating modes. A small-signal model of the proposed converter is necessary to derive the open loop transfer functions. From Mode1 the volt-second balance of the inductor L_1 is:

$$\langle V_{L_1} \rangle_{T_s} = V_i \times d_3 + (V_i - V_0) \times (1 - d_3) \quad (21)$$

The steady state parameters in the linear model are perturbed over a small quiescent point to arrive at the detailed model.

$$\begin{aligned} V_i &= V_i + \hat{v_i} \\ V_0 &= V_0 + \widehat{v_0} \\ d_3 &= d_3 + \widehat{d_3} \\ d_3' &= d_3' + \widehat{d_3'} \end{aligned} \quad (22)$$

Hence, substituting (22) in (21) yields:

$$\begin{aligned} \langle V_{L_1} \rangle_{T_s} = (V_i + \hat{v_i}) \times \left(d_3 + \widehat{d_3}\right) \\ + \left((V_i + \hat{v_i}) - (V_0 + \widehat{v_0})\right) \\ \times \left(d_3' + \widehat{d_3'}\right) \end{aligned} \quad (23)$$

By eliminating the averaged large signal terms and the second order terms, the final equation is derived as:

$$\langle V_{L_1} \rangle_{T_s} = \hat{v_i} + V_0 \times \widehat{d_3} - \widehat{v_0} \times d_3' \quad (24)$$

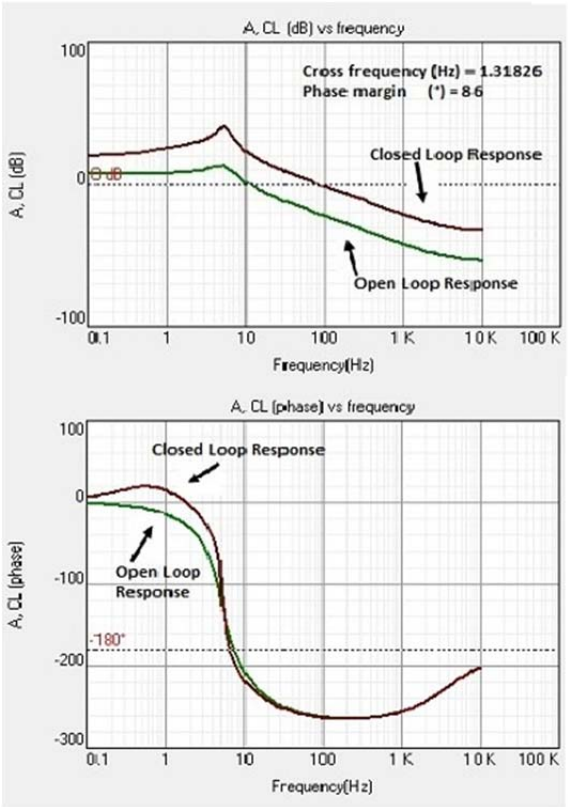
Similarly, the charge-second balance of the output capacitor yields:

$$\langle I_{C_0} \rangle_{T_s} = C_0 \times \frac{dV_0}{dt} = -I_{L_{1\times}} \times \widehat{d_3} + \widehat{i_L} \times d_3' - \frac{\widehat{v_0}}{R} \quad (25)$$

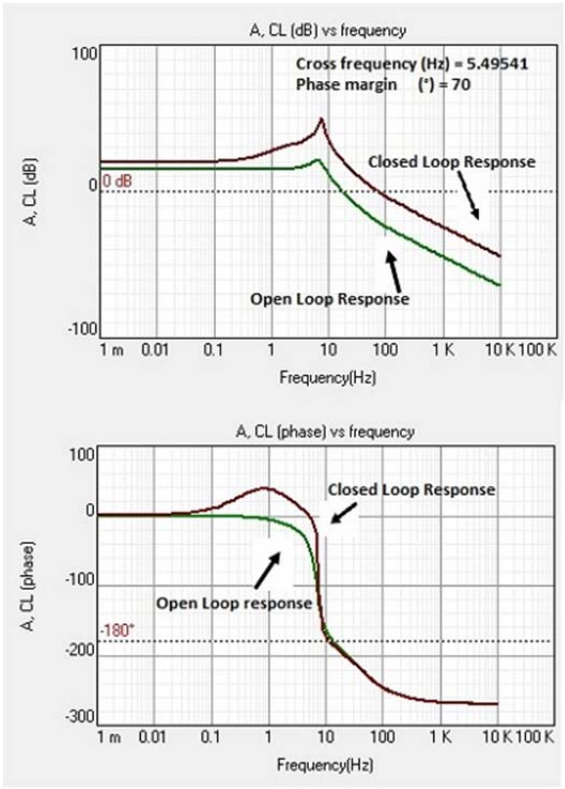
Using the volt-second and charge-second balance equations, the DC transformer model [32] of the converter is ascertained. This is then reduced to two different transfer function namely: the input-to-output (G_{vg}) and control-to-output (G_{vd}) transfer functions. A Bode plot of the open loop transfer function is plotted. The different transfer functions and their stabilities are listed in Table IV. Since the first five modes replicate a Boost converter, the transfer functions are similar to each

TABLE IV
SMALL-SIGNAL TRANSFER FUNCTIONS AND ITS STABILITY

Mode	Input-to-output transfer function (G_{vg})	Control-to-output transfer function(G_{vd})	Stability of G_{vd}
Mode1	$\frac{\frac{1}{1-d_3}}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	$\frac{\frac{V_0}{1-d_3}\left(1-\frac{s\times L_1}{R\times(1-d_3)^2}\right)}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	stable
Mode2	$\frac{\frac{1}{1-d_3}}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	$\frac{\frac{V_0}{1-d_3}\left(1-\frac{s\times L_1}{R\times(1-d_3)^2}\right)}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	stable
Mode3	$\frac{\frac{1}{1-d_4}}{1+s\times\frac{L_1}{(1-d_4)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_4)^2}}$	$\frac{\frac{V_0}{1-d_4}\left(1-\frac{s\times L_1}{R\times(1-d_4)^2}\right)}{1+s\times\frac{L_1}{(1-d_4)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_4)^2}}$	stable
Mode4	$\frac{\frac{1}{1-d_3}}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	$\frac{\frac{V_0}{1-d_3}\left(1-\frac{s\times L_1}{R\times(1-d_3)^2}\right)}{1+s\times\frac{L_1}{(1-d_3)^2\times R}+s^2\times\frac{L_1\times C_0}{(1-d_3)^2}}$	stable
Mode5	$\frac{\frac{1}{1-d_2}}{1+s\times\frac{L_1}{(1-d_2)^2\times R_b}+s^2\times\frac{L_1\times C_1}{(1-d_2)^2}}$	$\frac{\frac{V_i}{1-d_2}\left(1-\frac{s\times L_1}{R_b\times(1-d_2)^2}\right)}{1+s\times\frac{L_1}{(1-d_2)^2\times R_b}+s^2\times\frac{L_1\times C_1}{(1-d_2)^2}}$	stable
Mode6	$\frac{\frac{-d_5}{1-d_5}}{1+s\times\frac{L_2}{(1-d_5)^2\times R_{uc}}+s^2\times\frac{L_2\times C_2}{(1-d_5)^2}}$	$\frac{\frac{V_0}{d_5\times(1-d_5)^2}\left(1-s\times\frac{d_5\times L_2}{R_{uc}\times(1-d_5)^2}\right)}{1+s\times\frac{L_2}{(1-d_5)^2\times R_{uc}}+s^2\times\frac{L_2\times C_2}{(1-d_5)^2}}$	stable



(a) Mode 1.



(b) Mode 6.

Fig. 11. Simulated Frequency response of Input-to-Output transfer functions.

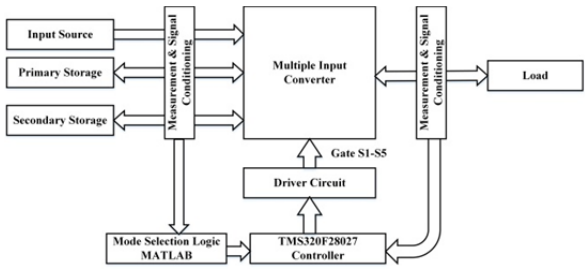


Fig. 12. Block Diagram for Hardware Implementation.

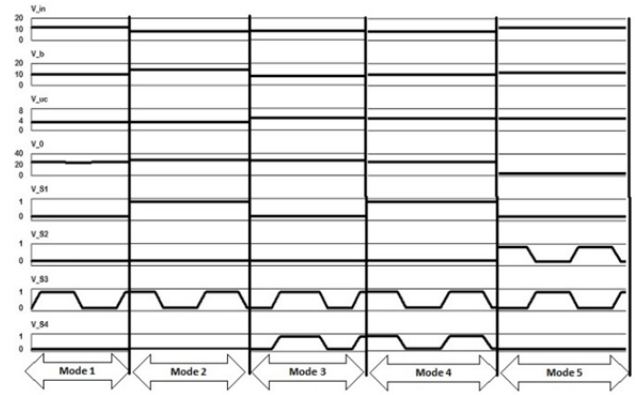


Fig. 13. Simulation Results.

other. The behavior of Mode 6 resembles a Buck-Boost converter. Since first five Input-to-Output transfer functions are behaviorally identical, the Bode plots of G_{vg} in Mode 1 to Mode 5 are similar. The theoretical frequency response is simulated with SmartCtrl tool and its results with the open loop and closed loop responses are shown in Fig. 11. With the open loop transfer function model, the closed loop controller constants K_p=0.104117 and K_i =0.0334486 were obtained.

V. Hardware Implementation

Details of the hardware components for the proposed four port converter are presented in this section. The primary source is a solar panel with a Maximum Power Point (MPP) controller that is capable of generating 200W. The gate pulse for the switching device S_3 is obtained from the MPP controller when the solar panel supplies energy to the load. An overall block diagram of the converter for hardware implementation is shown in Fig. 12. A 14V, 5Ah battery is deployed as a primary storage unit. Two ultracapacitors with 2.7V, 50F ratings, are connected in series and utilized as the secondary storage unit. A laboratory-level prototype was built to verify the feasibility of the converter. The mode selection logic is implemented using MATLAB Stateflow and the PI controller is implemented using a TMS320F28027 controller. The voltage level of the source and storage ports are measured and used as inputs for the automatic mode selection using MATLAB Stateflow while the measured converter output voltage is fed into the controller for voltage regulation.

TABLE V
Details of Hardware Elements

Topology	Non-Isolated
Controller	TMS320F28027
Primary source	Solar panel (12V, 200W_p)
Primary storage	Battery (14V, 5Ah)
Secondary storage	Ultracapacitor (2.7V,50F each)
MOSFET	IRFP250N
Diode	1N5822
C_0	100μF
L_1	200μH
L_2	49mH
Inductor core	T50-75-TAF200
MOSFET driver	TC4422/TC4432
Optocoupler	6N317
Switching frequency	20kHz

The inductor and capacitors were chosen based on the equations of the volt-second and charge-second balance.

$$L_1 = \frac{V_i \times (V_0 - V_i)}{\Delta i_{L_1} \times f_s \times V_0} \quad (26)$$

where, ΔiL1 is the current ripple, and fs is the switching frequency. This equation applies to Mode 1. Since the same inductor works across all five modes, a maximum value of the inductor is chosen for the hardware. The output voltage requirement of the other modes is adjusted by varying the duty cycle of the corresponding switches. In the same way, the output capacitance value is calculated by the following equation:

$$C_0 = \frac{I_0 \times d_3}{\Delta V_0 \times f_s} \quad (27)$$

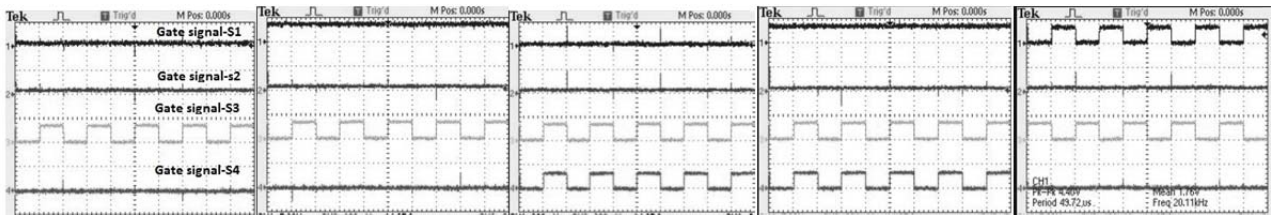
where, ΔV_0 is the output voltage ripple. The value of the inductor L_2 is calculated by the following equation:

$$L_2 = \frac{V_0 \times (V_{uc} - V_0)}{\Delta i_{L_2} \times f_s \times V_{uc}} \quad (28)$$

The details of the hardware are listed in Table V. For experimental verification, the converter is loaded with a rheostat.

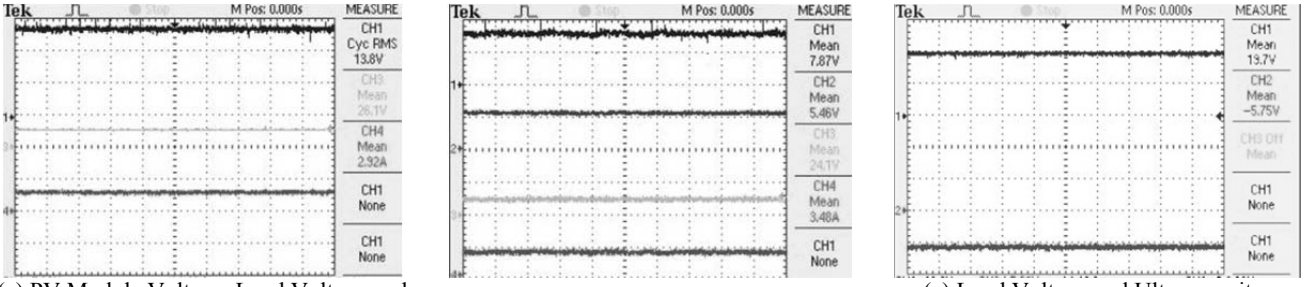
VI. Results and Discussion

This section presents the results obtained from both the simulation and experimental verification of the proposed four port converter. Each mode is simulated separately with a PI controller to test its feasibility. As discussed earlier, the first five modes exhibit the behavior of a Boost converter. Out of these five modes, Modes 1, 2 and 5 are single source modes, in which only one source will be utilized. Modes 3 and 4 utilizes two different sources simultaneously. The simulation results are shown in Fig. 13. The working of the mode selection logic is tested with different voltage ranges and the gate signals of the switching signals S_1-S_4 for the different modes are shown in Fig. 14. The active gate pulses corresponding to each mode can be found in Table II. The



(a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

Fig. 14. Mode Selection Logic and its Gate Pulse Pattern.

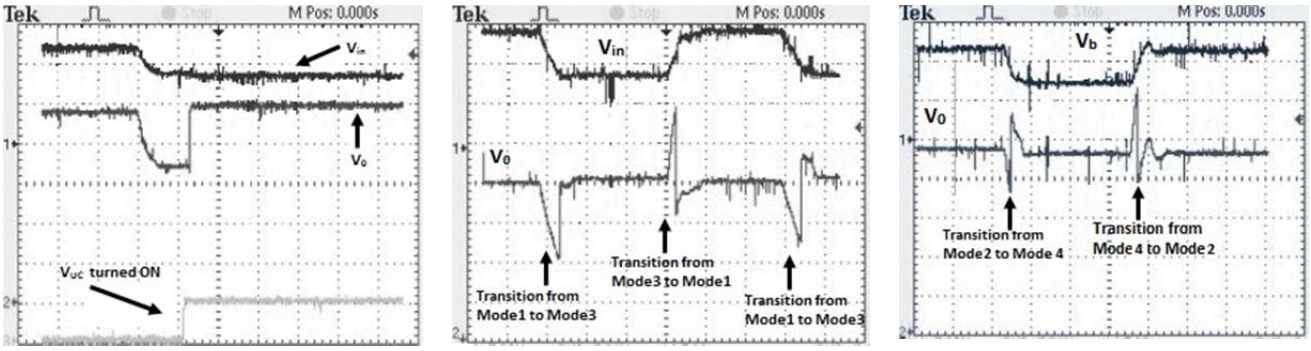


(a) PV Module Voltage, Load Voltage and Load Current in Mode 1.

(b) PV Module Voltage, Ultracapacitor Voltage, Load Voltage and Load Current in Mode 3.

(c) Load Voltage and Ultracapacitor Voltage in Mode 6.

Fig. 15. Steady State Waveforms.



(a) Mode 1 to Mode 3 transitory waveforms.

(b) Multi mode transition.

(c) Mode 2 to Mode 4 transitory waveforms.

Fig. 16. Mode Transition Waveforms.

output of Mode 1 with the primary source voltage V_i on CH1, the output voltage V_0 on CH3, and the output current I_0 on CH4 is shown in Fig. 15(a). Similarly, the output waveforms of Mode 3 with the primary source voltage V_i on CH1, the secondary storage voltage V_{uc} on CH2, the output voltage V_0 on CH3, and the output current I_0 on CH4 is shown in Fig. 15(b). The waveforms of Mode 6 in the steady state with the load voltage on CH1 and the ultracapacitor voltage on CH2 is shown in Fig. 15(c). The various mode transient waveforms are shown in Fig.16. The significant waveforms for the transition from Mode1 to Mode3 are shown in Fig. 16(a). The PV panel voltage is reduced to below the threshold by shading, and the transition waveforms are obtained. As shown in Fig. 10, once V_i increases above its threshold level ($V_i > V_{it}$), the system will return to Mode 1 as shown in Fig. 16(b). The prevailing condition of the battery in the single and hybrid modes and its transition are shown in Fig. 16(c). The primary source threshold voltage V_{it} has been set as 9V. When the primary source voltage drops below its threshold voltage, Mode 3 is invoked where both the primary source and primary storage ports deliver power to the load port. Irrespective of the voltage levels of the source or storage ports, a near constant value is achieved on the load port.

VII. CONCLUSION

This paper proposes a four port DC/DC converter with an input port, two storage ports and a load port. The synthesis of the proposed converter, the switch realization, and the steady state analysis of all of the significant operating modes are presented. A competitive mode selection logic with a PI controller for voltage regulation is proposed. The system utilizes different combinations of sources and storage units depending upon the mode initiated. The results indicate that

the inductor can be used as a buffer to hybridize power sources. Instead of completely ignoring the source/storage units and shifting to an alternative source, the hybrid usage of sources provides an attractive way of utilizing low power sources in combination with high power sources. The feasibility of the converter is tested with different modes and it is suitable for automotive applications.

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