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Output Noise Reduction Technique Based on Frequency Hopping in a DC-DC Converter for BLE Applications

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***Abstract*:** In this paper, a different type of pulse width modulation (PWM) control scheme for a buck converter is introduced. The proposed buck converter uses PWM with frequency hopping and a low quiescent–current low dropout (LDO) voltage regulator with a power supply rejection ratio enhancer to reduce high spurs, harmonics and output voltage ripples. The low quiescent–current LDO voltage regulator is not described in this paper. A three-bit binary-to-thermometer decoder scheme and voltage ripple controller (VRC) is implemented to achieve low voltage ripple less than 3mV to increase the efficiency of the buck converter. An internal clock that is synchronized to the internal switching frequency is used to set the hopping rate. A center frequency of 2.5MHz was chosen because of the bluetooth low energy (BLE) application. This proposed DC-DC buck converter is available for low-current noise-sensitive loads such as BLE and radio frequency loads in portable communications devices. Thus, a high-efficiency and low-voltage ripple is required. This results in a less than 2% drop in the regulator's efficiency, and a less than 3mV voltage ripple, with -26 dBm peak spur reduction operating in the buck converter.

***Keywords*:** Buck converter, Frequency hopping, Thermometer decoder, Pulse width modulation, Spurious noise

1. Introduction

DC-DC converters are widely used for generating low-voltage power supply applications, such as analog and radio frequency circuits. However, pulse width modulation (PWM) in a DC-DC buck converter creates switching noise and voltage ripple. PWM is usually a square wave with a constant frequency (f_c) and variable duty cycle ($D = t_{on}/T$), as explained by Balcells et al. [1]. Because of these, the most serious interference and cross-mixing with electric circuits are at the fundamental switching frequency and its harmonics. Thus, control sawtooth wave signals having a spectrum with lower peak amplitude than the conventional constant frequency square signal are used to reduce main interference. There are many methods to reduce output noise, such as a spread spectrum clock generator (SSCG) [1], sigma delta modulation (SDM) [2], frequency hopping [3], frequency stepping [9] and a pseudo-noise coded constant off time (PNC-COT) controlled switching regulator (SWR) [8] have already been introduced. However, a frequency hopping technique would seem to be the best candidate for spur reduction. Thus, this paper proposes a DC-DC converter using frequency hopping with a thermometer decoder (FHTD) to reduce output noise and current consumption for high-performance radio frequency circuits. Fig. 1 shows the proposed DC-DC buck converter top block diagram composed of an internal low dropout (LDO) voltage regulator, a compensation circuit, band gap reference (BGR), soft start, a sawtooth generator, dead time generator, gate driver and dead time generator. The level shifter and gate driver get power from a lithium-ion battery, 2.2V~5V. Other circuits use 1.2V (V_{DCIN}) generated from an internal LDO voltage regulator. So a level shifter is mandatory to increase the voltage to the V_{OUT} level. BGR and soft start are temporarily used while the circuit is not saturated. A dead time generator is very efficiency at reducing leakage current and improving the efficiency of the DC-DC converter by generating a non-overlap pulse. A sawooth generator is a switching regulator to control M_0

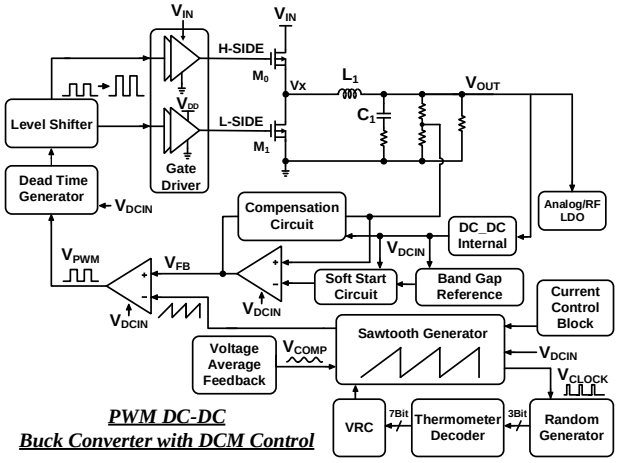

Fig. 1. Top block diagram of a PWM-controlled buck converter.

(PMOS) and M_1 (NMOS). It affects the switching frequency. This paper controls the switching frequency using frequency hopping and a thermometer decoder.

2. Frequency Hopping with Thermometer Decoder

The general buck converter suffers from switching noise, which appears as spurs and harmonics due to the periodic switching of the buck converter. Therefore, the use of frequency hopping with thermometer decoder control to reduce spurs in the output spectrum of the buck converter is explained using the conceptual implementation shown in Fig. 2. The source current IF is used to charge sawtooth generator capacitance C_{SAW}, while a much larger sink current, I_{SAW}, is used to discharge it. A sawtooth generator, two comparators, an SR latch and two reference voltages from voltage average feedback, V_{COMPH} and $V_{COMPL,}$ are used to generate V_{CLOCK}, which indicates the charging and discharging points of M_2(PMOS) and M_3(NMOS). V_{CLOCK} goes to a random generator to make three-bit random code (P<2:0>). If a period of the random code is quite short, the switching frequency will create more sub-harmonics. Therefore, a long period code is mandatory. The thermometer decoder extends the code to seven bits (T<6:0>). Theoretically, the magnitude of each spur is reduced by a factor of 1/hopping rate, or 20x log (hopping rate) dB from the single frequency. This proposed frequency hopping employs eight hopping frequencies, as illustrated in Fig. 3. This is the maximum, because 16 hopping frequencies does not follow the equation 20 x log 16 ≠ 24dB, which results in 19.4dB. The 16 hopping frequencies occupy a large area and generate high glitches on output for the fast hopping rate. Therefore, we use eight frequencies between 2MHz and 3MHz to avoid operation frequency interference in the block linear equalizer (BLE) application. The main frequency, $f_{c,}$ was set to 2.5MHz (450ns), spacing the frequencies 125KHz (80ns) apart. This achieves an 18dB reduction in output spurs compared to the traditional single-frequency scenario, and significantly suppresses maximum spur and harmonics without the cost of increasing the capacitance (C_1) or inductance (L_1) of the buck output LC filter. On the other hand, the noise floor is slightly increased to spread the spectrum over the harmonics. Changing the switching frequency disturbs the steady-state duty cycle of the converter. It causes pulse swallowing or significant instantaneous error in the duty cycle. So, to avoid these problems, synchronization between the hopping rate and internal switching frequencies of the converter must be ensured, such that hopping always takes place at the end of the hopping clock in order to maintain the same steady-state switching duty cycle. Thus, hopping from one frequency to another only occurs exactly at the end of the hopping rate for one frequency and at the beginning of the

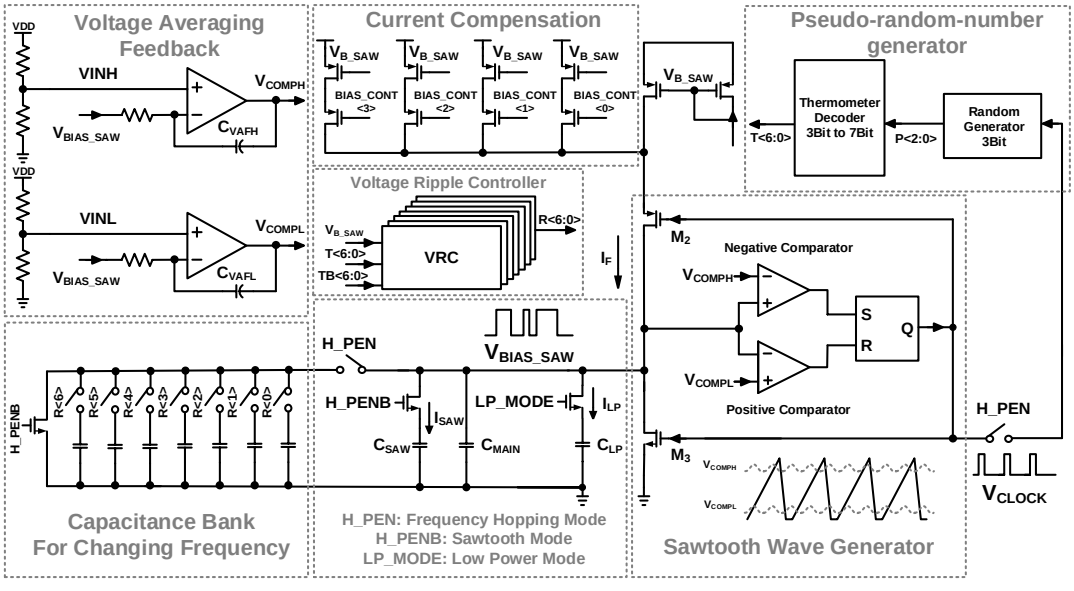

Fig. 2. The implementation of Frequency hopping with thermometer decoder.

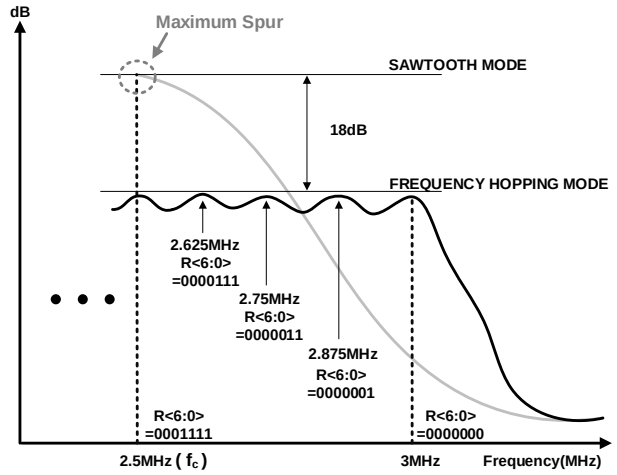

Fig. 3. Spectral analysis of a frequency hopped regulator with eight hopping frequencies.

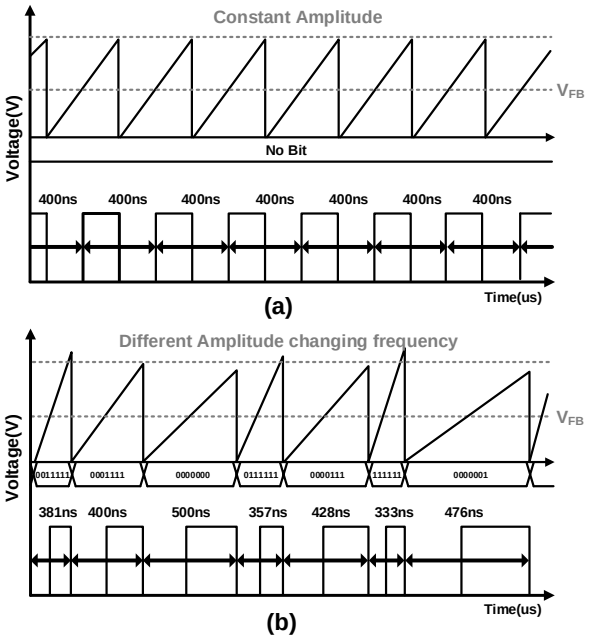

Fig. 4. Pulse-width modulated square wave output (a) Sawtooth mode, (b) FHTD mode.

hopping clock of the next frequency. However, V_{BIAS_SAW} amplitude is not kept constant, because the charging and discharging current, I_F, is fixed, as illustrated in Figs. 4(a) and (b), and is determined only by the reference voltages V_{COMPH} and V_{COMPL}. It reduces buck converter efficiency a little. Figs. 4 and 5 show comparisons of the sawtooth mode and frequency hopping mode. Fig. 4 uses the time domain to compare the two modes' switching on H_PEN or H_PENB to show how much the pulse duty differs. The pulse duty of the sawtooth mode is always constant from using a single frequency. On the other hand, eight different pulse duties at frequencies from 2MHz(500ns) ~ 3MHz (333ns) randomly operate. Output voltage distribution of sawtooth mode and frequency hopping mode were implemented for Fig. 5. The output voltage ripple is mainly affected by the frequency and inductor current. The

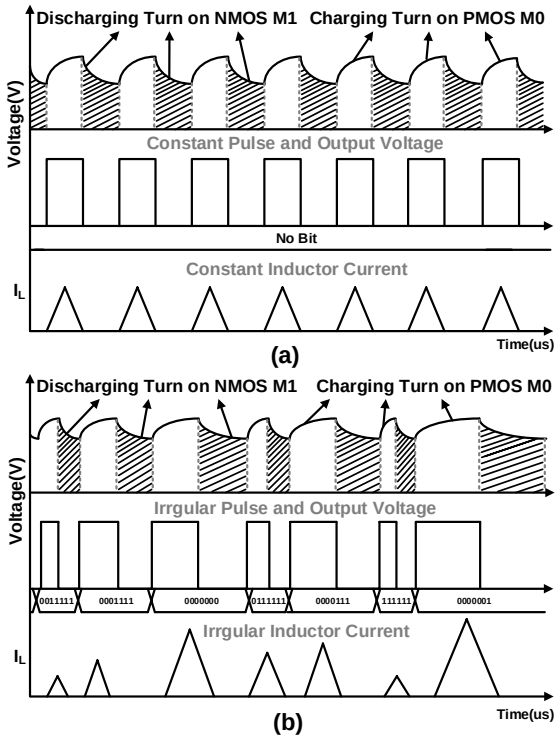

Fig. 5. The output ripple voltage wave from (a) Sawtooth mode, (b) FHTD mode.

inductor current ripples abruptly on switching frequency hops. The variation in the current ripple passes through the LC output filter and results in transient glitches in the output voltage for several switching periods. The transient glitches are generated whenever the switching frequency hops to control M_O and M_1, with each MOS located in front of L_1 and C_1. When PWM output pulse is low, NMOS M_1 is turned on, so that L_1 and C_1 start charging, which increases the voltage level. Then, the PWM pulse goes up, PMOS M_0 is turned off, NMOS is turned on, and L_1 and C_1 are discharged. Figs. 5(a) and (b) show the mechanisms of sawtooth mode and FHTD mode. Sawtooth mode has constant pulse width to make a half-duty cycle, so that charging and discharging times are equal. It generates the same voltage ripple in the output voltage. However, FHTD mode changes the pulse duty all the time and has irregular output voltage ripple from shifting frequency by frequency hopping. This voltage ripple in the frequency domain at 2~3MHz seems small, but the transient voltage ripples are larger in the time domain. It degrades modulation accuracy. Thus, the voltage ripple controller (VRC) is adapted to reduce glitches.

The proposed VRC [6] is composed of an RC filter and a transmission gate. The VRC input signal is based on the seven bits from the three-bit binary-to-thermometer decoder, and others that are inverted. It triggers seven-bit signals to smoothly control transmission gates in front of switching capacitance, in order to hold the voltage that controls the converter's switching frequency, and decreases the output voltage ripple by about 10%~20%. The waveforms in Fig. 5 illustrate the results of the output voltage ripple of the buck converter.

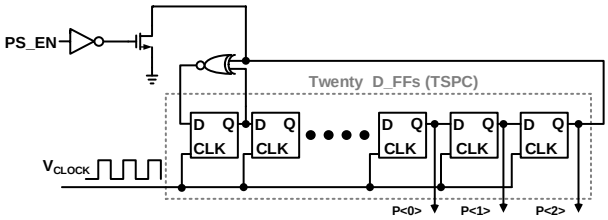

Fig. 6. Pseudo-random-number generator.

2.1 Sawtooth Wave Generator

The sawtooth wave generator is composed of an SR latch and two hysteresis comparators [7]. Output voltage is V_{BIAS_SAW}, switch M_1 turns on when low voltage is applied, and switch M_2 turns on when high voltage is applied. As an initial condition, V_{BIAS_SAW} = 0, output of the pulse comparator is low, and that of negative comparator is high, and the output of the SR latch is low. Because switch M_1 turns on and switch M_2 turns off, capacitor C_{SAW} is charged by current source IF, and the output voltage is founded on VBIAS = (I_F/C_{SAW})*t. When V_{BIAS_SAW} becomes V_{HIGH}, the output of the negative comparator becomes high, and the output of the positive comparator becomes low, so that the output of the SR latch becomes high. Then, switch M_1 turns off, and switch M_2 turns on; charging C_{SAW} is finished, and discharging C_{SAW} starts. The charging/ discharging process is repeated continually until I_F is cut. The sawtooth wave generator creates a single frequency related to current I_F and C_{SAW} sizes through the charging/discharging process.

2.2 Pseudo-Random-Number Generator

A pseudo-random-number generator (PSNR) is used to make three-bit random digital code, as explained by Tao et al. [3]. The PSNR is basically a set of shift registers connected in series, with the output of some of the shift registers combined in an exclusive-OR configuration to provide a feedback mechanism. When the input of the register is fed with a seed value, and the PSNR is clocked, it generates a pseudo-random pattern of 1's and 0's. The clock comes from the output of the SR latch. Fig. 6 shows a 20-stage PSNR. A 20-stage shift resister can produce maximal code with a length of $2^{20} - 1$ = 1,048,575 bits. This is large enough for the sequence to appear random. To eliminate the PSNR, the PS_EN signal is used during startup to set the output of last flip-flop to 0, and then release it afterwards [3]. The three-bit random code created by the PSNR goes to the thermometer decoder.

2.3 Three-bit Binary-to-Thermometer Decoder

The three-to-seven–bit binary-to-thermometer decoder implemented in frequency hopping is shown in Fig. 7. The three-bit binary code is decoded to digital thermometer code in order to reduce glitches. The control logic of the switches causes voltage spikes and affects the output

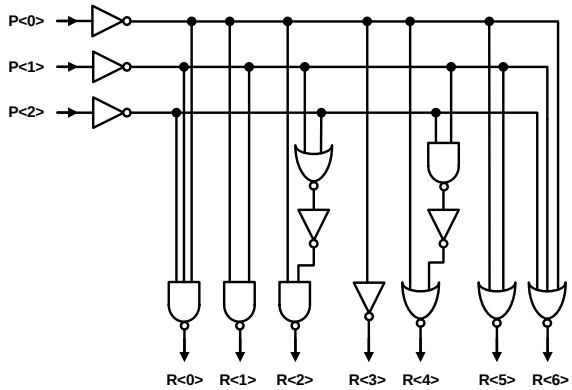

Fig. 7. Three-bit binary-to-thermometer decoder.

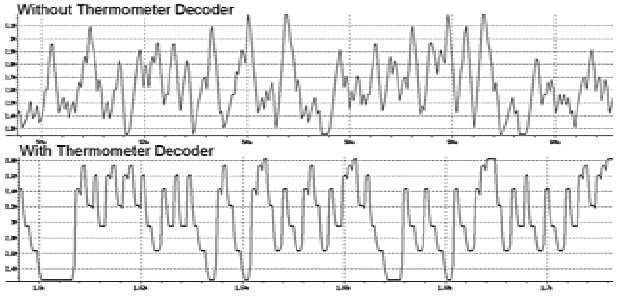

Fig. 8. Time-domain representation of the change-frequency operation.

voltage ripple of the buck converter. The three-to-seven–bit binary-to-thermometer decoder has better performance and less voltage ripple, compared with a three-to-eight–bit decoder and a gray code decoder. Because the converters are based on thermometer decoder code, they promise to be monotonic and do not change seven-bit code without changing MSB to LSB. The seven-bit code immediately controls capacitance bank switches in front of capacitance to vary the frequency, and maximizes the hopping rate so it is as fast as the regulator's switching frequencies when a PEN switch is turned on. In order to change frequency, the thermometer decoder spaces the frequencies at 125KHz (80ns) apart, and turns a transmission gate on or off through the VRC. If PSNR code goes directly to the control transmission gate, it generates change from MSB to LSB frequently, compared to using a thermometer decoder. This is illustrated in Fig. 8. Using a thermometer decoder is a better process than others. It more smoothly changes the frequency in the time domain, and does not frequently generate glitches.

2.4 Voltage Averaging Feedback (VAF)

Voltage averaging feedback (VAF) is used to reduce flicker noise [4]. Flicker noise mainly comes from comparators that are in the sawtooth wave generator. The basic solution to efficiently reduce flicker noise is enlarging the size of transistors that impact noise. However, the large size of the gate increases the ratio of gate parasitic capacitors and increases current consumption.

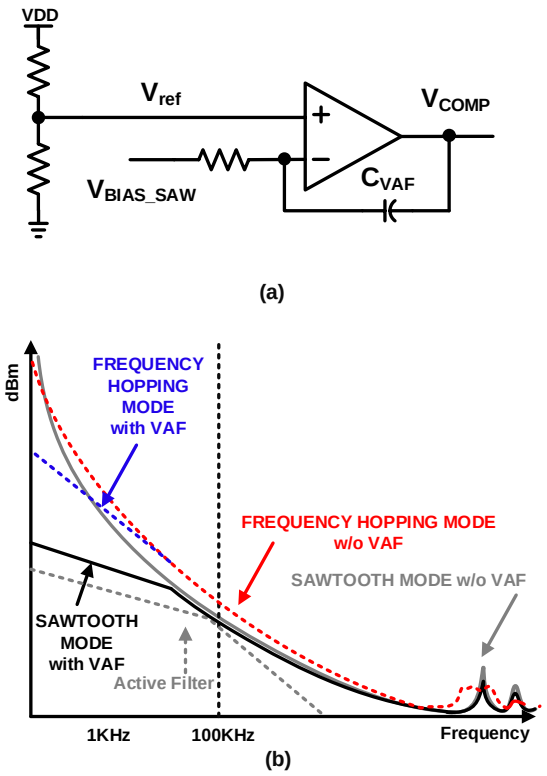

Fig. 9. Voltage averaging feedback (a) structure, (b) VAF operation in the power module.

This does not match our motivation for low current consumption. Thus, the structure in Fig. 9(a) considers the dominant noise source first, and noise generated from the active filter in the VAF loop and the phase noise from the sawtooth wave generator second. The total phase noise is a summation of thermal noise applied in the closed loop transfer function. This function changes voltage to phase, phase to frequency, and frequency to averaged voltage, as explained by Tokunaga et al. [4]. Each VAF and sawtooth wave generator is operated as a low pass filter and a high pass filter for phase noise and summation phase noise [4]. The amplifier in Fig. 9(a) is used by the rail-to-rail amplifier to get enough phase margin. VAF is constantly fed by V_{BIAS_SAW}. V_{ref} and V_{BIAS_SAW} are virtually shorted in a low-frequency domain defined by time constants R_{VAF} and C_{VAF}. Fig. 9(b) is the result of the phase noise spectrum at V_{COMP}. It means that phase noise at a low offset frequency is dominated by the VAF. This affects low frequencies below 100KHz because of active filtering. However, spurious noise is dominated by switching frequency changing current or capacitance in the signal generator. Thus, VAF is hardly affected in the buck output spectrum. Nevertheless, it helps the BLE application because the most important frequency band in the BLE application is below 1MHz. Therefore, low noise in the low-frequency domain is the dominant area.

3. Experimental Result

The measured result and layout for FHTD are implemented in this section. Fig. 10 shows the top layout of the buck converter, and Table 1 compares the converter's key parameters in the buck converter. The total active area, including pads, is 1900 * 1400 μm2 with FHTD. FHTD is a relatively small part of the whole process. Only 10% of this area is consumed by the additional circuitry required to implement the FHTD scheme. The DC-DC buck converter is measured using power supply and an oscilloscope, with the SPI PC, electric load generator and digital multi-meter. Fig. 11 shows how to make the measurement environment. The single switching frequency of 2.5MHz, which is sawtooth mode, is implemented, and changing switching frequency from 2MHz to 3MHz, which is the FHTD, is also implemented. Frequency hopping uses eight frequencies to spread the spectrum by spacing frequencies at 125KHz, chosen to maximize the spread and avoid the BLE application operation point. It reduces spurious noise up to -64dBm. All measurements were made at 1.7V output (VOUT) and 1~20mA load current. The output spectrum of the regulator was measured using a real-time spectrum analyzer with a resolution bandwidth of 500MHz. The output spectrum shows up to 20MHz in sawtooth mode and FHTD mode. Fig. 12 shows the output spectrum of DC-DC out (Vout) in sawtooth mode. The maximum spur

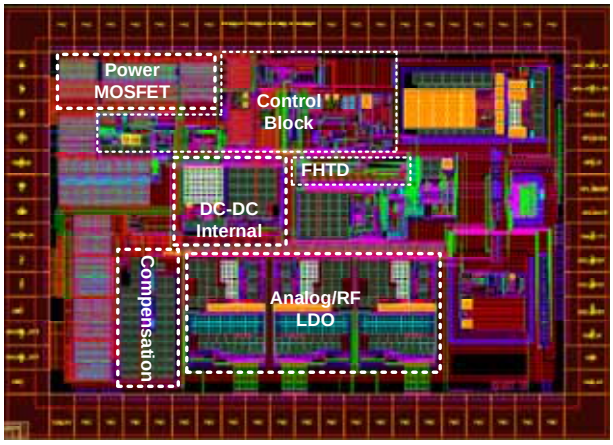

Fig. 10. Top Layout of the proposed regulator.

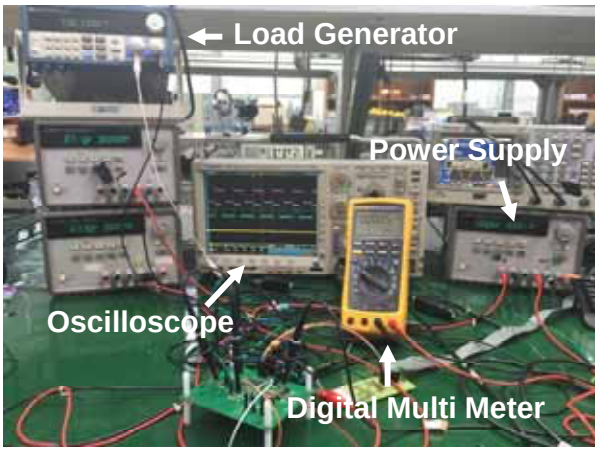

Fig. 11. The performance measurement environment.

Table 1. Comparison of spread spectrum operation in DC-DC switching power modulator.

Parameters	This Work	[9]	[3]	[8]	[2]	[1]
Technology	0.13 μm	0.18 μm	0.35 μm	40 nm	0.35 μm	N/A
Control Methodology	PWM+Frequency hopping &Thermometer decoder +LDO with PSR enhancer	Frequency Stepping	PWM+Frequency hopping & phase chopping	PNT-COT controlled SWR with SSFC	3rd CT-Sigma Delta Mdoulation	SSCG
Spread Spectrum Operation	Hard Switching	Hard Swiching	Hard Switching	Soft Switching	Soft Switching	Hard Switching
Number of Frequencies	8	64	8	N/A	N/A	N/A
Switching Frequney (MHz)	2~3	2.2~4.4	3~6.5	0.5~8	8	0.1~1
Output voltage ripple	2.2~3.4 mV	N/A	N/A	35 mV	Below 17 mV	N/A
Peak Noise Floor	-64dBm/Hz	-56dBm/Hz	-90dBm/Hz	-72dBm/Hz	-53.2dBm/Hz	N/A
Active area	320*120 μm 2	250*100 μm 2	0.36 ㎟	680*700 μm 2	1.4 ㎟	N/A
DC-DC efficiency	86%	92%	N/A	92%	78~92%	N/A

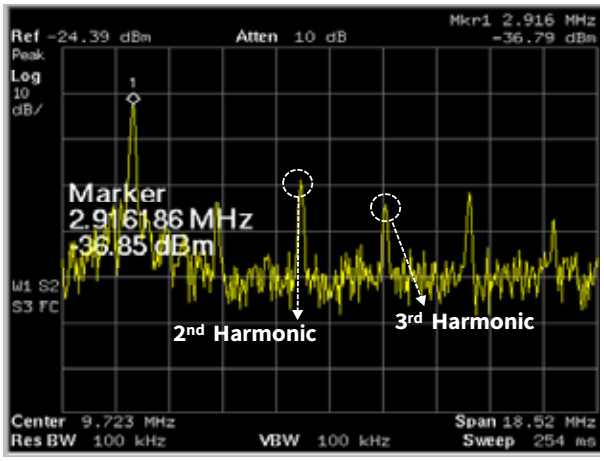

Fig. 12. The DC-DC output spectrum measured

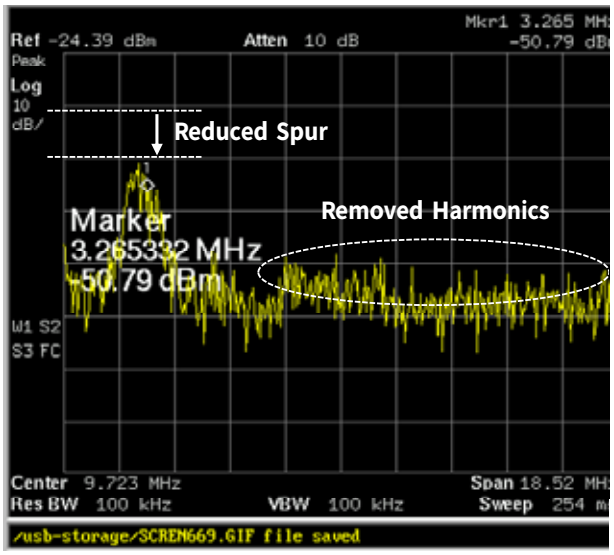

Fig. 13. The DC-DC output spectrum measured result in FHTD mode

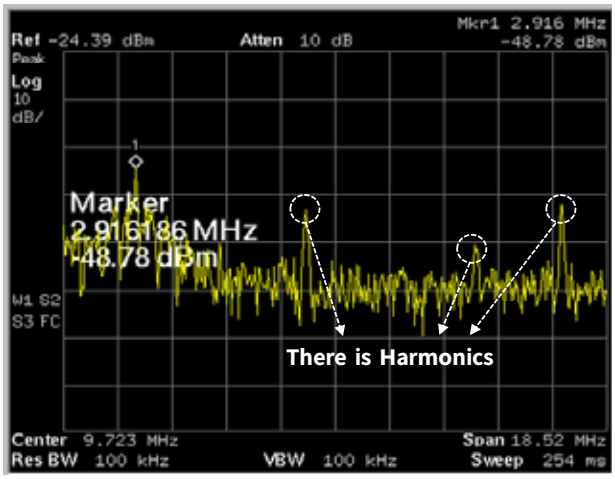

Fig. 14. The LDO voltage regulator output spectrum's measured result in sawtooth mode

is -36dBm, and there are second and third harmonics. FHTD mode is shown in Fig. 13 using eight frequencies.

The harmonics were removed, but increasing the noise floor was affected by spread spectrum. Average reduced spur is almost 15~16dBm. There is a difference between the theoretical value and the measured value due to parasitic capacitance and resistance in a bond wire. LDO with PSR enhancement, which is not presented in this paper, affects spurious noise degradation by almost 12dBm, adjusting the enhancer frequency at 2.5MHz. Figs. 14 and 15 show the results of each mode.

The output spectrum of the LDO voltage regulator reduces spurs and the noise floor. The total output noise reduction is an almost 26dBm degradation. Operated hopping to the frequency worsens the output voltage ripple. Output voltage ripple was already shown in Fig. 5, and output voltage ripple is consistently at 3mV in sawtooth mode, whereas it varies between 2.2mV and 3.4mV in FHTD mode. It is very important to note that hopping between one switching frequency to another does not

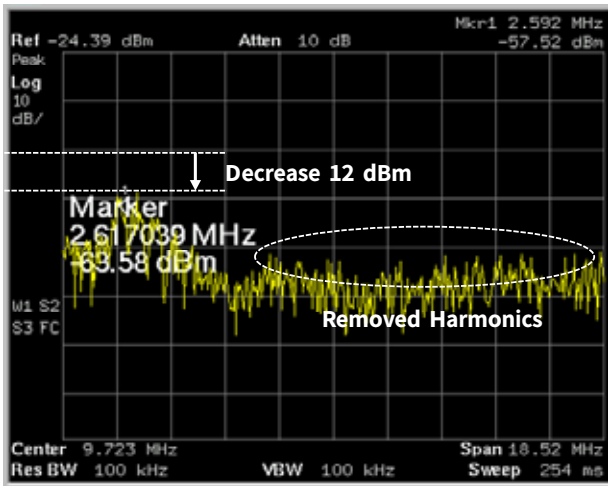

Fig. 15. The LDO voltage regulator output spectrum's measured result in FHTD mode

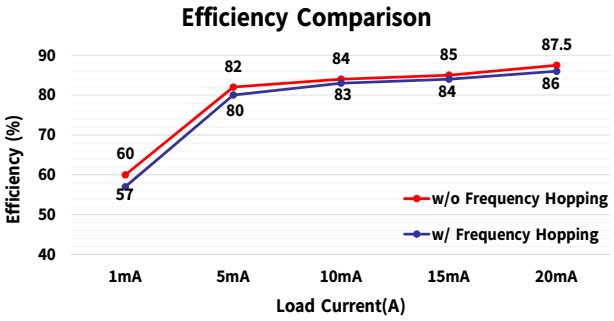

Fig. 16. The efficiency of the DC-DC buck converter with FHTP or without FHTP

produce large transients in buck output [5]. This ripple loss reduces the efficiency of the buck converter by less than 2% in Fig. 16. Each load current creates different efficiencies. The highest efficiency of the DC-DC converter is at 20mA load current.

4. Conclusion

In this paper, the proposed buck converter, combining frequency hopping with a thermometer decoder in 0.13 CMOS technology with a 3.3V Li-ion battery and a 1.2V internal LDO voltage regulator supply voltage is fully analyzed and implemented. The buck converter uses synchronous frequency hopping with eight hopping frequencies to achieve up to -26dB reduction in output spurs with a 125KHz hopping rate. It is a very attractive circuit for designing generic low-noise power supplies for spur-sensitive loads, as well as for loads that are sensitive to the random noise floor without post-line regulation, extra passive filtering, or customization for each load [3]. It occupies 10% of the overall system area and consumes just 20uA. Besides, the overall efficiency of the buck converter is not sacrificed much below 1.1%. This circuit is more useful than others [1-3, 8, 9]. Additionally, it is easily incorporated with an already existing PWM controller by adding a pseudo-random-number generator and capacitance bank.

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