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A Single-Ended ADC with Split Dual-Capacitive-Array for Multi-Channel Systems

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Abstract—**This paper presents a power and area efficient SAR ADC for multi-channel near threshold-voltage (NTV) applications such as neural recording systems. This work proposes a split dual-capacitive-array (S-DCA) structure with shifted input range for ultra low-switching energy and architecture of multi-channel single-ended SAR ADC which employs only one comparator. In addition, the proposed ADC has the same amount of equivalent capacitance at two comparator inputs, which minimizes the kickback noise. Compared with conventional SAR ADC, this work reduces the total capacitance and switching energy by 84.8% and 91.3%, respectively.**

Index Terms—**Multi channel, Near threshold-voltage (NTV), Analog-to-digital converter (ADC), Digital-to-analog converter (DAC), Successive approximation register (SAR), Split dual-capacitive-array (S-DCA)**

I. INTRODUCTION

As advances in low-power integrated circuits are made, multi-channel applications such as neural signal acquisition systems (ECG, EEG, and EMG) have been widely studied for portable and implantable biomedical devices. In the design of ADCs for these applications, successive-approximation register (SAR) architectures with segmented capacitive array would be the most preferred solution owing to inherent low-power consumption and small area compared with other type ADCs [1-5].

One of the previous segmented SAR architectures [1] reduces the switching energy in capacitive array, however higher sampling operations and larger area are required for analog front-ends (AFEs) as the number of channels increases due to the use of a single sample-and-hold (S/H) circuit. The architecture using analog multiplexing scheme [2] adopts 2-branch pipelined S/H to reduce the sampling frequency of the AFEs, which needs additional large S/H capacitor. Another approach for reducing the burden of the AFEs is the digital multiplexing scheme [3] that uses dedicated S/H for each channel. Because the required number of comparators is proportionally increased as the number of channels increases, offset mismatches among multiple comparators is problematic for better linearity in [3]. In addition, the kickback noise of segmented SAR architectures [1-3] causes linearity performance degradation since the load capacitances at two comparator inputs are different. Another segmented SAR architecture is the split capacitor array scheme with attenuation capacitors, which can be applied to both a single-ended and a differential-input SAR ADC [4]. Even though the attenuation capacitors are additionally split to decrease the switching energy, linearity performance is also degraded due to their mismatches.

In this paper, a single-ended SAR ADC by using split dual-capacitive-array (S-DCA) with shifted input range for multi-channel NTV systems is proposed. This work

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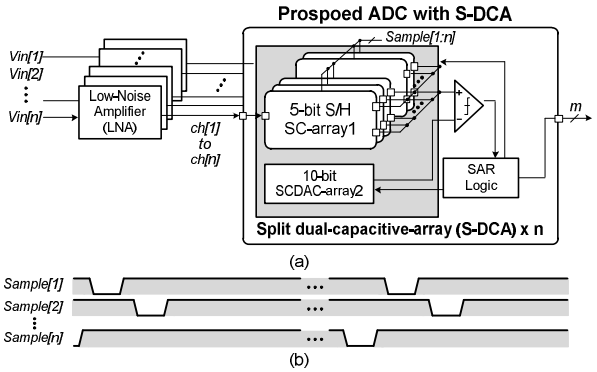

Fig. 1. (a) Block diagram of conventional multi-channel architecture for neural recording system, (b) Timing diagram of sampling signals for channel inputs

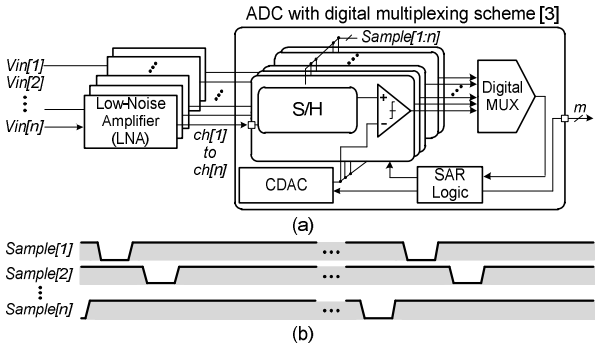

Fig. 2. (a) Block diagram of multi-channel architecture with digital multiplexing scheme [3], (b) Timing diagram of sampling signals for channel inputs

has several advantages: (1) dramatically reduced switching energy by using S-DCA as well as by shifting sampled input voltage, (2) released bandwidth limitation in AFEs, (3) minimized chip size without degradation in performance due to the kickback noise, and (4) enhanced speed of a comparator at near threshold-voltage (NTV) operation because of the aforementioned input-range shifting scheme of sampled input voltage. Compared with the DCA SAR ADC [5], the total capacitance and the switching energy of the proposed ADC can be reduced by 84.8% and 91.3%, respectively. Section II describes the conventional and proposed architectures followed by Section III which shows the circuit descriptions about two representative schemes of this work. Section IV demonstrates simulated results and Section V summarizes the proposed ADC.

II. ARCHITECTURE

Fig. 1(a) shows the block diagrams of conventional architecture for neural recording systems with *n* channels configuration. It is composed of *n* AFEs, an analog multiplexer (MUX) and an *m*-bit ADC. The AFE consists of low-noise amplifier (LNA) and buffer. Because every channel shares only one ADC, the sampling operation is performed sequentially for each channels and the sampling time of each channels is limited by the number of channel. Fig. 1(b) illustrates the timing diagram for each channel samplings with their signals (*Sample[1]*, *Sample[2]* … *Sample[n]*). The sampling operation of ADC is performed for each ADC input (*ch[1]*, *ch[2]*, … , *ch[n]*) in sequential order. Because one ADC can handle as many as 32 channels [1-5], the settling time for ADC is limited in multi-channel systems, which means that the sampling window (the shaded area in Fig. 1(b)) becomes smaller when the number of channel increases. Consequently, both the analog MUX and ADC must be supported by a driving buffer with sufficient bandwidth and slew rate to minimize sampling error in ADC. These buffers consume much higher power consumption than those of front-end amplifiers because of wide bandwidth and high slew rate requirements. This explains the excessive power dissipation for buffers in the conventional multi-channel system.

To overcome this problem, the digital multiplexing scheme [3] is developed by implanting the MUX function in the ADC, thus eliminates analog MUX and associated buffers required in the front-end block of the previously described conventional multi-channel architecture. Fig. 2(a) shows the block diagram of multi-channel system with the digital multiplexing scheme. Because the analog MUX is replaced by digital MUX, this architecture includes only LNA in the front-end circuitry. As shown in Fig. 2(b), the sampling period for each channel input is increased compared with [1]. Although the sampling period is not limited by the number of channels, the ADC reported in [3] requires a dedicated pair of S/H circuit and comparator for each channel, which leads to the large area and the linearity degradation due to offset mismatches among channel-dedicated comparators.

In the proposed ADC architecture, these drawbacks are eliminated in aspect of architecture level. Furthermore, total capacitance and switching energy are

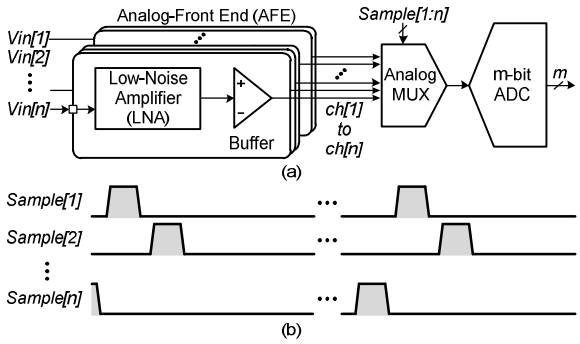

Fig. 3. Block diagram of proposed ADC with S-DCA for multi-channel system

greatly reduced in circuit level. Fig. 3 shows the block diagram of the proposed architecture for multi-channel applications. It is composed of *n* 5-bit S/H split-capacitive arrays (*SC-array1*), a 10-bit split-CDAC array (*SCDAC-array2*), a comparator and SAR logic. The single comparator is shared for the multi channels, which eliminates the offset problems of the digital multiplexing scheme [3]. The 5-bit S/H *SC-array1* are assigned for ADC inputs (*ch[1:n]*) and their outputs are connected to the positive input of the comparator. The 5-bit S/H *SC-array1* plays a role of S/H for each channel input and DAC for upper 5-MSB bits. The 10-bit *SCDAC-array2* plays a role of DAC for lower 5-LSB bits.

III. CIRCUIT DESCRIPTION

The proposed SAR ADC with n-channel formation consists of 10-bit split dual-capacitive-array (**S-DCA**), *n* PMOS switches (M_1), a comparator, and a SAR logic as shown in Fig. 4. The 10-bit **S-DCA** includes *n* 5-bit S/H *SC-array1*s and a 10-bit *SCDAC-array2*. When one channel input is selected, the dedicated 5-bit S/H *SC-array1* is activated and connected to comparator by turning on the M_1 transistor and the other 5-bit S/H *SC-array1*s sample associated channel inputs. After the sampling operation, the sampled input signal is resolved to 5-MSB bits by using the 5-bit S/H *SC-array1*. During the decision of 5-MSB bits, the top-plate of the 10-bit *SCDAC-array2* is set to the V_{REF} by the M_2 transistor. The remained 5-LSB bits are resolved in the 10-bit *SCDAC-array2* with the same manner in the 5-bit S/H *SC-array1*. The proposed **S-DCA** has several advantages and these will be described in the following section.

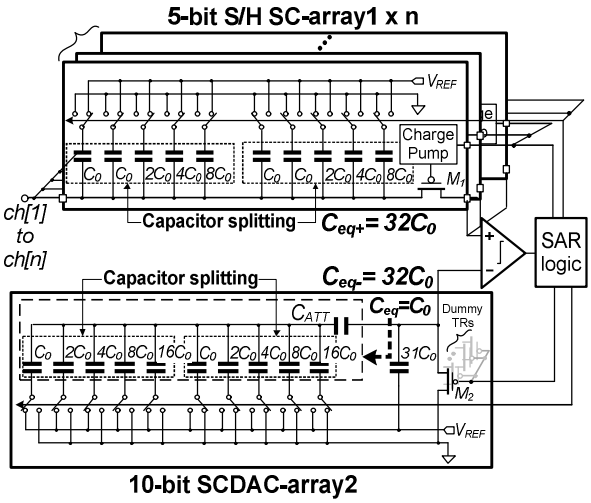

Fig. 4. Block diagram of proposed SAR ADC for multi-channel system

1. Kickback Noise Reduction Scheme

The kickback noise is critical error from dynamic comparator in SAR ADC. When comparator is activated, parasitic capacitances of input transistors in comparator disturb the input voltages of comparator. This fluctuated voltage is accumulated through the conversion-phases and it degrades the linearity of ADC. In case of the DCA structure [5], the capacitances of two capacitive-arrays are different from each other (one array has $32C_0$ and the other array has $1024C_0$), which leads to the different amount of kickback effect to the inputs of comparator. To minimize the kickback noise, the DCA structure uses unit capacitance over 50fF which is relatively larger than the unit capacitance (1.5fF) used in [4]. In the proposed design; however, the capacitances of two capacitive-arrays are same with $32C_0$, which has the same voltage fluctuation to the two capacitive-arrays when comparator is activated. In order to consist of identical amount of capacitive-arrays, this ADC uses the attenuation capacitor (C_{ATT}) to make the equivalent capacitance same in both differential input of comparator. Also, the effect of kickback noise is reduced compared to the DCA structure and its level is same as the differential-input SAR ADC [4]. However, when the number of channel increases, parasitic capacitances of switches for channel selection is dominant and increase the comparator error from kickback noise. To minimize the channel effect, dummy transistors for modeling of channel selection

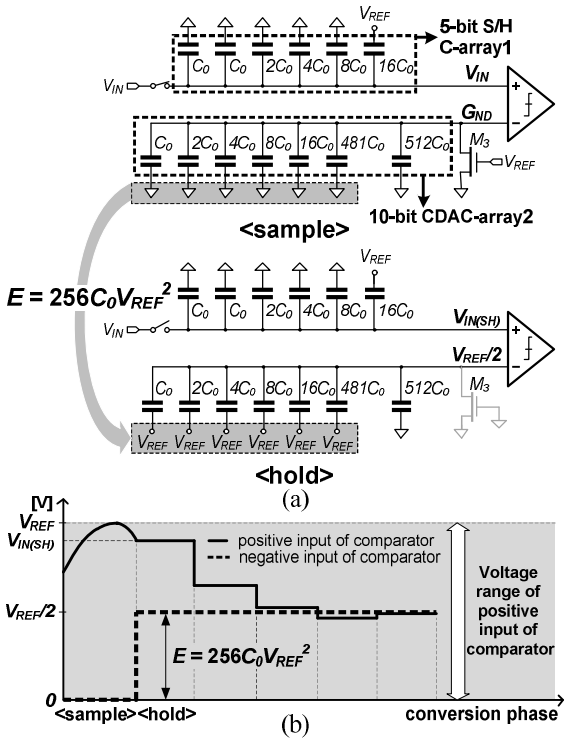

Fig. 5. Block diagram and switching energy generation of 10-bit DCA SAR ADC [5] (a) Block diagrams of the sample and hold operations, (b) Waveform of the comparator inputs (only the upper 5 MSBs are shown)

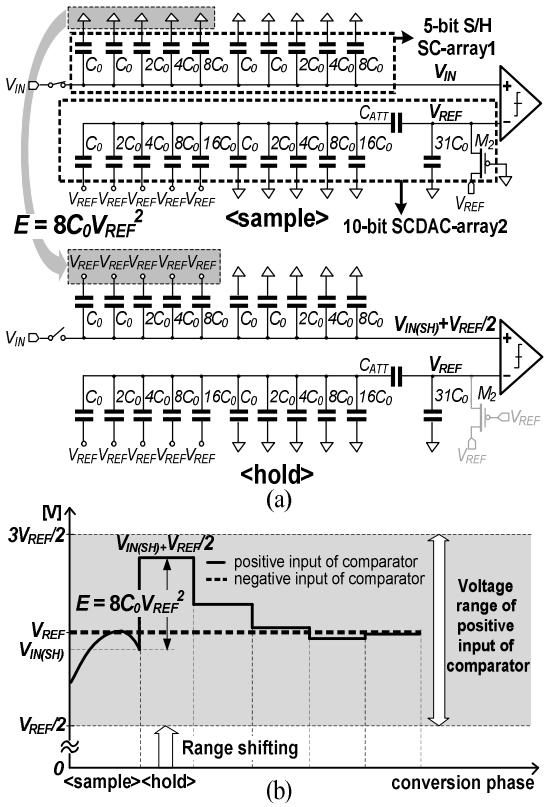

Fig. 6. Block diagram and switching energy generation of the proposed 10-bit SAR ADC with S-DCA (a) Block diagrams of the sample and hold operations, (b) Waveform of the comparator inputs (only the upper 5 MSBs are shown)

switches is also considered in the proposed design.

2. Energy-efficient Switching Scheme

In a single-ended SAR ADC, the capacitive-array is the most power hungry block owing to the large amount of switching energy. Although the DCA SAR ADC [5] reduces the switching energy at the expense of the additional 5-bit sample and hold (S/H) array, the DCA SAR ADC still consumes large amount of switching energy during the S/H operation. Several techniques using additional voltage reference of V_{CM} (=V_{REF}/2) have been introduced to reduce the switching energy [6, 7]. When V_{CM} is lower than the threshold voltage of the MOS switches, however, it cannot be applied to low-voltage, especially NTV applications [4]. The proposed ADC with no extra voltage reference achieves at least 42.7% less switching energy as compared with other single-ended SAR ADCs.

For the simple explanation, the ADC operation with one channel connection is illustrated to compare the conventional design [5] and the proposed design. Fig. 5(a) shows the block diagrams when the phase changes from sample to hold in the DCA SAR ADC, where the 10-bit DCA includes a 5-bit S/H *C-array1* and a 10-bit *CDAC-array2*. The largest capacitor of $512C_0$ is not for switching operation but for the binary ratio of the 10-bit *CDAC-array2*. In the sample phase, the positive input of a comparator is connected to the V_{IN} and the negative input is set to G_{ND} through M_3. Once the positive input of the comparator is sampled and held to be $V_{IN(SH)}$, the halves of the capacitors $512C_0$(C_0, $2C_0$, $4C_0$, … , $481C_0$) in the 10-bit *CDAC-array2* are reconnected from G_{ND} to V_{REF}, which results in V_{REF}/2 voltage shift of the negative input with the large switching energy of $256C_0V_{REF}^2$. Fig. 5(b) shows the waveform of the comparator inputs, where the voltage range of positive input of comparator is ranged from 0 to V_{REF}. Fig. 6(a) shows the block diagram of the proposed ADC for the S/H operation. The capacitor of $31C_0$ is for the binary ratio of the 10-bit *CDAC-array2*. The proposed ADC with **S-DCA** not only has the same capacitance between two capacitive-arrays

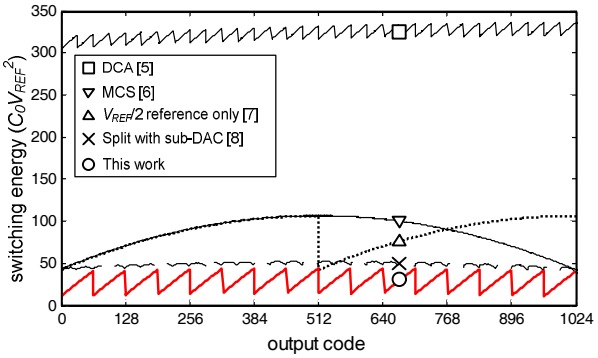

Fig. 7. Switching energy comparisons

Table 1. Comparisons between various switching schemes (single-ended SAR ADCs)

Switching procedure	Average switching energy ($C_0V_{ref}^2$)	Energy saving (%)
DCA [1]	323.0	reference
MCS [2]	85.3	73.6
V_{REF}/2 reference only [3]	84.7	73.7
Split with sub-DAC [4]	49.1	84.8
This work	28.1	91.3

but also contains the less total capacitance compared to the DCA SAR ADC. The analog voltage transition of the proposed ADC is different from the DCA SAR ADC.

Unlike the DCA structure that the negative input of the comparator is shifted up by V_{REF}/2, the positive input of comparator in the proposed S-DCA is shifted up by V_{REF}/2 to reduce the switching energy by 96.9% during the S/H operation. In the sample phase, the positive input of comparator is connected to the V_{IN} and the negative input is set to V_{REF} through M_2. In the hold phase, the halves of capacitors $16C_0$(C_0, C_0, $2C_0$, … , $8C_0$) in the 5-bit S/H *SC-array1* are reconnected from G_{ND} to V_{REF}, which results in V_{REF}/2 voltage shift of the positive input with the switching energy of $8C_0V_{REF}^2$. Eventually, the positive input of comparator becomes $V_{IN(SH)}$+V_{REF}/2 and its voltage range is shifted up by V_{REF}/2 as shown in Fig. 6(b). The switching energy of the proposed SAR ADC for the S/H and conversion phases is $80C_0V_{REF}^2$ and $12.1C_0V_{REF}^2$, which corresponds to 3.1% and 30% when compared with [5], respectively. The input-range shifting scheme is also suitable for NTV operations.

IV. Simulated Results

Fig. 7 shows MATLAB behavioral simulation results of the switching energy in 10-bit SAR ADC with various switching schemes. The proposed ADC shows the saw-type waveform which is the lowest switching energy over the entire output codes. The average values are summarized in Table 1. The proposed ADC reduces the average switching energy by 91.3% and 42.7% when compared with the DCA SAR ADC [5] and the split with sub-DAC [8], respectively. Table 2 shows the performance summary of the proposed 10-bit SAR ADC in 1P6M 55 nm CMOS process. As shown in Fig. 8, SNDR of 58.6 dB and SFDR of 74.5dB are achieved at 500 kS/s and 0.5V supply. The analog circuits (comparator, S/H, CDAC) consume 1.58 uW while the digital power consumption is 0.93 uW. The FOM of the proposed 10-bit SAR ADC is 7.2 fJ/conversion-step.

Table 2. Performance summary of the proposed 10-bit ADC

Process	55nm CMOS process
Supply	0.5V
Resolution	10bit
Sampling rate	500kS/s
SFDR	74.51dB
SNDR	58.6dB
ENOB	9.44bit
Power consumption	2.51uW
FOM	7.2fJ/conversion-step
Unit capacitance	5fF
Core area (only 1-channel)	0.13 x 0.07 mm^2

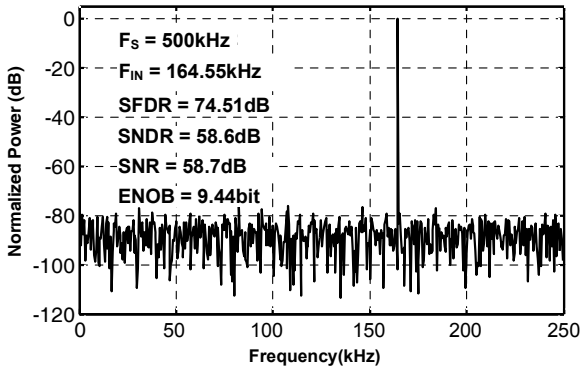

Fig. 8. Dynamic performance (F_S=500 kHz, F_{IN} = 164.55 kHz)

V. Conclusions

This paper proposes a single-ended SAR ADC by using S-DCA combined with input-range shifting scheme for multi-channel NTV systems. This work removes the

power hungry driving buffer in the front-end block of the analog MUX scheme, thus enhancing sampling speed. It also eliminates the offset mismatch problem between multiple comparators existed in the digital multiplexing scheme. Additionally, the large amount of kickback noise is reduced by assigning the same amount of load capacitance in this design, which reduces the total unit capacitance 84.4% compared to the previous DCA structure. By shifting up the sampled input voltage, the switching energies for S/H as well as conversion operations in the proposed ADC are dramatically reduced. As a result, the proposed ADC reduces the switching energy by at least 42.7% as compared with the previously reported schemes and achieves the state-of-the-art switching energy among single-ended SAR ADCs.

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