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위상차 클럭 기반 NoC 용 동기회로 설계

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Mesochronous Clock Based Synchronizer Design for NoC

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요 약

NoC는 SoC의 IP 코어들 사이에서 통신하는 시스템으로 기존의 버스 시스템이나 크로스바 상호연결 시스템보다 월등히 향상된 성능을 제공한다. 그러나 NoC의 송신부와 수신부 사이에서 데이터 이동 시에 송신부와 수신부 사이에 발생하는 불안정 상태(metastability)는 극복하기 위하여 동기회로가 필요하다. 본 논문에서는 신호 영역 발생기, 선택 신호 발생기와 데이터 버퍼로 구성된 새로운 위상차 동기회로를 설계하였다. 불안정 상태가 없는 선택구간을 구하기 위하여 전송된 클럭을 지연하는 회로가 사용되며, 전송클럭과 지역 클럭을 비교하여 선택신호를 발생한다. 제안된 위상차 동기회로는 선택신호 값에 의하여 지역클럭의 상승 또는 하강 모서리 중의 하나를 선택하여 불안정 상태를 제거한다. 모의실험 결과는 제안된 위상차 동기회로가 전송된 클럭과 지역 클럭의 어떤 위상차에서도 잘 동작하는 것을 보여 주었다.

ABSTRACT

Network on a chip(NoC) is a communication subsystem between intellectual property(IP) cores in a SoC and improves high performance in the scalability and the power efficiency compared with conventional buses and crossbar switches. NoC needs a synchronizer to overcome the metastability problem between data links. This paper presents a new mesochronous synchronizer(MS) which is composed of selection window generator, selection signal generator, and data buffer. A delay line circuit is used to build selection window in selection window generator based on the delayed clock cycle of transmitted clock and the transmitted clock is compared with local clock to generate a selection signal in the SW(selection window). This MS gets rid of the restriction of metastability by choosing a rising edge or a falling edge of local clock according to the value of selection signal. The simulation results show that the proposed MS operates correctly for all phase differences between a transmitted clock and a local clock.

키워드

Mesochronous Clock, Synchronizer, Metastability, Selection Window, Selection Signal
위상차 클럭, 동기 회로, 불안정 상태, 선택 구간, 선택 신호

Ⅰ. Introduction

Recent silicon technology has many processing elements and memories contained into a single chip

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to increase processing performance and a system is built in a chip. A system on chip(SoC) involves many computing resources such CPU, DSP, GPI, etc. A shared bus interconnection which needs an arbitration logic to serialize several bus access requests early in SoC is adopted to communicate with each integrated processing unit because of its low-cost and simple control characteristics. However, only one master at a time utilize the bus, that is, all the bus accesses should be serialized by the arbitrator, so such shared bus interconnection has some limitation in its scalability. Global synchronization(GS) is no longer suitable for high frequency SoC because of high latency, high area, and wire overhead, Globally Asynchronous, Locally Synchronous(GALS) clocking scheme is proposed[1].

Network on a chip(NoC) is a communication subsystem between intellectual property(IP) cores in a system on a chip(SoC) and can span synchronous and asynchronous clock domains. NoC technology applies networking theory and methods to on-chip communication and improves the scalability of SoCs, and the power efficiency of complex SoCs compared with SoC buses[2-4].

On-chip packet-switched micro-network of interconnects is used for scalable bandwidth requirement as shown in Fig. 1. This architecture consists in routers and IP(intellectual property)s. The basic idea came from traditional large-scale multi-processors and distributed computing networks [4]. The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC based system implementations[3].

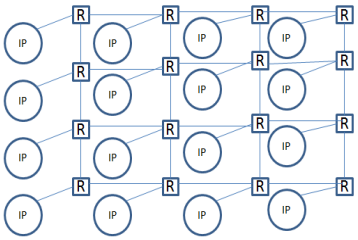


Fig. 1 NoC structure

A synchronizer is a device that samples an asynchronous signal and outputs a version of the signal that has transitions synchronized to a local or sample clock. In a mesochronous synchrony, signal has same frequency, but is out of phase with the clock[5]. Synchronization is required for multiple-clock domains in SoC designs when transferring signals and data asynchronously[5]. The mesochronous network is a network in which the clocks run with the same frequency but different phases compared with synchronous network. A mesochronous synchroizer(MS) is the most important part of mesochronous network. As shown in Fig. 2, input data and a clock in the sender are transferred to the receiver.

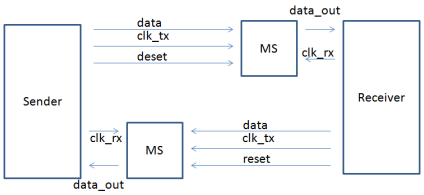


Fig. 2 Mesochronous network

In this paper, a new MS to solve above problems is proposed. The rest of paper is organized as follows. In section II, related work is described and a new MS is proposed in the section III. Section IV shows the simulation results, and the conclusion is described in section V.

II. Related work

The traditional mesochronous synchronizers are classified into a delay-line synchronizer, two register synchronizer, FIFO synchronizer and brute-force synchronization. A mesochronous signal is synchronized with the local clock and MS has to adjust the phase shift, if needed, to keep the signal transitions away from the unsafe regions of the local clock[5], [12]. A common design of mesochronous synchronizers consists of delaying either data or the clock signal to sample data reliably when they are guaranteed to be stable.

A typical scheme of delay-line based mesochronous synchronizer was proposed[6-8]. By changing the delay line settings, the relation between data and the clock is modified so that data transitions happen outside the dangerous region. The MS is very expensive because they need a delay line for each input.

A different approach for dealing with an unknown clock phase shift involves a phase detector circuit[9-12]. A phase detector is used to predict conflicts and to delay the write clock. Conflict detectors are used to track drifting phase shifts between multi-synchronous clock domains and to prevent metastability when using periodic clocks[8], [12].

Delay-line based synchronizers are mostly suitable for full custom designs. They require clock tree modifications and multiple instantiations for multi-bit applications. For SoCs which are based on standard cell design, including both ASIC and FPGAs, and which do not permit any fine-tune clock tree modifications, another approach to mesochronous synchronization is required[14], [15]. This mesochronous synchronizer employs cyclic write and read pointers respectively, with a certain initial spread to allow collision-free write and read operations. The write pointer is synchronous to a transmitted clock and the read pointer is synchronous to a local clock while the clocks are mesochronous. They provide enough time for multi-stage metastability resolution, but they require the design of ring counter.

Mesochronous data synchronization by defining forbidden zone mesochronous communication which uses two clocks with a phase shift of 180°and failure detector is designed[11], [13]. But many transistors are used for a phase detector. The MS for implementing the mesochronous clocking scheme which deals with metastability by using double-edge triggered flip-flops is developed[3]. this design has the architecture with less transistor and power consumption, but even though the scheme is not based on DLL, a phase detector is also needed.

A low complexity link microarchitecture for mesochronous on-chip communication is presented[16], but the MS requires the backward of complex control.

A scheme to handle mesochronous communication in 3D NoCs is proposed which assesses timing margins in a real NoC test case, thus coming up with optimized circuit solutions[17], [18]. However the work for 3D NoC addresses the support for bidirectional communication and flow control for backwards is needed for mesochronous signaling in a NoC.

An all-digital synchronizer that exploits the predictability of periodic clocks is proposed[19]. Its advantages include low latency, handling various clock frequency relations and robustness to clock jitter and phase drift. However, it incurs relatively high implementation complexity, requiring the tuning of several parameters to guarantee safe synchronization. It also uses custom design delay lines.

In summary, most of MSs can solve metastability disaster, but they have some other problems such as expensive cost and complex design. A new MS with low cost and simple design is required.

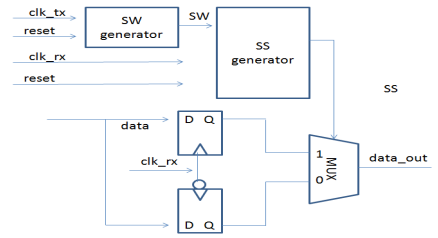
III. The proposed mesochronous synchronizer for NoC

The proposed MS receives input data, reset signal and a clock(clk_tx) from the transmitter and a local clock(clk_rx) from the receiver and outputs the synchronized data(data_out) to the receiver shown as Fig. 3[20].

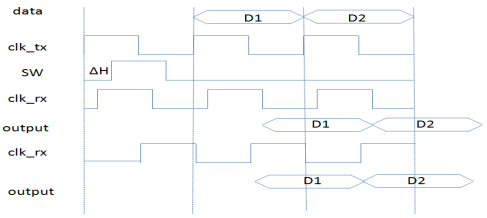
The MS is composed of SW generator, SS Generator, and other data buffers like Fig. 3(a). SW(selection window) is defined to a half-clock pulse window that the metastability does not happen. SS(selection signal) is defined to a signal used in MUX(multiplexer) to choose one of two input data which are latched by clk_rx and an inverted local clock(clk_rx_bar) respectively. clk_tx is used as a strobe as well. The proposed MS solves the metastability problem by selecting a clk_rx or clk_rx_bar as a synchronization clock depending on the value of SS whether the rising edge of clk_rx is inside the SW or not. A delay circuit is used to build SW based on the phase difference between clk_tx and clk_rx.

SS generator compares clk_rx and SS is outputted to MUX for data buffer selection. Then, selection is done by an alternative multiplexer named MUX based on the value of received SS. Input data is stipulated to start at the second rising edge of clk_tx.

If a rising edge of clk_rx is with the SW, the rising edge of clk_rx is used as a synchronization clock in the receiver and If a falling edge of clk_rx is with the SW, the falling edge of clk_rx is used shown as Fig. 3(b). So MS gets rid of the limit of metastability by selecting clk_rx or clk_rx_bar according to the value of selection signal.



(a) Proposed MS Scheme

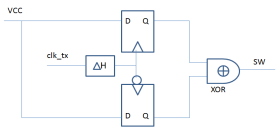


(b) Operation waveforms of the proposed MS

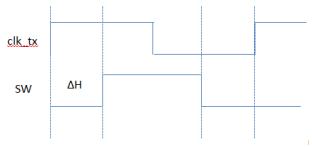
Fig. 3 Proposed MS and data operation waveforms

Fig. 4(a) shows a block diagram of the SW generator, which generates a single pulse of SW with a half clock period of clk_tx. The setup time and hold time can be obtained using bisection method by HSPICE and measurement results can be used for designing delay circuit with ΔH. In order to ensure correct data synchronization, following conditions should be satisfied,

1. ΔH must be larger than hold time violation.
2. ΔH should be smaller than half clock cycle minus setup violation.
3. MW should be smaller than half clock cycle.



(a) Block diagram

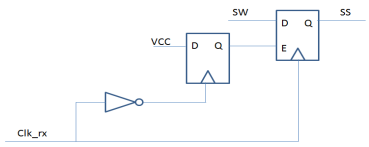


(b) clk_tx and SW waveform

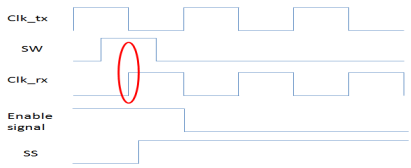
Fig. 4 Selection window generator and SW waveform

If this logic is designed without delay ΔH, there will be a wrong selection in data buffer. The relationship between clk_tx and SW is shown in Fig. 4(b) and ΔH is the delay between the rising edge of clk_tx and SW.

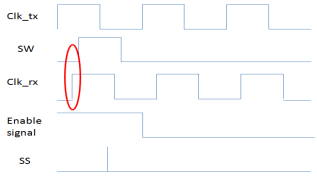
Fig. 5 shows SS generator and SS waveforms. SS generator consists in a DFF with enable signal and a delay circuit used for enable signal as shown in Fig. 5(a). The SS generator generates SS for MUX. clk_rx catches the value of SW and SS becomes logic 1 or 0 depending on the state of SW. If the rising edge of clk_rx is inside the SW, the value of SS is logic 1 like Fig. 5(b). otherwise the value of SS is logic 0 like Fig. 5(c).



(a) Block diagram of SS generator



(b) The rising edge of clk_rx inside the SW



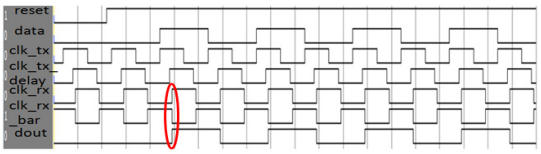
(c) The rising edge of clk_rx outside of the SW

Fig. 5 Block diagram of SS generator and SS waveforms

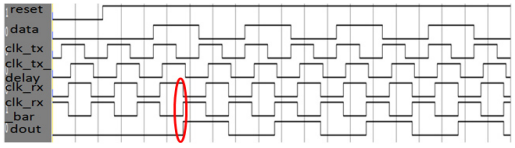
Ⅳ. Simulation results and considerations

The mesochronous synchronizer is designed by Quartus Ⅱ 9.1sp1 Web Edition and simulated by ModelSim- Altera 6.5b. Fig. 6 shows the simulation results of the proposed MS. clk_tx_delay is clk_tx with delay ΔH by delay logic in Fig. 4 and dout is data output of MS.

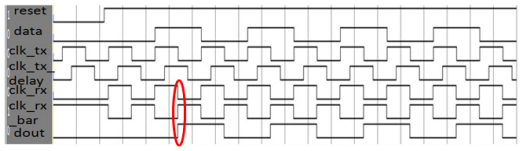
Fig. 6(a) shows that the rising edge of clk_rx is in the inside of SW and input data are latched at the rising edge of clk_rx and Fig. 6(b) shows that the rising edge of clk_rx is in the outside of SW and input data are latched at the falling edge of clk_rx when input data are at the outside of metastability window respectively. FIg. 6(c) shows that input data are within the setup time violation area of metastability window and they are latched at the falling edge of clk_rx behind a half clock cycle and MS outputs the data correctly. Fig. 6(d) shows that input data are within the hold time violation area of metastability window and they are latched at the falling edge of clk_rx behind a half clock cycle and MS outputs the data without error.



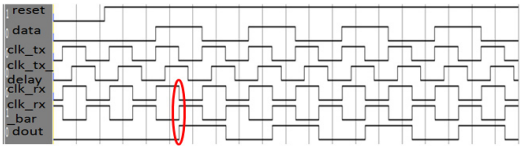
(a) Rising edge of clk_rx at the inside of SW



(b) Rising edge of clk_rx at the outside of SW



(c) Rising edge of clk_rx within the setup time



(d) Rising edge of clk_rx within the hold time

Fig. 6 Simulation results of MS

The proposed MS is compared with other MSs as shown in Table 1. It utilizes a delay line circuit to build SW signal, but without FIFO and phase detector. Some MSs need special design such as a nonoverlapping circuit or a frequency divider circuit to solve metastability problem. However, the proposed MS selects a local clock correctly without additional overhead and covers all phase differences between a transmitted clock and a local clock.

Table 1. Comparison with other MS

	Delay line	Phase detector	All phases coverage	Brute force
Vitullo [16]	Y	N	N	N
Mesgarzadeh [11]	N	Y	N	N
Frank[8]	N	N	N	N
Kim [13]	Y	N	Y	N
Dally [19]	Y	Y	Y	N
Ludovici[18]	N	Y	Y	Y
Proposed MS	Y	N	Y	N

Ⅴ. Conclusions

A new mesochronous synchronizer is proposed in this paper. A delay line circuit based on measurement results of MW is used to build SW. SS is based on the phase difference between a transmitted clock from sender and a local clock in the receiver. Then, SW is used to generate SS. This MS avoids the restriction of metastability by selecting the rising edge or falling edge of a local clock according to the value of SS. The simulation results show that the proposed MS works correctly for all phase difference. In the future work, the I/O buffers to be used in NoC will be designed.

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