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동기회로 설계를 위한 CMOS DFF의 준비시간과 유지시간 측정

김강철*

Measurement of Setup and Hold Time in a CMOS DFF for a Synchronizer

Kang-Chul Kim*

요 약

반도체 공정 기술의 발전으로 하나의 칩에 많은 코어가 포함되고 있으며, 전력이나 클럭 스큐 문제들을 해결하기 위한 방안으로 다른 주파수나 위상차를 가지고 있는 여러 개의 클럭을 사용하는 GALS 기법이 사용되고 있다. GALS에서는 송수신부 사이에서 동기화 문제를 해결하기 위하여 동기회로가 사용된다. 본 논문에서는 180nm CMOS 공정 파라미터를 사용하여 온도, 전원전압, 트랜지스터의 크기에 따라 동기회로 설계에 필요한 DFF의 준비시간(setup time)과 유지시간(hold time)를 측정하였다. HSPICE의 이분법을 이용한 모의실험 결과에서 준비시간과 유지시간의 크기는 전원 전압의 크기에 반비례하고, 온도에 비례하였다. 그리고 유지시간은 음의 값으로 측정되었다.

ABSTRACT

As the semiconductor processing technology has been developing, multiple cores or NoC(network on chip) can be contained in recent chips. GALS(globally asychronous locally synchronous) clocking scheme that has multi-clock domains with different frequencies or phase differences is widely used to solve power consumption and clock skew in a large chip with a single clock. A synchronizer is needed to avoid a synchronization problem between sender and receiver in GALS. In this paper, the setup and hold time of DFF required to design the synchronizer are measured using 180nm CMOS processing parameters depending on temperature, supply voltage, and the size of inverter in DFF. The simulation results based on the bisection method in HSPICE show that the setup and hold time are proportional to temperature, however they are inversely proportional to supply voltage, and negative values are measured for the hold time.

Keywords

Gals, Setup Time, Hold Time, Metastability

전역 비동기 국소 동기화, 시동 시간, 유지 시간, 메타 안정도

Ⅰ. Introduction

As the chip size and the number of gate in a chip are increasing, a system can be included in a chip called SoC(System on Chip). The clock distribution in design of SoC is one of a key component to reduce power consumption of the chip, and it is assumed that all clock signals are arrived at the flip flops at the same time, but there may be a delay due to the length difference

* 교신저자 (corresponding author) : 전남대학교 전기전자통신컴퓨터공학부(kkc@jnu.ac.kr)
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of metal line, load capacitance of node, and so on. Various clock scheme methods such as H-tree structure, GALS(Globally Asychronous Locally Synchronous), etc. are proposed[1-3]. The chip implemented by GALS architecture is divided into multiple frequency domains. When GALS architecture is applieded to SoC or NoC(Network on chip), synchronizers should be used to solve the synchronization.

The degrees of synchrony between input signals and the receiver system clock is classified into synchronous, mesochronous, plesiochronous, periodic and asynchronous clock[4]. Mesochronous clock has same frequency, but is out of phase with the clock.

A synchronous clock scheme is the most convenient to CMOS VLSI design, but there may exist a clock skew in NoC. To avoid the above problems, multi-clock schemes are used in general.

Any violation of the synchronous design style could greatly complicate the circuit design and increase design time and the risk of system failure. The risk named as metastability results in wrong or metastable value of output almost in every flip flop and its window exists as the sum of setup time and hold time. To reduce the effect of metastability when communicating with a mesochronous clock, flip-flops are used for synchronization. To design reliable synchronizers, a model to estimate the failure mechanism is given by MTBF(mean time between failure) as the equation (1).

$$\mathrm{MTBF}=\frac{e^{s/\tau}}{T_W F_C F_D} \tag{1}$$

where F_C and F_D are the clock and data transition frequencies respectively, s is the time allowed for metastability resolution, τ is the resolution time constant, and T_W is the parameter describing a vulnerable time window[5-6].

Typical types of timing constraint violations include data setup time before the clock, data hold time after the clock, minimum pulse width required for a signal to propagate to the output. and maximum toggle frequency of the components[7]. The data should be stable before it is captured by the clock edge and on the other hand, the logic value of input data must be kept stable for hold time after the capturing clock edge to guarantee that the flip flop will store the correct value.

Then a proper logic to effectively deal with metastability is needed. In order to design such a synchronizer, measurement and analysis of setup time and hold time in a flip flop are necessary.

In this paper the setup and hold time of a CMOS DFF(: D-type flip-flop) that are composed to metastability window are measured by bisecction in Hspice and analyzed to design a new mesochronous synchronizer for NoC depending on supply voltages and temperature variation effects.

This paper is organized as follows. In section II, related works are described, and bisection method is introduced and output sweeping and procedures are shown in section III. Section IV shows measurement results in DFF using HSPICE. Finally conclusion is written in section V.

II. Related work

As the number of primary parameters affecting circuit performance are increasing, the need for Statistical Static Timing Analysis(: SSTA) has been firmly established in the last few years[8,9].

Assuming Gaussian distribution, Variation Per Sigma(: VPS) from two points of the distribution curve can be derived[9]. To reduce number of simulations, it is best to simulate in the low sigma region. For this purpose, the following hold time characterization methodology was proposed. First binary search to find the hold time failing point with local random variability turned off was used and the real failure at the latched node to avoid

circuit topology dependency was observed. In the vicinity of the failing point, another two hold-time offset points to run limited number of Monte-Carlo simulations were selected. Using the simulated yield results, the zero-sigma hold time and VPS were derived, ans the new hold time was defined as the corresponding sigma value like the equation (2),

$$T(s)=T(0)+(s+m)*VPS \quad (2)$$

where s is the sigma value, T(0) is the zero sigma hold time, VPS is the variation per sigma, and m is the margin number. In [9], a new statistical margin quantifying methodology, setup and hold time definition and characterization methodology were proposed.

Failure probabilities considering device process variations on several long and short paths extracted from a RTL MAC Multiplier-Accumulator physical synthesis based on a SSTA(Statistical Static Timing Analysis) method were studied with the manipulation of probability distribution functions and thus, to keep all the variability information[10]. Setup time, hold time, and delay propagation variation figures were extracted and several results on combinatory paths and flip-flop cells were given to underline the variability impacts.

There are various synchronizers for clock synchronization and variants of N-flip-flop synchronizers are employed when the communicating clocks are asynchronous. The reliability of N-flip-flop synchronizers is expressed by the standard MTBF formula[6]. The paper described the coherent clocks that suffer of a higher failure rate than predicted by the MTBF formula and showed metastability failure in a real 40nm circuit and guidelines used to increase its MTBF.

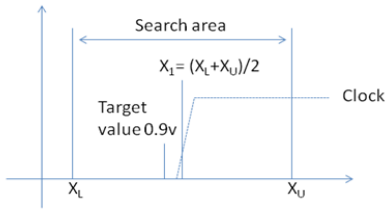
Synchronizers play a key role in multiclock domains systems on chip and their performance is usually measured by the mean-time between failures of the system. A new model for the metastability time constant, the metastability window, and MTBF was presented[5]. Design guidelines that account for supply voltage and temperature variations and determine the correct number of synchronizer stages required for target MTBF were proposed.

Conventional flip-flop timing models have fixed values of setup/hold times and clock-to-q delay, with some advanced “setup-hold pessimism reduction” methodologies exploiting multiple setup-hold pairs in the timing model. Multiple timing models to give more flexibility at timing path boundaries were proposed[11].

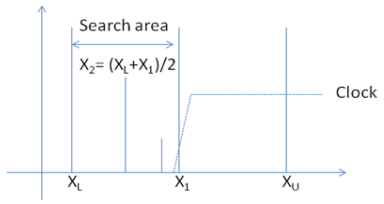
III. Bisection method and output sweeping

Three iterations of the measurement method are shown in Fig.1. This method uses a bisectional search to find the minimum setup time for a DFF. Hspice does not directly optimize the setup time, but extracts it from its relationship with the parameter named DelayTime(the delay between clock and data signal), which is the parameter to optimize. The target value which indicates the value of DFF output is 0.9v in this method and supply voltage is 2V. XU and XL are two initial boundaries in first iteration. First bisection value as shown in Fig. 1 (a) is the mid-way(X1) between specified boundaries and the first test value passes because measured value is greater than goal value. Then X1 will be the new lower boundary. Similarly X2 in second and X3 in third iteration are bisection value as shown in Fig. 1 (b) and (c).

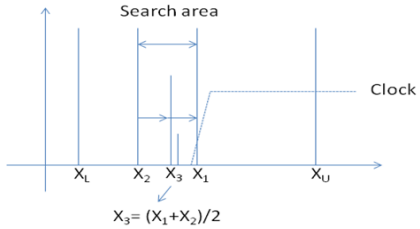
Before the bisection is used, a pair of values (the upper and lower boundaries of the input variables), a goal value, error tolerance value and related variables are specified. When the difference between the two latest test input values is within the error tolerance and the latest measured value exceeds the goal, bisection has succeeded and then ends.



(a) First iteration



(b) Second iteration



(c) Third iteration

Fig. 1 Bisection of three iterations

One bisection procedure of measuring setup time as an example of showing how to organize bisection procedure in DFF shown as Fig. 2 is implemented[12][13].

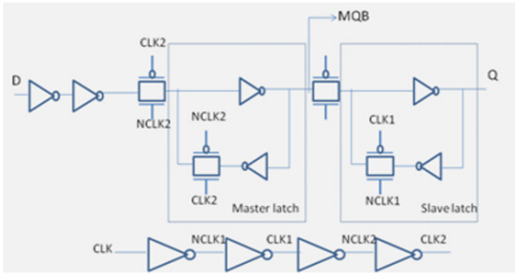
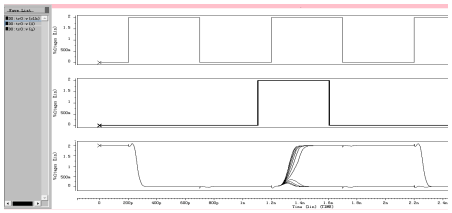


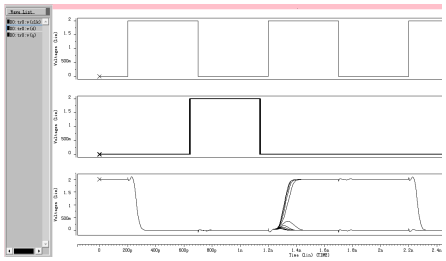
Fig. 2 CMOS DFF

Setting initial upper and lower boundaries is based on the actual value of setup time. Long time period of upper and lower boundaries results in same output value of DFF. If the time period of upper and lower boundaries is too short, the target value can not be searched.

The data arrival time near the setup and hold time domain is swept and the results are shown in Fig. 3 (a) and (b). The upper and lower boundaries easily are set from these results. For example, the setup domain is located obviously between 1100ps and 1200ps in Fig. 3 (a). Thus 1100ps and 1200ps are the initial upper and lower boundaries. Then the acquiescent measurement is done when temperature is 25℃ and the supply voltage is 2V.



(a) Setup time sweeping



(b) Hold time of sweeping

Fig. 3 Setup and hold time sweeping

To see the influence of temperature, supply voltage, and CMOS size of transmission gate in the metastability window, various experiments are committed. The temperatures of 0℃ to 100℃ with the step of 20℃ are swept. Fig. 4. shows that the higher temperature causes longer delay of DFF output. The supply voltage is swept from 1.2V to 4.0V with the step of 0.2V and the result indicates that the higher supply voltage causes the shorter output delay in Fig. 5.

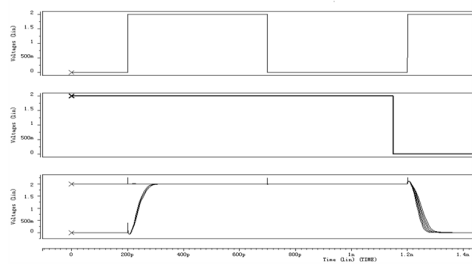


Fig. 4 Output sweeping for temperature

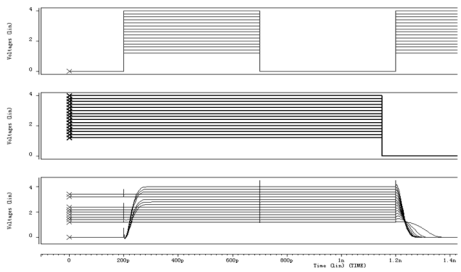


Fig. 5 Output sweeping for supply voltage

To measure and simulate the setup and hold time the clock cycle is set to 1000ps and input data has one positive pulse with 500ps duration. Measurements and simulations are performed in 180nm CMOS process by HSPICE. The DFF used for all simulations is shown in Fig. 2.

The width of NMOS in transmission gate in Fig. 2 is swept from 1 unit length(180nm) to 5X. The width of the PMOS transistor is twice to NMOS transistor. The result shows that delay of output in DFF increases as width of NMOS in the transmission gate increases like Fig. 6.

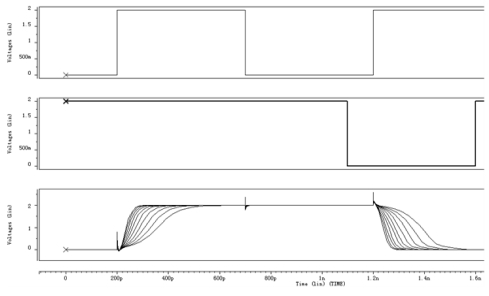


Fig. 6 Output sweeping for CMOS size

IV. Measurement results

Setup time and hold time values versus temperature and supply voltage are measured using bisection method. The simulation results show that setup and hold time increase as temperature is increasing in Table 1 for the size ratio P/N=1/1 of transmission gate at supply voltage 2V in DFF shown in Fig. 2. And setup and hold time decrease as supply voltage is increasing in Table 2 for the size ratio P/N=2/1 of transmission gate at 25℃.

Table 1. Setup time and hold time versus temperature

Temperature(℃)	Setup time(ps)	Hold time(ps)
0	41.310	-35.848
25	44.343	-38.416
50	47.724	-41.056
75	51.065	-43.760
100	54.455	-46.473

The results indicate that the setup time and hold time are positively proportional to temperature at fixed supply voltage and P/N size ratio of inverter, and inversely proportional to supply voltage at fixed temperature and P/N size ratio of inverter. The hold time has a negative value, which means that the hold time duration happens before the rising edge of clock. Fig. 7 and Fig. 8 show the setup time and hold time for temperature and supply voltage respectively.

Table 2. Setup time and hold time versus supply voltage

Supply voltage(V)	Setup time(ps)	Hold time(ps)
1.2	73.912	-69.970
1.5	56.212	-52.886
1.7	50.282	-46.497
2.0	44.791	-40.267
2.5	39.809	-42.285
3.0	37.384	-30.743
3.5	36.131	-28.434
4.0	35.654	-26.685

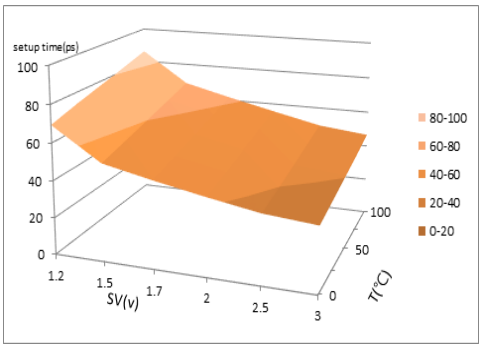


Fig. 7 Setup time for temperature and supply voltage

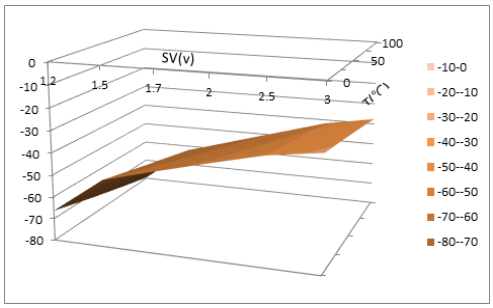


Fig. 8 Hold time for temperature and supply voltage

VI. Conclusions

Many clocks with different frequency or phase difference are used for large chips such as SoC or NoC. The mismatch between sender and receiver in phase and frequency can cause data loss and good synchronizers are needed. The analysis and measurement of the setup and hold time are indispensible to avoid metastability state in synchronizer.

In this paper, the setup and hold time were analyzed and measured using bisection method for different levels of supply voltage, temperature and the P/N size ratio of inverter in DFF. The HSPICE simulation results show that the setup time and hold time are proportional to temperature and inversely proportional to supply voltage. These results will be used to design synchronizers for the future.

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저자 소개

김강철(Kang-Chul kim)

1981년 서강대학교 전자공학과 학사
1983년 서강대학교 전자공학과 석사
1996년 경상대학교 전자공학과 박사
현재 전남대학교 전기전자통신컴퓨터공학부 교수
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