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Optimization of Thermal Performance in Nano-Pore Silicon-Based LED Module for High Power Applications

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Abstract

The performance of high power LEDs highly depends on the junction temperature. Operating at high junction temperature causes elevation of the overall thermal resistance which causes degradation of light intensity and lifetime. Thus, appropriate thermal management is critical for LED packaging. The main goal of this research is to improve thermal resistance by optimizing and comparing nano-pore silicon-based thermal substrate to insulated metal substrate and direct bonded copper thermal substrate. The thermal resistance of the packages are evaluated using computation fluid dynamic approach for 1 W single chip LED module.

Keywords: *chip-on-board (COB), direct bonded copper (DBC), insulated metal substrate (IMS), light emitting diodes (LEDs), nano-pore silicon-based (NPSB) printed circuit board (PCB)*

1. Introduction

In the recent decades, incandescent lamps are replacing with LED bulbs with their advantages of high efficiency, long lifetime, reliable fabrication, and environmental protection [1]. However, as the input power increases, redundant heat generated from the chip result in elevated junction temperature. This phenomenon will reduce the lifetime and accelerate the luminous decay rate of LEDs [2, 3]. In general, input power in LEDs is only converted light illumination of 15%~30%, whereas 70% to 85% is dissipated thermally [4, 5]. For effective heat dissipation, an economical heat spreader, heat sink is used. The heat dissipation in a typical LED package can be described by a few stages: At first, the heat at the p-n junction of LED chip is conducted through intermediate materials such as die, die-attach, thermal substrate, thermal interface materials (TIMs), heat slug and transferred heat is then conducted into an attached heatsink. The downstream heat at heatsink is transferred to the environment by convection phenomenon. The upstream heat flow is ignored due to only a small amount of heat is transferred to the lens area [6, 7]. Therefore, there have been many researchers working on optimization of thermal characteristics of high power LED packages with analytical, simulation, or experimental methods [8, 9].

In this paper, the thermal performances of single chip was investigated by computational fluid dynamic (CFD) based Flotherm software simulation. Thermal substrates including the proposed NPSB, insulated metal substrates (IMS) and direct bonded copper (DBC) were designed and studied by implementing

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chip-on-board package technology. In the CFD analysis, several lead free solders and thermal interface materials were considered. Optimization was done with die and die-attach in terms of their thicknesses and conductivities. Comparative package analysis was conducted on 1 W LED module with thermal substrates of NPSB, IMS, and DBC. With this thermal analysis, critical design considerations were investigated in order to minimize device temperatures which used to improve ultimately both light output, device lifetime, and reliability.

2. Computational fluid dynamic analysis

The LED chip composed of InGaN structure and the dimensions are 1150 μm by 1150 μm and 5 μm thick. In addition, uniform heat generation in the volume of the chip. InGaN structure is mounted on a Si die and attached using a eutectic bonding such as Au-Si. In that case, the generated heat around chip can be considered as a uniform heat flux on the top surface of the die. The die is located on a power electronic substrate including NPSB, DBC, PCB and IMS, and attached using method of the lead-free solders. This structure can be regarded as a single-chip LED package with NPSB, DBC, PCB and IMS or a part of LED arrays implementing COB package technology. The detailed information for materials, dimensions, and thermal conductivities are summarized and depicted in Table 1.

Table 1. The detailed information of dimensions and material properties.

Components	Thickness	Size	Material		Thermal conductivity
LED Chip	5	1.15 x 1.15 mm^2	InGaN		130
Metallization	10	~	Au-Si eutectic bonding		27
Die	375	~	Si		124
Die-attach	50	~	Lead-free solder	100In	82
				Au-20Sn	57
				Sn-3.5Ag	33
Thermal substrate	~	1 x 1 cm^2	NPSB	Ag/Si	117/419
				Au-20Sn	57
				Al	150
			IMS	Cu	385
				Dielectric	1.1
				Al	150
			DBC	Cu	385
				AlN	180
				Al_2O_3	30
TIM	50	~	Thermal grease		3
Heatsink	~	~	Alloy 6061		150

The materials are homogeneous and isotropic, and their thermal conductivities are not dependent on the temperature. 3D view of the heatsink design is shown in Fig. 1 (a) that based on Al 6061 Alloy, which is a commercially available heatsink for natural convection. Boundary conditions are displayed in Fig 1 (b). Entire surfaces the die and substrate excluding the top of the die are adiabatic. The consideration of the boundary condition is reasonable because total heat generated by LEDs is dissipated by conduction. The heat dissipation by convection around the die and substrate is negligible because they are placed inside the

package and the most of them has very low thermal conductivity. The general heat dissipation by conduction in LED package is considered as more than 90%. In general, generated heat passes through the LED package structure and is dissipated through heatsink. Free convection around heatsink was considered, therefore uniform convective heat transfer coefficient, h=10 W/m^{2}K, at 25 ℃ ambient temperature.

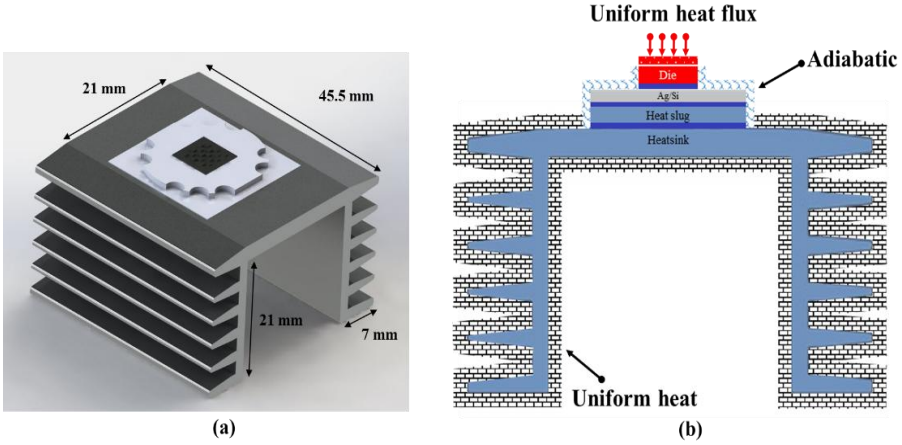

Figure 1. (a) An implemented heatsink design and (b) the boundary conditions

In order to evaluate the thermal management of the proposed system, it is needed to analyze thermal characteristics of the system. The vertical temperature profiles and heat flux along the central reference line provides very good view for the thermal resistance of the system. In addition to the temperature profile, prediction of the thermal resistance of each layer and the variation in thermal resistance with the variation of design. The vertical temperature profiles and heat flux along the central reference line was investigated by use of conduction thermal resistances in Fig.2.

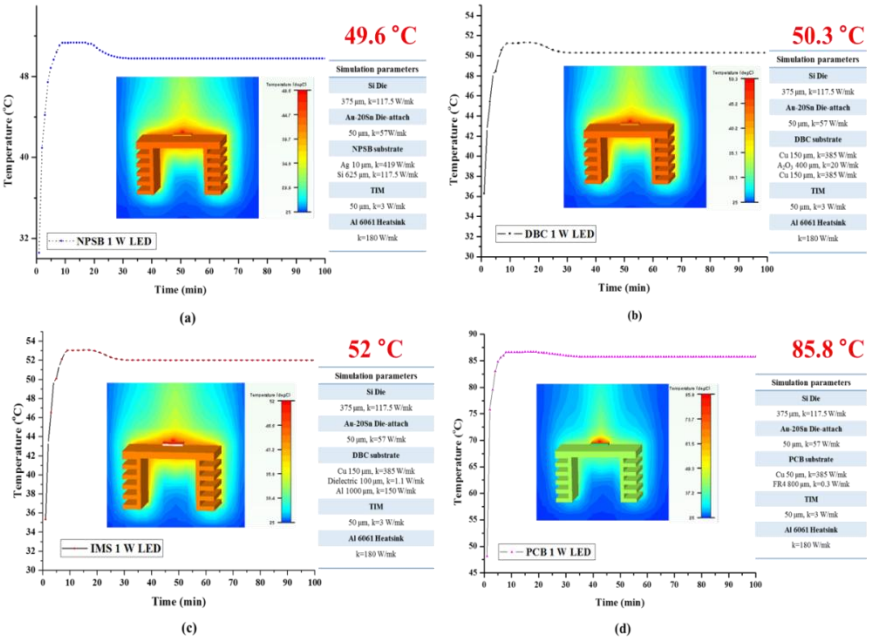

Figure 2. The contour plots of temperature distribution of LED package using power electronic substrate. (a) NPSB substrate, (b) Al_2O_3 DBC substrate, (c) IMS, and (d) PCB

Discrepancy between two points directly gives the area dependent thermal resistance by applying Eq. 1.

$$q'' = \frac{Q}{A} = -k\frac{\Delta T}{L} \quad (1)$$

The temperature difference between the top and bottom of each layer becomes the thermal resistance of each layer. The thermal resistance of the NPSB substrate without a heatsink is 2.48 ℃/W, which is much smaller than that of the heatsink, 24.54 ℃/W. This is because a NPSB substrate with good thermal performance was used for the package while a relatively small size for the heatsink was simulated. The heat flux along the central reference line in the die, the die-attach, and the TIM barely changes, which indicates that little or no heat spreading has occurred. In contrast, the heat flux along the central reference line in substrate changes a lot, which indicates large heat spreading. The reduction of the heat flux also makes the thermal resistance of the TIM small despite its very low thermal conductivity, 3 W/mK.

In order to investigate the thermal characteristic with respect to different substrates, the vertical temperature profiles of the packages, which use Al_2O_3 DBC substrate and a dielectric IMS structure, were also plotted, and compared with that of an NPSB substrate in Fig.3.

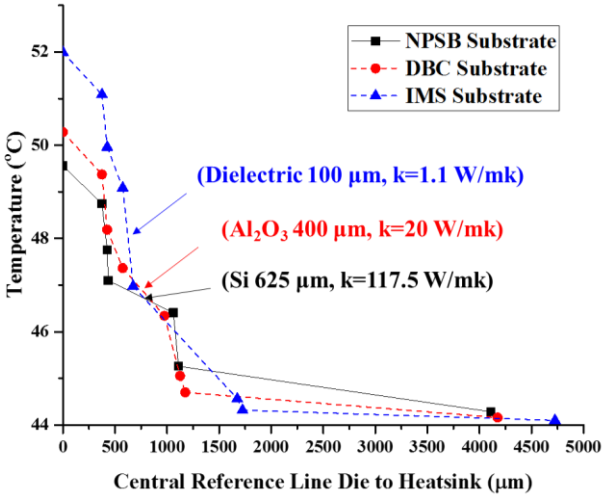

Figure 3. Comparison of the packages with respect to vertical (z-axis) temperature profile

The same design and conditions were used for these simulations, with only changes in the dielectric material and overall substrate thickness. The same thickness of the copper layer in the substrate, 150 µm, was used. Since the same geometry and materials were used in the die and the die-attach, the slopes of three simulations are almost same in the die and die-attach. The large difference is shown in the substrate because different substrates are used. The thermal resistance of IMS is about 1.5 times larger than that of NPSB substrate. This is not a large difference compared to the difference between thermal conductivities of the dielectric layers of the IMS and NPSB; 1.1 W/mK and 127 W/mK, respectively. Since the heat flux is spread by the top Ag layer and then flows through the Si layer, it increases the heat flux area and the thermal resistance of Si layer is reduced. Therefore, the thickness and the area size of the Ag layer are important for the reduction of the thermal resistance of overall power substrate. Since the heat flux in the die and die-attach is very high, the junction temperature is very sensitive to the thermal conductivity and the thickness of the die and die-attach.

2. Optimization of thermal substrates

The junction temperature change with respect to different materials and thicknesses of the die and die-attach was studied. The vertical thin film structure was considered and available materials for die are Si and SiC. Si is very widely used because of its cheap price, easiness in processing, and fairly high thermal conductivity, 124 W/mK. SiC is an alternative material that has not only high thermal conductivity, 370 W/mK, but also well-matched CTE with GaN. Nevertheless, it is not used generally due to its extraordinary high price. The junction temperature as a function of thickness is shown in Fig. 4 (a). The behavior of junction temperature with respect to thickness is almost linear, which implies that the thermal resistance of die can be assumed as a one-dimensional form. Therefore, the thinner die is definitely better for thermal management. The behavior of junction temperature with respect to die-attach thickness shown in Fig. 4 (b) is almost linear and response is similar to the die. Although the thermal conductivities of die-attach materials are lower than those of die materials, their thermal resistances are not significantly high because of their relatively small thickness. Considering the general thickness of die-attach, around 50 μm, the junction temperatures of the packages using Sn-3.5Ag, Au-20Sn, and 100In are 50.2 ℃, 49.55 ℃, and 49.34 ℃, respectively.

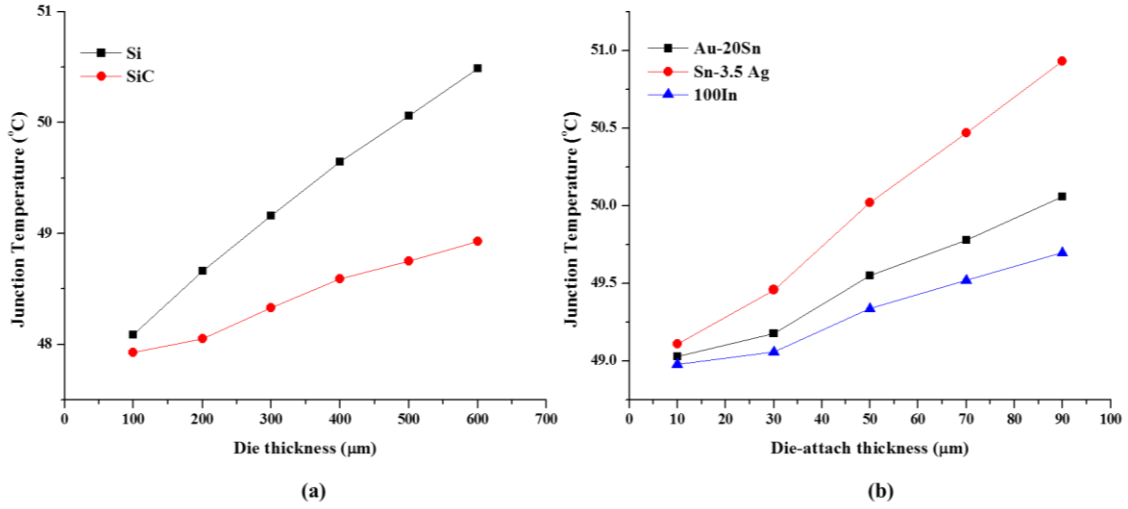

Figure 4. The junction temperature as a function of (a) die and (b) die-attach thicknesses

The heat spreading of the substrate level mainly occurs in the plated metal circuit layer such as Cu, Al, and Ag, the important factors to determine the thermal resistance of a substrate are the thickness of the plated metal circuit layer and the size of the substrate. Several simulations using different thickness of the plated metal layer and different size of substrates were performed. The difference of the plated metal circuit layer thickness is shown in Fig. 5 (a), and the junction temperature as a function of thickness of plated metal circuit layer. It confirms that a thicker plated metal layer can achieve a lower thermal resistance. However, the impact of plated metal thickness varies with types of the substrate and their property. In case of the LED package with the NPSB substrate, the junction temperature difference between 10 μm and 400 μm of Ag layer is only 1.58 ℃ with 1 W operation.

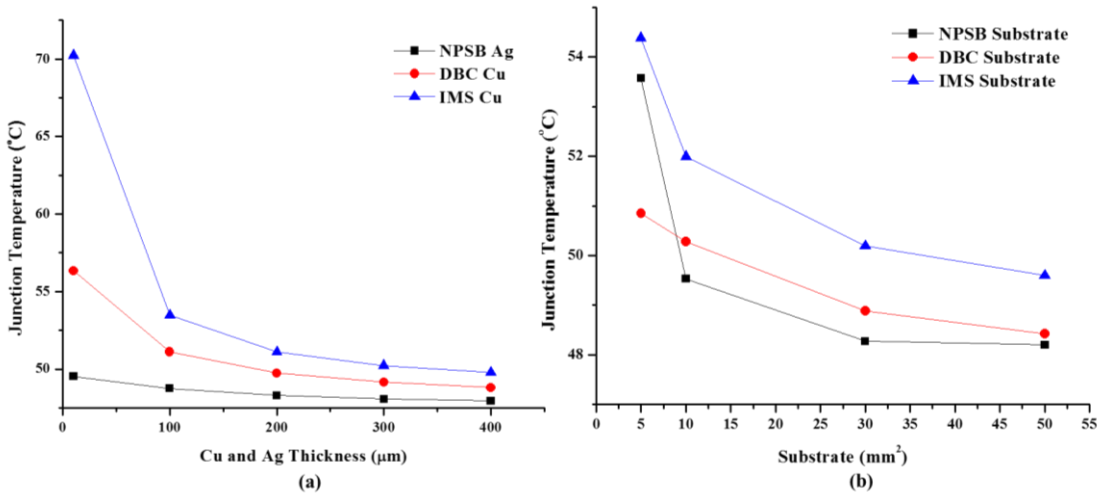

Figure 5. The junction temperature as a function of (a) thickness of the metal circuit layer and (b) thermal substrate size

This is because the Si with its large thermal conductivity of 117.5 W/mK contributes to the heat spreading, assisting thinner Ag with high thermal conductivity of 389 W/mK circuit layers. Simulation analysis was performed by varying substrate size shown in Fig. 5 (b). When the size of a substrate is small, the rate of decrease in junction temperature is large. This is because a certain size of substrate is required to spread heat enough in the substrate and the size is determined by the design and materials used. For example, 20 to 30 mm^2 is enough to spread heat for all the substrate, from 40 to 50 mm^2 is reducing impact the of substrate size. A thicker plated metal circuit layer is typically better for thermal management. However, the plating metal circuit layer's thickness is limited by the cost and by the ability to pattern thick circuit layers. The required resolution of the circuit pattern is strongly dependent on the application.

3. Conclusion

In this paper, the thermal analysis of NPSB high power LEDs implementing COB architecture was analyzed by CFD and was compared to DBC and IMS thermal electronic substrate. The thermal analysis started with single chip LED with 1 W and to evaluate thermal substrate, comparative analysis was discussed. In the simulation, effects of the metallization layer thickness was examined in terms of variation of the junction temperature. As well as, effect of the die and die-attach was analyzed. As result of simulation analysis, NPSB substrate can dissipate heat very efficiently compared to a conventional FR4 based PCB, even DBC and IMS, and this is because of low thermal impedance of dielectric layer and effective heat spreading in thin Ag layer.

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