Generalized Selective Harmonic Elimination Modulation for Transistor-Clamped H-Bridge Multilevel Inverter

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Abstract

This paper presents a simple approach for the selective harmonic elimination (SHE) of multilevel inverter based on the transistor-clamped H-bridge (TCHB) family. The SHE modulation is derived from the sinusoidal voltage-angle equal criteria corresponding to the optimized switching angles. The switching angles are computed offline by solving transcendental non-linear equations characterizing the harmonic contents using the Newton-Raphson method to produce an optimum stepped output. Simulation and experimental tests are conducted for verification of the analytical solutions. An Altera DE2 field-programmable gate array (FPGA) board is used as the digital controller device in order to verify the proposed SHE modulation in real-time applications. An analysis of the voltage total harmonic distortion (THD) has been obtained for multiple output voltage cases. In terms of the THD, the results showed that the higher the number of output levels, the lower the THD due to an increase number of harmonic orders being eliminated.

I. INTRODUCTION

Recently, the demand for medium-voltage, higher power converters that are capable of producing high quality waveforms, while utilizing low voltage devices and reduced switching frequencies have led to increases in multilevel inverter development. Over the years, several multilevel inverter topologies have been developed as alternatives for medium voltage and high power applications, and they offer advantages over the single switch and series connection approaches [1]. Multilevel inverters have been shown to have the following advantages: reduce common-mode voltage,

lower switching stress, lower total harmonic distortion (THD), improve output voltage/current quality, etc. [2]-[4].

The most common multilevel inverter topologies include the diode clamped or neutral point clamped (NPC), capacitor clamped or flying capacitor (FC), and cascaded H-bridge (CHB) inverters [3]-[8]. It is absolutely necessary to produce an effective and innovative power converter design, from the perspective of cost and efficiency, for optimizing output power with significantly fewer losses. The requirements for the maximum voltage and current total harmonic distortions (THDs), as specified in IEEE Std.519-1992, must be fulfilled by the multilevel inverter [9]. Some researchers have overcome the complexity of the multilevel inverter circuit by rearranging the switches and DC voltage sources [10]. This produces a new breed of multilevel topologies: the active NPC (ANPC) [11], modular multilevel converter (MMC) [12] and transistor-clamped converter (TCC) [13], [14].

To obtain a good output voltage, various modulation algorithms have been developed for multilevel inverters. They are classified according to their switching frequency. Each has

unique advantages and drawbacks and their selection is made according to the application and the inverter topology. When the high switching frequency exceeds 1 kHz [3], the schemes involve multireference/multicarrier pulse-width modulation (PWM) [2],[13],[15] and space-vector modulation (SVM) [7]. Although the acoustic noise is low and in some cases the output filter size is also reduced, the high switching frequency technique increases the switching losses and is complicated in eliminating low-order harmonics. Another modulation algorithm for multilevel inverters running on the low (or fundamental) switching frequency [16]-[23] is selective harmonic elimination (SHE). There are two different aims when using the low switching frequency modulation technique: 1) to eliminate the specific lowest order harmonics of the inverter output voltage; and 2) to minimize the inverter voltage THD. Such a scheme lets the power semiconductors have very few commutations per output cycle. This has the advantages of reducing the switching losses, eliminating the low-order harmonics, and allowing for a smaller size filter if necessary [16].

To address the SHE problems, the determination of the optimized switching angles is essential through solving a set of non-linear transcendental equations. The transcendental equations, which are defined as SHE equations, characterize the harmonic components with respect to the fundamental voltage component based on the Fourier series expansion. As these equations increase, solving them becomes a challenge. One of the most widely used techniques is the Newton-Raphson (NR) method [17], [18]. This is an iterative method to find complex roots in polynomials and roots of equations with several variables. Another approach for the SHE method, based on optimization algorithms utilizing genetic algorithm (GA), has been proposed to calculate the optimum angles for CHB multilevel inverters [18]-[20]. A particle swarm optimization (PSO) technique has been used to calculate the switching angles of an 11-level inverter with equal and unequal DC source cases in [18], [21], [22]. Although optimization methods based on GA and PSO are frequently proposed in reducing calculation time, the harmonic elimination will be difficult to implement owing to the advanced control and the urge to use advanced mathematical algorithms.

To date, most of the low switching frequency modulations have been realized for the CHB topology, either in single-phase or three-phase systems. However, the CHB topology has some drawbacks since it requires a higher number of switching devices and isolated DC power supplies as the number of output levels is increased. Recently, the authors in [23] have proposed the harmonic distortion minimization method, with or without the elimination of the lowest order harmonics for a higher number of voltage level (i.e. 5-level up to 13-level). Although the proposed method in [23] may achieve the minimum voltage THD, it necessitates the use of a larger AC
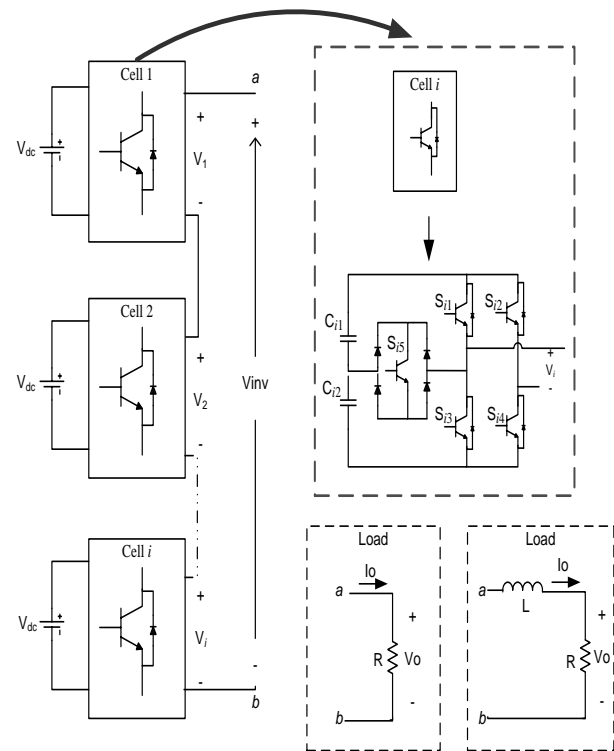

Fig. 1. The TCHB based cascaded multilevel inverter topology.

output filter, as pointed out in [16]. Moreover, the implementation results for 11- to 13-level cases have been excluded in [23]. Therefore, in this paper, the real implementation of SHE modulation for up to 13-level inverter output is demonstrated.

The evaluation of different output voltage levels and THD performance of single-phase transistor-clamped H-bridge (TCHB) multilevel inverters using SHE modulation has never been reported before. Therefore, a generalized SHE modulation scheme is presented to investigate the performance of a family of TCHB based on cascaded multilevel inverter. The SHE scheme is used in order to eliminate the low-order harmonic components while minimizing the output voltage THD of the adopted inverter. To verify the effectiveness of the proposed SHE modulation, an inverter prototype is built by utilizing a field-programmable gate array (FPGA) as the digital controller. The analytical, simulation and experimental results are presented in this paper.

II. THE TCHB MULTILEVEL INVERTER CONFIGURATION

Fig. 1 depicts the general configuration of the single-phase TCHB inverter topology [13],[24]. Each TCHB inverter unit is added with one bidirectional switch comprised of one transistor with four diodes together with a conventional H-bridge inverter. Table I lists the five modes of operation of the adopted inverter. A five-level voltage output (0, $\pm\frac{1}{2}V_{dc}$ and $\pm V_{dc}$) is produced in a single unit of the TCHB inverter. Half of the output voltages

TABLE I
GENERAL SWITCHING STATES AND THE VOLTAGE LEVELS OF
5-LEVEL TCHB INVERTER

Mode	Switches ON	Voltage level
1	S_{i1}, S_{i4}	$+V_{dc}$
2	S_{i4}, S_{i5}	$+\frac{1}{2} V_{dc}$
3	S_{i1}, S_{i2}	0
	(or S_{i3}, S_{i4})	
4	S_{i2}, S_{i5}	$-\frac{1}{2} V_{dc}$
5	S_{i2}, S_{i3}	$-V_{dc}$

TABLE II
GENERAL COMPARISONS FOR VARIOUS SINGLE-PHASE
N-LEVEL INVERTER TOPOLOGIES

Criteria	TCHB	NPC	FC	CHB
Number of level	n	n	n	n
Power switches	1.25* $(n\text{-}1)$	2* $(n\text{-}1)$	2* $(n\text{-}1)$	2* $(n\text{-}1)$
Power diodes	$n\text{-}1$	2* $(n\text{-}3)$	-	-
DC bus capacitors	$\dfrac{n-1}{2}$	$\dfrac{n-1}{2}$	$\dfrac{n-1}{2}$	$\dfrac{n-1}{2}$
Balancing capacitors	-	-	$2\left[\left(\dfrac{n-1}{2}\right)-1\right]$	-
Isolated DC supplies	$\dfrac{n-1}{4}$	1	1	$\dfrac{n-1}{2}$

are produced through the proper switching of S_{i5} and S_{i2} or S_{i4}, where i is the number of TCHB cells. Through combinations of the "on" state of the switches (S_{i1}-S_{i5}), the cell output voltage V_i is given by:

$$V_i = V_{dc}(S_{i4} - S_{i2})\{\tfrac{1}{2}S_{i5} + |S_{i1} - S_{i2}| \cdot |S_{i3} - S_{i4}|\} \quad (1)$$

This arrangement enables a higher output voltage, owing to the fact that the synthesized AC output voltage is the sum of individual inverter voltages. Note that when the TCHB cells are connected in cascade, the total inverter output voltage V_{inv} is given by:

$$V_{inv} = V_1 + V_2 + ... + V_i \quad (2)$$

Generally, the adopted topology has $4i + 1$ output levels (where i is the number of TCHB cells). Connecting two units of the TCHB inverter in series will produce a 9-level output. Meanwhile, if three units of the TCHB inverter are in series, a maximum of 13-level output is produced.

Table II shows a general comparison between the adopted TCHB topology and the conventional NPC, FC, and CHB multilevel inverter topologies. It is clear that, for the same number of output levels (n-level), the adopted TCHB inverter has a lower number of power switches and isolated DC sources when compared to the conventional multilevel inverter topologies. However, under certain circumstances, such as during a sudden large disturbance or transient conditions, the DC-link capacitor voltages in the TCHB inverter may become unbalanced [24]. Therefore, as discussed in [25], a voltage-balancing technique, either by hardware or software, is
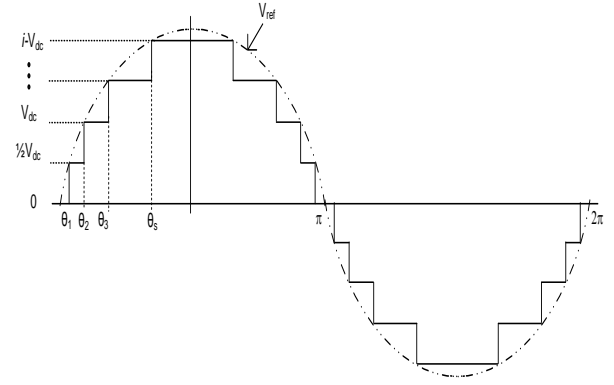

Fig. 2. The inverter output voltage V_{inv} waveform.

required to prevent capacitor voltage imbalances. The simplest approach is to use a larger value for the capacitance [13], [24]. This method is adopted in this paper.

III. BACKGROUND OF SHE MODULATION

The intention of this paper is to produce an output waveform for a single-phase system with the capability to dispose of specific low-order harmonics while maintaining its fundamental voltage. It is possible to determine the switching angle through the Newton-Raphson (NR) method. The NR method is one of the most widely used methods for root-finding. It starts with an initial approximation, and then converges on a good initial guess. In general, the Fourier series of the inverter output voltage V_{inv} (see Fig. 2) is given by:

$$V_{inv}(\omega t) = a_0 + \sum_{n=1}^{\infty}[a_n \cos(n\omega t) + b_n \sin(n\omega t)] \quad (3)$$

As the Fourier series contains only a sine term, the coefficients a_0 and a_n are zero for all of the n harmonics. All of the even harmonics are zero. Therefore, the inverter output voltage V_{inv} waveform can be expressed as [2]:

$$V_{inv}(\omega t) = \frac{2V_{dc}}{n\pi} \sum_{n=1,3,5..}^{\infty}[\cos(n\theta_1) + ... + \cos(n\theta_s)]\sin(n\omega t) \quad (4)$$

where $\theta_1 - \theta_s$ are the switching angles at each level in the first quarter waveform. They need to satisfy the following condition:

$$0 < \theta_1 < \theta_2 < ... < \theta_s < \pi/2 \quad (5)$$

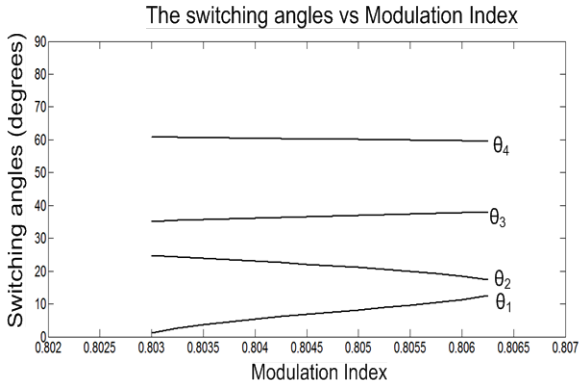From (4), the expression of the fundamental voltage V_1 is given by:

$$\frac{2V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + ... + \cos(\theta_s)] = V_1 \quad (6)$$
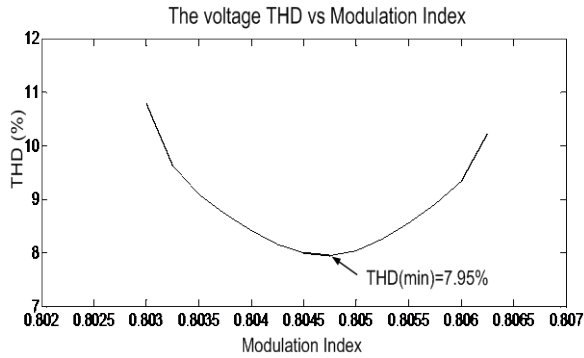
The modulation index M can be defined from (6) as:

$$M = \frac{\pi V_1}{2sV_{DC}} \quad (0 \le M \le 1) \quad (7)$$

where s is the number of positive steps in a quarter waveform.

The switching angles of the adopted inverter in a single-phase system can be obtained by solving the following

(a)

(b)

Fig. 3. The solutions for 9-level inverter. (a) The switching angles. (b) The voltage THD.

(a)

(b)

Fig. 4. The solutions for 13-level inverter. (a) The switching angles. (b) The voltage THD.
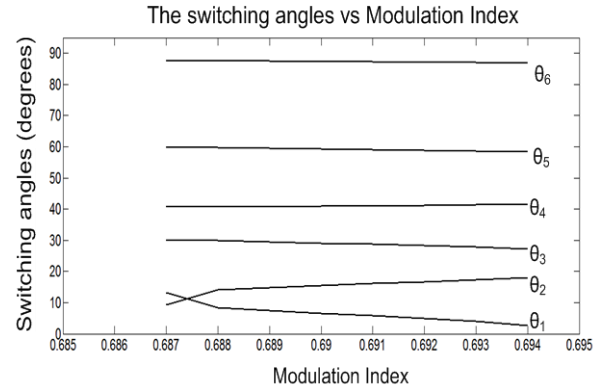
transcendental equations:

$$
\left.\begin{array}{l}
\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_s) = sM \\
\cos(3\theta_1) + \cos(3\theta_2) + \ldots + \cos(3\theta_s) = 0 \\
\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_s) = 0 \\
\quad\quad\quad\quad \vdots \\
\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s) = 0
\end{array}\right\} \quad (8)
$$

In this group of equations, the first equation guarantees the desired fundamental component, while the remaining equations ensure the elimination of specific low-order harmonics as they dominate the THD. The set of switching angles is then examined for its THD to select the best solution, the one with the lowest THD. The computed voltage THD is defined by:
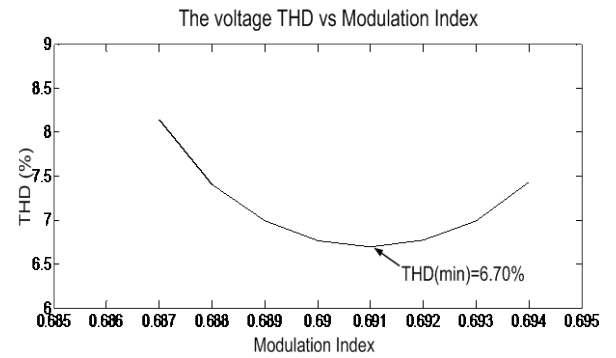
$$
THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad (9)
$$

The following steps are executed to implement the proposed SHE modulation:

1) Calculation of the switching angles is performed in Matlab via the NR method. The solution is computed with an arbitrary initial guess for the switching angles as M is varied from 0 to 1 in steps of 0.001.

2) By utilizing the voltage-angle equal criteria of a sinusoidal reference waveform, the threshold voltages corresponding to the calculated switching angles are

recognized.

3) The gating signals are produced from a correlation of the voltage reference with respect to the threshold voltages and some combinational logics.

A. The SHE Modulation for a 9-level TCHB Inverter

The solution sets of switching angles to cancel the 3rd, 5th and 7th harmonics for a single-phase 9-level TCHB inverter in some of the modulation indices range are depicted in Fig. 3(a). The minimum THD values of these angles is 7.95%. This is calculated according to (9), as shown in Fig. 3(b).

B. The SHE Modulation for a 13-level TCHB Inverter

Either of the switching angles set in Fig. 4(a) can be used in a 13-level TCHB inverter to eliminate the 3rd, 5th, 7th, 9th, and 11th harmonics. Fig. 4(b) shows a 6.7% minimum THD in a single-phase 13-level TCHB inverter.

IV. THE GENERALIZED SHE MODULATION AND ITS IMPLEMENTATION

The generalized SHE modulation for the TCHB inverter family is derived from one sinusoidal reference signal and several triggered voltage levels (V_L and V_H) as illustrated in Fig. 5. The two voltages V_L and V_H are classified as the triggered voltage levels, which correspond to the switching angles of the related cell. For the developed SHE technique, only a
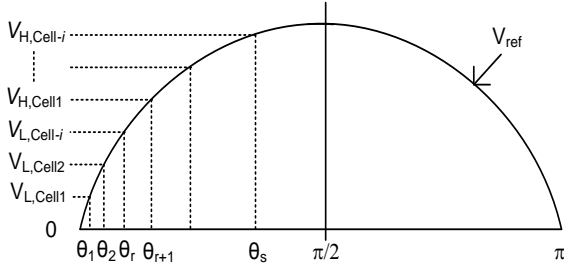
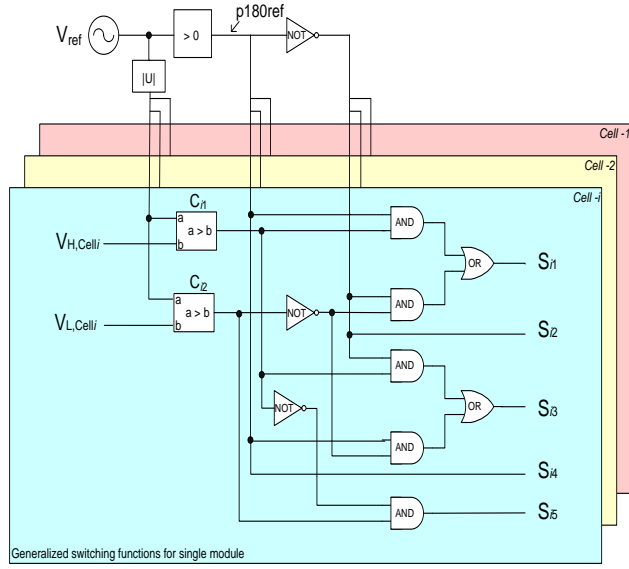Fig. 5. The generalized reference signal and triggered voltages.

Fig. 6. Generalized SHE scheme for TCHB multilevel inverter.

half-wave diagram is illustrated. According to Fig. 5, the reference voltage V_{ref} is defined as:

$$V_{ref} = V_m \sin \omega t \qquad (10)$$

where V_m is an arbitrary (peak) value.

The relationships between the switching angles and the triggered voltage levels in one TCHB cell are provided in the following equations:

$$\left. \begin{array}{l} V_{L,Cell\ i} = \sin(\theta_r \times \pi/180) \times V_m \\ V_{H,Cell\ i} = \sin(\theta_s \times \pi/180) \times V_m \end{array} \right\} \qquad (11)$$

where i is the number of TCHB cells, $r = 1, 2, .. i$, and $s = r + i$.

To perform SHE modulation for the adopted 9-level TCHB inverter topology, a simple calculation for the triggered voltage levels is derived from the calculated switching angles ($\theta_1 - \theta_4$) by using the voltage-angle equal criteria. There are four voltage levels ($V_{L,Cell1}$, $V_{L,Cell2}$, $V_{H,Cell1}$ and $V_{H,Cell2}$) during the positive half-cycle of the modulating signal. These triggered voltage level calculations are based on the angle measurement in radians. Hence, the voltage levels can be computed as follows:

$$\left. \begin{array}{l} V_{L,Cell\ 1} = \sin(\theta_1 \times \pi/180) \times V_m \\ V_{L,Cell\ 2} = \sin(\theta_2 \times \pi/180) \times V_m \\ V_{H,Cell\ 1} = \sin(\theta_3 \times \pi/180) \times V_m \\ V_{H,Cell\ 2} = \sin(\theta_4 \times \pi/180) \times V_m \end{array} \right\} \qquad (12)$$

TABLE III
SWITCHING ANGLES FOR 9-LEVEL AND 13-LEVEL TCHB INVERTERS

No.	Case	Switching Angles (°)
1	9-level	[7.5, 21.6, 36.8, 60.2]
2	13-level	[4.9, 16.8, 28.3, 41.2, 58.9, 87.2]

The sequence is chosen so that cell 1 operates at the angles θ_1 & θ_3, and cell 2 operates at the angles θ_2 & θ_4, in order to avoid over-burdening any particular cell. Moreover, similar approaches can be applied to any angle, any number of voltage levels and any type of multilevel inverter topology.

The proposed SHE modulation requires the two main modules of the sine-wave generator and the combinational logics as illustrated in Fig. 6. The modulus operation of a sinusoidal waveform has been included since the steps of the output voltage in other regions are sequential. The SHE control scheme can be extended to any number of TCHB cells. The switches S_{i1}, S_{i3}, and S_{i5} (where i is the number of TCHB cells) operate by comparing the reference signal with the triggered voltage levels and through the combinational logic gates, while S_{i2} and S_{i4} operate complementarily in the half cycle of the reference signal. The general logic expressions (using AND, OR and NOT gates) for the gating signals are given as follows:

$$\left. \begin{array}{l} S_{i1} = (C_{i1} . p180\,ref) + (\overline{C_{i2}} . \overline{p180\,ref}) \\ S_{i2} = \overline{p180\,ref} \\ S_{i3} = (C_{i1} . \overline{p180\,ref}) + (\overline{C_{i2}} . p180\,ref) \\ S_{i4} = p180\,ref \\ S_{i5} = \overline{C_{i1}} . C_{i2} \end{array} \right\} \qquad (13)$$

where C_{i1} and C_{i2} are the outputs of the comparators and the $p180ref$ signal is the 180° reference based on the frequency of the reference signal, which is also identified as the S_{i4} signal.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

In order to verify the proposed SHE modulation, the adopted inverter is simulated using Matlab/Simulink. Two types of simulation tests are carried out to produce 9-level and 13-level output waveforms. An equal DC voltage input of 200 V was considered for each of the 5-level TCHB inverter modules. The frequency of the inverter was set at 50 Hz. The inverter circuit arrangement was similar to that in Fig. 1. In both configurations, the generated inverter outputs were triggered at the points of the switching angle. The set of switching angles in Table III was selected at the point of minimum THD, from the solution sets plotted in Figs. 3(a) and 4(a) for the 9-level and 13-level TCHB inverters, respectively.

The 9-level TCHB inverter arrangement incorporates two TCHB inverter units and two equal isolated DC sources. The simulation for the 9-level TCHB inverter produced Figs. 7(a) and 7(b). The 9-level inverter's 7.95% voltage THD was
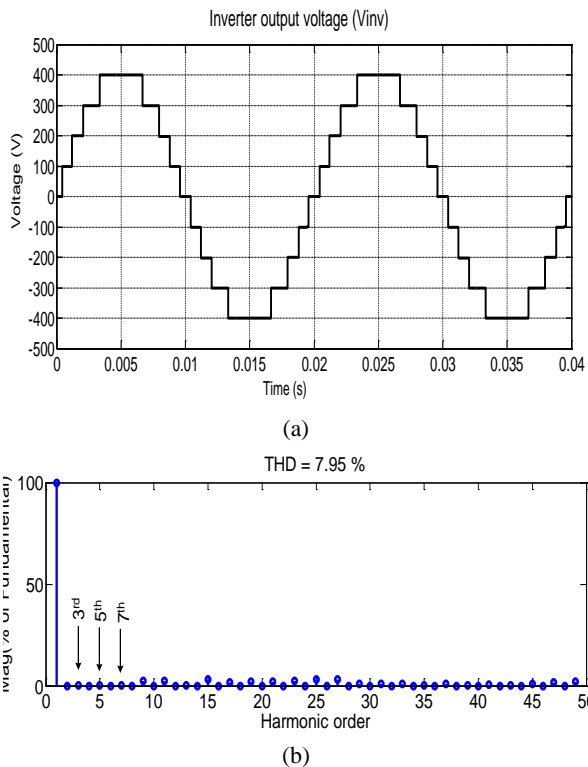
(a)

(b)

Fig. 7. Simulation results of 9-level TCHB inverter. (a) The inverter output voltage. (b) The voltage THD.
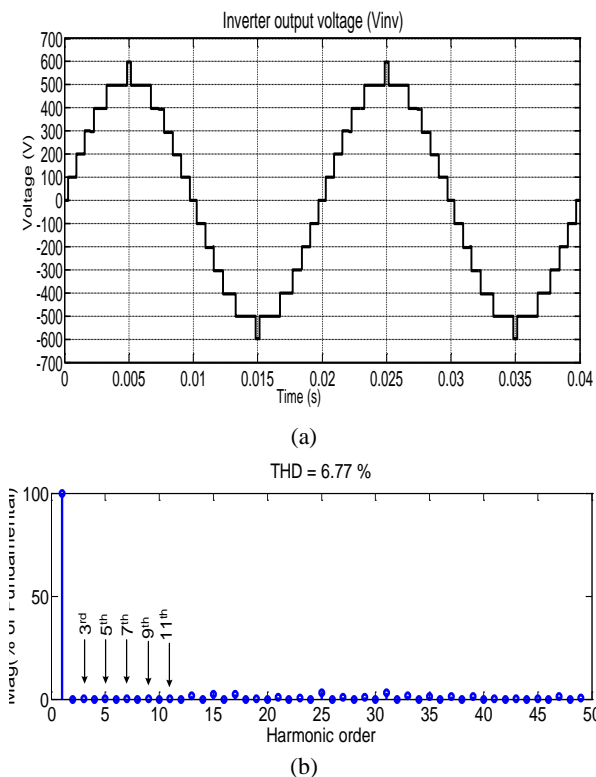

(a)

(b)

Fig. 8. Simulation results of 13-level TCHB inverter. (a) The inverter output voltage. (b) The voltage THD.

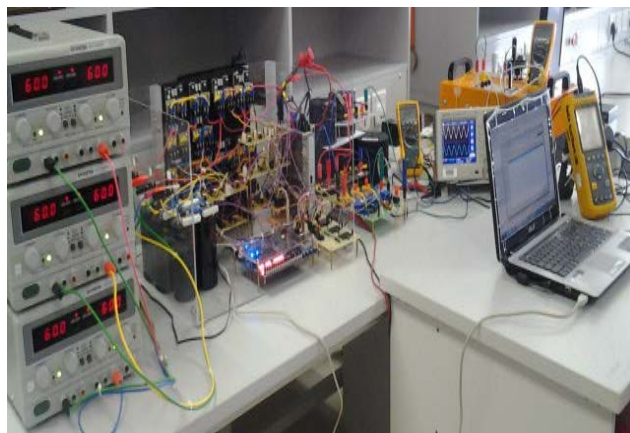similar to the calculated value [see Fig. 3(b)], and only the 3rd, 5th and 7th harmonics were eliminated.

Fig. 9. The overall experimental setup.

<center>TABLE IV
THE EXPERIMENT SPECIFICATIONS</center>

Parameter	Values
DC source for each TCHB module, V_{dc}	120 V
DC-link capacitors	3300 μF
IGBT	IRG4PC50UD
Diode	30CPF12PBF
Load resistance, R	130 ohm
Load inductor, L	81 mH

The 13-level TCHB inverter it is built with three TCHB inverter units and three equal isolated DC supplies. The simulation results for the 13-level TCHB inverter are shown in Figs. 8(a) and 8(b). The 13-level inverter's 6.77% voltage THD paralleled the calculated value [see Fig. 4(b)], and the 3rd, 5th, 7th, 9th, and 11th harmonics were eliminated.

B. Experiment Results

To demonstrate the validity of the proposed SHE control algorithm, a DE2 Altera FPGA board was used as the digital controller. It is a cost-effective board that incorporates a Cyclone II 2C35 FPGA device. The SHE controller was designed by using Verilog high-level description language (HDL) code and schematic design entries in Quartus II software. The corresponding voltages are stored in the FPGA memory and the switching patterns were formed through some combinational logics for real-time application.

A single-phase TCHB inverter prototype has been constructed as depicted in Fig. 9. The experimental parameters for the adopted TCHB multilevel inverter are listed in Table IV. The inverter was supplied by GW Instek (GPC6030D) isolated DC sources with V_{dc} = 120 V for each of the cells. The prototype uses IGBTs (IRG4PC50UD) as the switching devices and power diodes (30CPF12PBF) as part of the bidirectional switch element. Each of the TCHB units uses two 3300 μF electrolyte capacitors as the DC-link capacitors. A large capacitance is used to reduce the effects of the voltage imbalance [13], [24] so that the voltage across each capacitor is maintained at approximately ½V_{dc} throughout the course of the experiment. Two types of loads were set, i.e., a highly resistive load that uses only a resistor R = 130 Ω; while the later for an
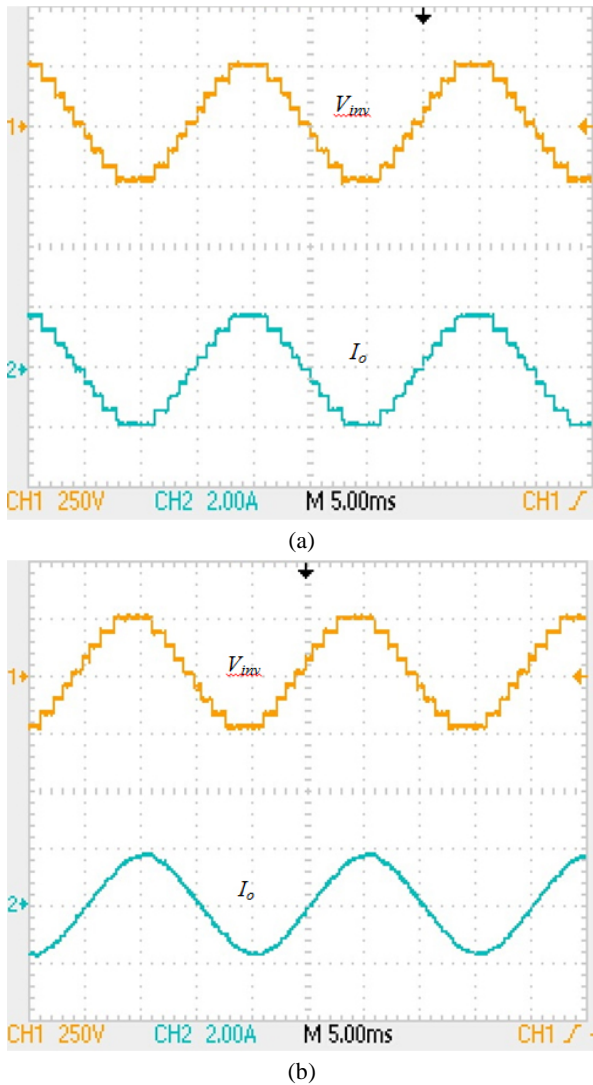
(a)

(b)

Fig. 10. The inverter output voltage and load current for 9-level TCHB inverter. (a)With a resistive load. (b) With an *RL* load.

Fig. 11. The voltage THD of 9-level TCHB inverter.

(a)

(b)

Fig. 12. The 13-level TCHB inverter with an *RL* load. (a) The inverter output voltage and load current (b) The voltage THD.

RL load, $L = 81$ mH is added in series to the resistor. A Tektronix TDS2002 digital oscilloscope was used to measure the voltage and current waveforms. Related data such as the total harmonic distortion (THD), power and power factor are measured using a FLUKE 43B power quality analyzer. The measured voltage THD was recorded for interharmonics up to the 50th harmonic order.

The first experimental setup was constructed for a 9-level TCHB inverter. Figs. 10(a) and 10(b) show the output waveforms of the proposed SHE scheme when tested with a highly resistive load and an *RL* load, respectively. Fig. 11 shows a 8.1% voltage THD where the 3rd, 5th and 7th harmonics were eliminated in the inverter output voltage V_{inv} of the 9-level TCHB inverter topology regardless of the load type.

Another experiment was carried out with a 13-level TCHB inverter. To examine the inverter performance with a higher frequency of 110 Hz, the output waveform for the same *RL* load is illustrated in Fig. 12(a). An inverter output voltage THD
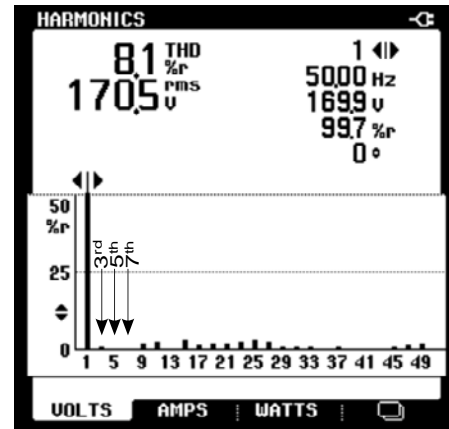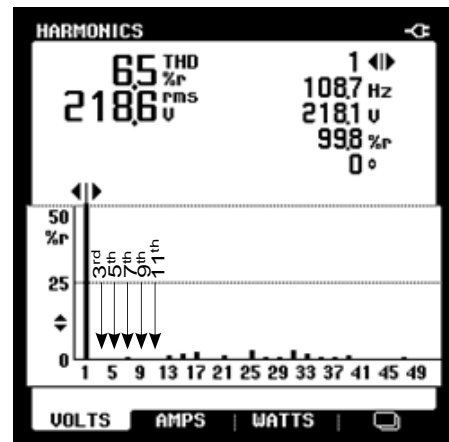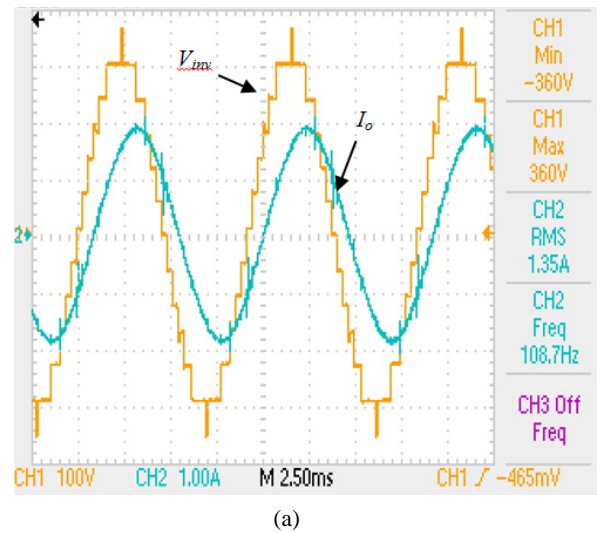
of 6.5% is shown in Fig. 12(b). The 13-level TCHB topology produced a much lower voltage THD and enabled the inverter to eliminate more harmonic components than did the 9-level TCHB. Whatever the load or frequency, five harmonic orders were eliminated (the 3rd, 5th, 7th, 9th and 11th orders) in the
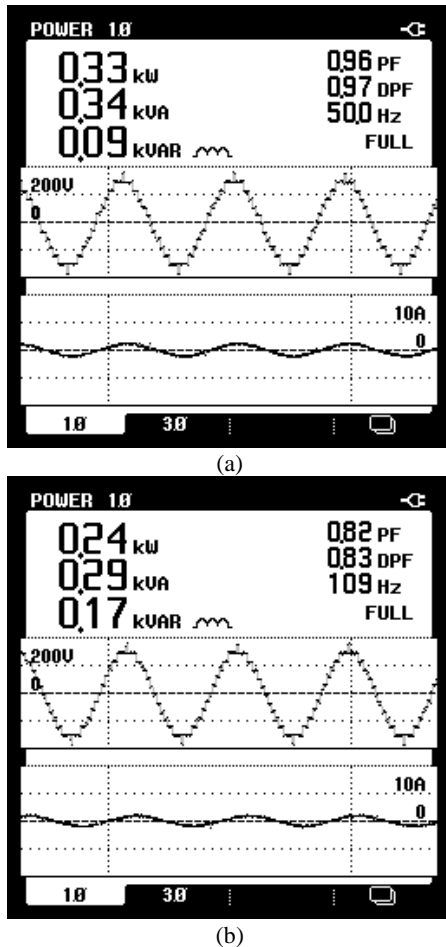
(a)

(b)

Fig. 13. Measured 13-level inverter output power and power factor for different frequencies (a) 50 Hz (b) 110 Hz.
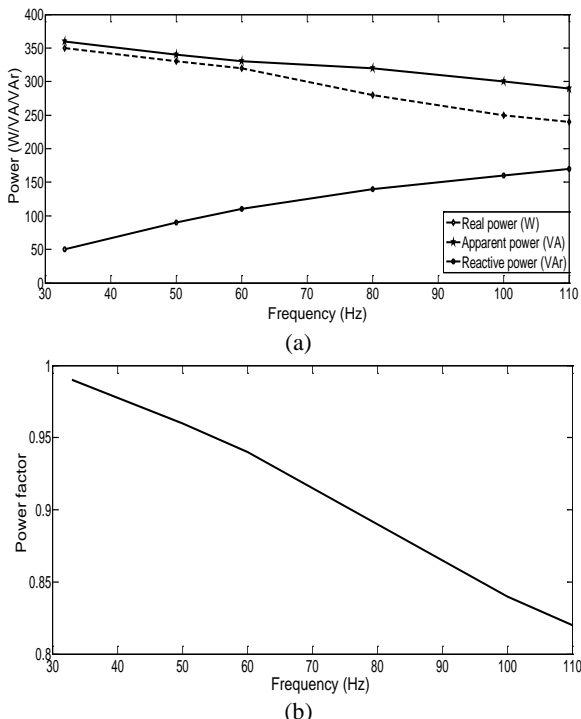

(a)

(b)

Fig. 14. The 13-level TCHB inverter (a) Power distribution against frequency (b) Power factor against frequency.

13-level TCHB inverter topology. The power distribution and power factor for different frequencies (50 Hz and 110 Hz) in the 13-level TCHB inverter with the same RL load parameters are shown in Figs. 13(a) and 13(b). The relationships between the power distribution and the power factor with the changes in frequency appear in Figs. 14(a) and 14(b), respectively. The results indicated that the real power and apparent power decrease with respect to the increase in frequency. However, the reactive power differed. It increased in proportion to the increase in frequency. Meanwhile, the load power factor decreased to become a more lagging pf when the frequency increased.

Both of the inverters produced a consistent stepped-waveform driven at an optimum point of the minimum THD corresponding to the analytical and simulation results. Specific low-order harmonics in the inverter output voltage V_{inv} were eliminated. In the case of a highly resistive load, the load current I_o had a similar stepped waveform as the inverter output voltage V_{inv}. In addition, with the RL load, the load current I_o was sinusoidal.

VI. CONCLUSION

This paper presented a generalized SHE modulation for a family of TCHB-based cascaded multilevel inverter. The SHE scheme was derived based on the Newton-Raphson method. Both simulation and experimental results verified the effectiveness of the SHE modulation for the TCHB inverter topology. It resulted in a dramatic decrease in the THD of the output voltage when there was an increase in the number of steps output. The proposed SHE scheme can be extended to other multilevel inverter topologies, via manipulating the application of the reference signal, the threshold voltage and the combinational logics. This method is precise in terms of harmonics elimination and also simple for practical implementation. Future work using the presented SHE can be carried out for a TCHB inverter with a single DC input source by employing several transformers at the inverter output.

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