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A New Symmetric Cascaded Multilevel Inverter Topology Using Single and Double Source Unit

Jagabar Sathik Mohd. Ali[†] and Ramani Kannan[*]

[†]Dept. of Electrical and Electronics Engg., J. J. College of Engineering and Technology, Tamil Nadu, India
[*]Dept. of Electrical and Electronics Engg., K. S. Rangasamy College of Technology, Tamil Nadu, India

Abstract

In this paper, a new symmetric multilevel inverter is proposed. A simple structure for the cascaded multilevel inverter topology is also proposed, which produces a high number of levels with the application of few power electronic devices. The symmetric multilevel inverter can generate 2n+1 levels with a reduced number of power switches. The basic unit is composed of a single and double source unit (SDS-unit). The application of this SDS-unit is for reducing the number of power electronic components like insulated gate bipolar transistors, freewheeling diodes, gate driver circuits, dc voltage sources, and blocked voltages by switches. Various new algorithms are recommended to determine the magnitude of dc sources in a cascaded structure. Furthermore, the proposed topology is optimized for different goals. The proposed cascaded structure is compared with other similar topologies. For verifying the performance of the proposed basic symmetric and cascaded structure, results from a computer-based MATLAB/Simulink simulation and from experimental hardware are also discussed.

Key words: Multilevel Inverter, Optimal Structure, Power Conversion, Power Semiconductor Switches, Total Harmonic Distortion (THD)

I. INTRODUCTION

The multilevel inverter is a kind of dc/ac power converter that produces a desired stepped-like sinusoidal output voltage waveform from an available dc input source [1], [2]. In recent years, this inverter has been widely recommended for medium and high power applications [3]. The important advantages of multilevel inverters are high quality output voltage, low harmonic distortion, low electromagnetic interference, low switching frequency, and low voltage stress on switches [4]. The technical and economic aspects of multilevel inverter development include modular realization, high availability, failure management, investment, and life-cycle cost [5]. Some applications of multilevel inverters include industrial drives, automotive applications, Flexible AC Transmission Systems (FACTS), and traction drive applications [6], [7]. Conventional multilevel inverters are of three types—diode clamped (NPC) [8], flying capacitor (FC) [9], and cascaded H-bridge (CHB) multilevel inverters [10].

The CHB multilevel inverter has received special attention due to its modularity, simple control techniques, reliability, and the absence of capacitor imbalance issues [11]. CHB multilevel inverters are mainly classified into two groups—symmetric and asymmetric multilevel inverters [12]. In symmetric CHB multilevel inverters, the magnitude of all dc voltage sources are equal, requiring an increased number of Insulated Gate Bipolar Transistors (IGBTs) and power diodes, as well as separate dc sources to generate many output levels [13]. These features lead to an increase in installation space and in the total cost of this inverter. In the asymmetric topology, the magnitude of dc voltage sources are unequal. The magnitude of a dc voltage source can be determined using various algorithms. The major advantage of the asymmetric CHB topology is it can considerably increase the number of output voltage levels using few dc voltage sources and IGBTs; however, this topology may also require a variety of dc voltage sources, which is a significant disadvantage. Several novel topologies, along with different new algorithms, for determining the magnitude of dc source voltages have been proposed [14]-[18]. These topologies increase the number of output voltage levels with reduced dc

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[†]Corresponding Author: jagabarsathik@gmail.com
Tel: + 91-431-2695606, J. J. College of Engineering and Technology
[*]Dept. of Electrical and Electronics Engg., K. S. Rangasamy College of Technology, India

sources and minimum switches. However, power electronic components required therein are high.

In this paper, a basic single-phase symmetric multilevel inverter unit is discussed, and a cascaded structure for which is recommended for its use in high power applications. A cascaded structure can generate the maximum number of output voltage levels with a reduced number of dc sources and power electronic components. For generating different levels (both even and odd levels), new algorithms are proposed to determine the magnitude of dc sources. The optimal topology is discussed in the terms of the best of the proposed algorithms. The proposed topology, with its best algorithm, is then compared with the conventional topology and other topologies in existing literature. The amount of voltage blocked by switches and the required number of power electronic components are the factors considered in these comparisons. This paper is arranged as follows: (i) Basic Unit, (ii) Recommended Cascaded Structure, (iii) Optimal Topologies, (iv) Comparison with Other Topologies, (v) Simulation and Experimental Results Verification, and (vi) Conclusion.

II. Basic Unit

The proposed basic symmetric multilevel inverter presented in [19] comprises a single and double source unit (Fig. 1). The single source unit consists of IGBTs in series/parallel connection, as shown in Fig. 1(a). The dc source V_1 is connected in series with switch S_1 *(voltage adder switch)* and parallel switch P_1 *(voltage subtractor switch)*—this basic unit is called a single source unit *(SS-Unit)*. The double source unit is composed of two dc sources, along with two IGBTs in series/parallel connection. The dc sources, V_1 and V_2, are connected in series with switch S_1 and in parallel with switch P_1; this unit is often referred to as a double source unit *(DS-Unit)*, as shown Fig. 1(b). When single and double source units are combined, the result is a single and double source multilevel inverter (SDSMLI). In the proposed structure, the power switches (S_1, P_1), (S_2, P_2), …(S_j, P_j) should not be turned on simultaneously with the dc voltage sources $(V_1, V_2, \ldots V_{n-1})$, respectively, to prevent short circuiting. The suggested basic unit is divided into the following two sections: (i) The combined single and double source sub module is called the level generator unit; (ii) The series connection of the H-bridge inverter is called the polarity changer. This topology has separate generalized structures for both odd and even sources, as shown in Figs. 1(c) and 1(d), wherein n is the number of dc voltage sources, which are separated by series-connected unidirectional controlled power switches $(S_1, S_2, S_3, \ldots S_j)$ and are parallel with $(P_1, P_2, P_3, \ldots P_i)$ switches.

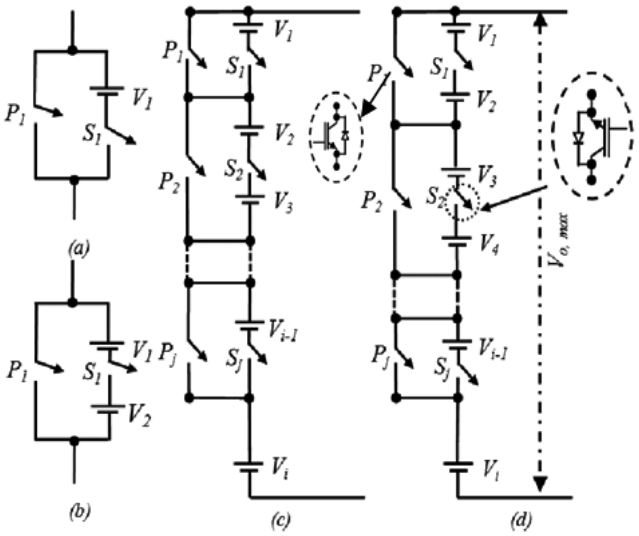


Fig. 1. (a) Basic single source unit. (b) Basic double source unit. (c) Generalized structure for odd number of sources. (d) Generalized structure for even number of sources.

The n_{th} dc source is represented as V_i. In this unit, V_i is not connected with any parallel switch. Presented in Table I are the switching pattern for n number of dc sources, wherein 1 and 0 represent ON and OFF switches, respectively.

The corresponding switches are turned on to synthesize a positive stepped waveform in the level generator; the H-bridge unit is used to create a current flow in both directions at the load terminals. The maximum output voltage $(V_{o,\,max})$ *is* the sum of all dc source voltages, given as:

$$V_{o,max} = V_1 + V_2 + \cdots\cdots + V_n \tag{1}$$

$$V_{o,max} = \sum_{i=1}^{n} V_i \tag{2}$$

(1) and (2) illustrate the stepped dc/dc output voltage level waveform generated by the level generator unit.

The H-bridge unit is synthesized for both positive and negative output voltage levels at the load ($\boldsymbol{V_{out}}$).

The output voltage at (V_{out}) is expressed as follows:

$$V_{out} = \begin{cases} \sum_{i=1}^{n} +V_i & H_{S1}, H_{S4} = 1 \\ \sum_{i=1}^{n} -V_i & H_{S2}, H_{S3} = 1 \end{cases} \tag{3}$$

where H_{S1}–H_{S4} are H-bridge switches. The number of output voltage levels (N_{Level}), number of IGBTs (N_{IGBT}), and the number of dc sources (n) are calculated as follows.

$$N_{level} = 2n + 1 \tag{4}$$

In the proposed topology structure, the number of odd dc sources is different from the number of even dc sources; thus, must express the number of IGBTs required for given output levels and number of dc sources, as in equation (5).

TABLE I
GENERALIZED SWITCHING PATTERN FOR BASIC SYMMETRIC MULTILEVEL INVERTER

State	Voltage Subtractor Switches						Voltage Adder Switches					Voltage Levels ($V_{o,max}$)
	P_1	P_2	P_3	…	$P_{(j-1)}$	P_j	S_1	S_2	…	$S_{(j-1)}$	S_j	
1	1	1	1	…	1	1	0	0	…	0	0	V_i
2	0	1	1	…	1	1	1	0	…	1	0	V_i+V_1
3	1	0	0	…	1	0	0	1	…	0	1	$V_i+V_{i-1}+V_1$
4	1	0	0	…	0	0	0	0	…	1	1	$V_i+V_1+V_2+V_3$
⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮
n-k	1	0	0	…	0	0	0	1	…	1	1	$\sum_{i=1}^{n-k} V_{n-k}$
⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮
n-1	1	0	0	…	0	0	0	1	…	1	1	$\sum_{i=1}^{n-1} V_{n-1}$
n	0	0	0	…	0	0	1	1	…	1	1	$\sum_{i=1}^{n} V_n$

$$N_{IGBT} = \begin{cases} n+5 & ,n = odd \\ n+4 & ,n = even \end{cases} \quad (5)$$

Determination of the required number of single and double source sub-modules is calculated on the basis of the given *n* of dc sources, as follows:

For even number of *n*:

$$DS-Unit = {}^{n-2}\!/_{2} \quad (6)$$

$$SS-Unit = 1 \quad (7)$$

For odd number of *n:*

$$DS-Unit = {}^{n-3}\!/_{2} \quad (8)$$

$$SS-Unit = 2 \quad (9)$$

The SDSMLI can generate high number of output voltage levels with a low number of IGBTs.

In this proposed topology, the maximum blocking voltage of level generator switches are reduced because separate dc sources are connected in series/parallel, leading to reduced voltage ratings of the protecting circuits for power devices. However, these effects do not apply in the H-bridge unit (polarity changer), which is required to withstand high voltage values. For protecting the H-bridge switches, the proposed topology may need some high voltage protecting circuits to protect the power devices. This requirement is the remarkable disadvantage of H-bridge (polarity changer) -based multilevel inverters.

III. RECOMMENDED CASCADED STRUCTURE

The SDSMLI topology has a few drawbacks, discussed as follows. This proposed symmetric topology requires high-blocking voltage switches at the H-bridge unit and an increased number of dc sources required to generate an increased number of output voltage levels. These requirements significantly increase the cost of the multilevel inverter. To rectify these problems, a cascaded structure of the basic symmetric multilevel inverter is proposed for high power applications. The basic symmetric multilevel inverter is only suitable for medium-power applications. This cascaded structure can generate an increased number of output voltage levels with minimum dc sources and IGBTs. The cascaded connection of the proposed SDSMLI is discussed in this section. The novel cascaded multilevel inverter topologies presented in [14]-[18], and the CHB (binary and trinary configuration), the last or the k^{th} sub-multilevel inverter unit should withstand high magnitudes of dc source voltages. Thus, the k^{th} sub-multilevel inverter unit switches of the proposed cascaded structure should have high voltage ratings. Nonetheless, the proposed topology requires minimal IGBTs, reduced dc sources, and reduced variety of dc source voltages. The cascaded connection of the basic symmetric multilevel inverter is shown in Fig. 2. The cascaded structure consists of sub-multilevel units (basic symmetric multilevel inverters) connected in series. These individual sub-multilevel inverters should have an equal magnitude of dc source voltages. Presented in Table II are the different switching patterns of the cascaded structure for generating maximum output voltage levels.

The individual sub-multilevel outputs are represented as $V_{01}, V_{02} \ldots V_{0k}$. The sum of all sub-multilevel output voltages is $\boldsymbol{V_{out}}$ $\left(Vout = V_{01} + V_{02} + \cdots + V_{0k}\right)$.

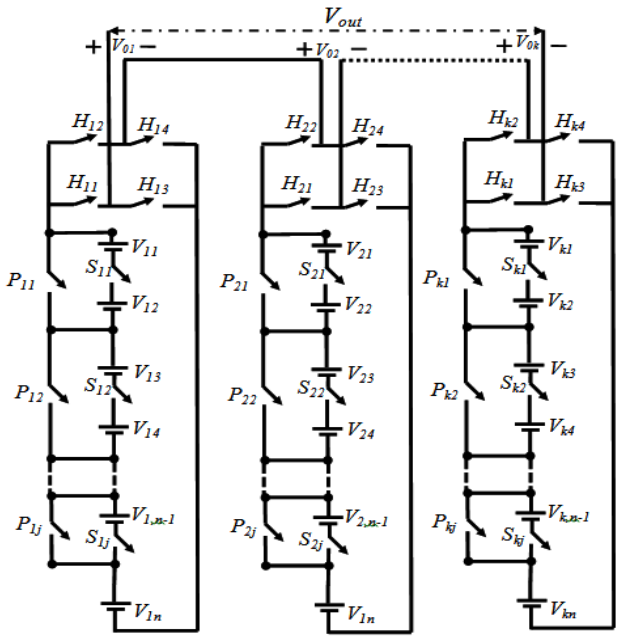


Fig. 2. Recommended cascaded single and double source multilevel inverter topology.

TABLE II
VALUES OF V_{OUT} FOR DIFFERENT STATES OF THE SWITCHES

States	On State Switches						V_{out}
1	-	-	-	-	H_{11}	H_{12}	0
2	P_{11}	P_{12}	-	P_{1j}	H_{11}	H_{14}	$+V_{1n}$
3	P_{11}	P_{12}	-	P_{1j}	H_{12}	H_{13}	$-V_{1n}$
4	P_{11}	P_{12}	-	S_{1j}	H_{11}	H_{14}	$+(V_{1n}+V_{n-1})$
5	P_{11}	P_{12}	-	S_{1j}	H_{12}	H_{13}	$-(V_{1n}+V_{n-1})$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2n	S_{1j}	S_{1j-2}	-	S_{1j}	H_{11}	H_{14}	$\sum_{l=1}^{n_1} V_{1,l}$
2n+1	S_{1j}	S_{1j-2}	-	S_{1j}	H_{12}	H_{13}	$-\sum_{l=1}^{n_1} V_{1,l}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\prod_{l=1}^{k}(2n_l+1)-1$	S_{1j}	S_{2j}	-	S_{kj}	H_{k2}	H_{k3}	$-\sum_{l=1}^{n_k} V_{kl}+\sum_{l=1}^{k-1}\sum_{l=1}^{n_l} V_{1l}$
$\prod_{l=1}^{k}(2n_l+1)-1$	S_{1j}	S_{2j}	-	S_{kj}	H_{k2}	H_{k4}	$\sum_{l=1}^{n_k} V_{kl}+\sum_{l=1}^{k-1}\sum_{l=1}^{n_l} V_{1l}$

TABLE III
DIFFERENT PROPOSED ALGRITHMS AND THEIR RELATED PARAMETERS

Algorithm	Determination of the DC voltage magnitude	$V_{o,max}$	$N_{Variety}$	N_{Level}
Algorithm 1	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=V_{dc}$ $V_{ki}=V_{k1}=V_{dc}$ for $i=1,2,3\cdots n$	nkV_{dc}	1	$(2nk+1)$
Algorithm 2	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=2V_{dc}$ $V_{ki}=V_{k1}=kV_{dc}$ for $i=1,2,3,\cdots n$	$3(k-1)n$	k	$2\sum_{j=1}^{k}(n*j)+1$
Algorithm 3	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=nV_{11}$ $V_{ki}=V_{k1}=n^{(k-1)}V_{dc}$ for $i=1,2,3\cdots n$	$\sum_{j=1}^{k} n^j$	k	$2\sum_{j=1}^{k} n^j+1$
Algorithm 4	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=2V_{dc}$ $V_{ki}=V_{k1}=2^{(k-1)}V_{dc}$ for $i=1,2,3\cdots n$	$(2^j-1)*n$	k	$(2^j-1)*2n+1$ $j=2,.....k$
Algorithm 5	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=3V_{dc}$ $V_{ki}=V_{k1}=3^{(k-1)}V_{dc}$ for $i=1,2,3\cdots n$	$\sum_{i=1}^{k}(n_i\times V_{i1})$	k	$(3^j-1)*n+1$ $j=2,.....k$
Algorithm 6	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=(n_1+1)V_{dc}$ $V_{3i}=V_{31}=(n_1+1)(n_2+1)V_{dc}$ $V_{ki}=V_{k1}=\prod_{i=1}^{k-1}(n_i+1)V_{dc}$ for $i=1,2,3\cdots n$	$\prod_{j=1}^{k}(n_j+1)-1$	k	$2\prod_{j=1}^{k}(n_j+1)-1$
Algorithm 7	$V_{1i}=V_{11}=V_{dc}$, $V_{2i}=V_{21}=V_{11}+2\sum_{i=1}^{n}V_{1i}$ $V_{3i}=V_{31}=V_{11}+2\sum_{i=1}^{n}V_{1i}+2\sum_{i=1}^{n}V_{2i}$ $V_{ki}=V_{k1}=\prod_{i=1}^{k-1}(2n_i+1)V_{dc}$ for $i=1,2,3\cdots n$	$\sum_{i=1}^{k}(n_i\times V_{i1})$	k	$\prod_{i=1}^{k}(2n_i+1)V_{dc}$

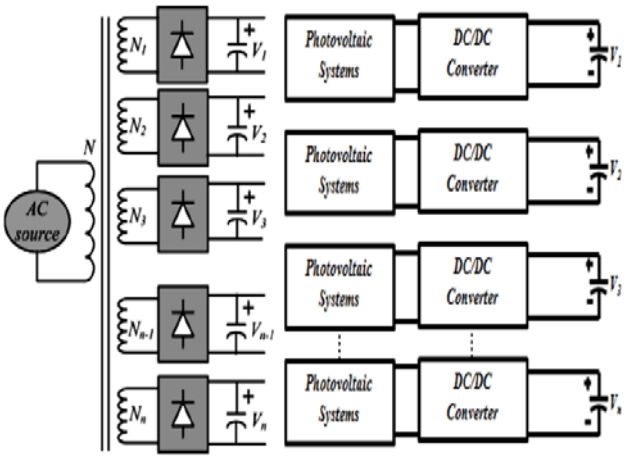


Fig. 3. Arrangement of the dc voltage source. (a) using multiwinding transformer, (b) using photovoltaic system.

For simplicity, switches in the on-state are presented in Table II. . A zero-voltage level at the output voltage can be generated using different switching states.

In Table II, one state is presented and any one of the series/parallel switches presented therein can be switched on to generate the desired output voltage. Different algorithms are discussed to determine the magnitude of the dc source voltages for each individual symmetric sub-multilevel inverter, as listed in Table III. The suggested topology is asymmetric; thus, the new algorithms produce symmetric magnitude values of dc source voltages for each sub-multilevel inverter.

In the following algorithms, the base value of V_{dc} is assumed. The proposed topology requires multiple dc voltage sources, which can be directly provided by a photo-voltaic panel or a multi-winding transformer, as shown in Figs. 3(a) and 3(b). If each individual sub-multilevel inverter has a different dc voltage magnitude, a different output voltage rating of photo-voltaic panel or a different ratio for the secondary winding turn of the transformer may be required. This requirement may reduce the efficiency of the multilevel inverter.

In order to avoid such a problem, the individual sub-multilevel units should have the same dc source magnitude values. However, photo-voltaic panel outputs are not constant. Thus, with regard to ensuring a constant output, the dc/dc converter and MPPT algorithms are preferred [20]-[22]. Table III describes different algorithms , their possible output voltage levels and variety of dc sources. Each sub-multilevel inverter may require a *k* variety of dc voltage magnitudes because each inverter has a dc source voltage magnitude equal to the other inverters. The proposed cascaded structure can generate both odd and even levels using the proposed algorithms. The maximum amount of

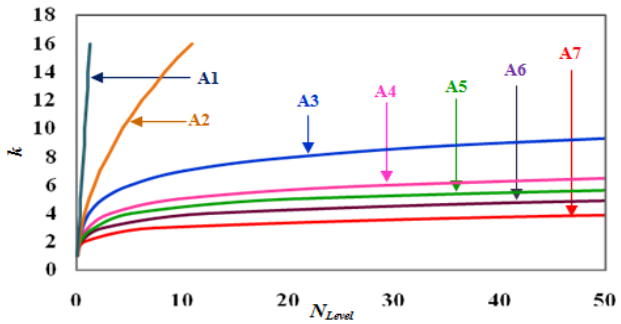


Fig. 4. Number of levels against k and constant *n*.

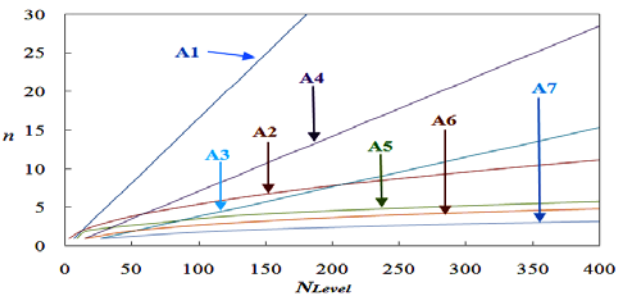


Fig. 5. Number of levels against *n* and constant *k*..

output voltage levels can be generated using the proposed algorithms, as demonstrated in Fig. 4 and 5.

The cascaded structure consists of an *n* number of dc sources and a *k* number of sub-multilevel inverters connected in series. In Fig. 4, *n* is kept constant (*n=4)* and the number of possible output voltage levels against different *k* is compared. Several *n* with a constant *k* are shown in Fig. 5, wherein the number of output voltage levels against a different *n* is shown. In both approaches, Algorithm-7 produces a high number of output voltage levels. The generalized equation for the total number of IGBTs is as follows:

$$N_{IGBT,T} = (n+4)k \quad for\ n = even$$
$$N_{IGBT,T} = (n+5)k \quad for\ n = odd \qquad (10)$$

Fig. 6 illustrates the required number of switches against output voltage levels under all the proposed algorithms. Evidently, Algorithm-7 produces a high number of output voltage levels with a few switches. However, the number of dc sources and the number of IGBTs is equal between all sub-multilevel inverters.

In Fig. 6 shows the required number of IGBTs for each sub-multilevel inverter under a constant number of dc sources. Algorithm-7 produces the maximum output voltage with the minimum number of IGBTs, dc sources, and variety of dc sources. Thus, Algorithm-7 is considered for the optimal topology. This topology is discussed in the following section.

IV. Optimal Topologies

As mentioned, Algorithm-7 is considered for the optimal topology because it can generate the maximum number of output voltages with minimal IGBTs.

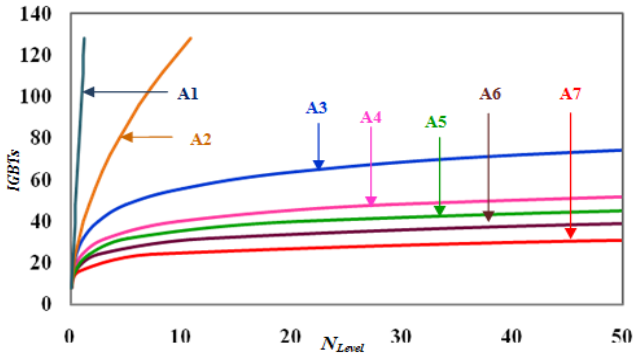


Fig. 6. Number of levels against the number of IGBTs.

A. Optimization of the Recommended Cascaded Topology for the Maximum Number of Voltage Steps with a Constant Number of IGBTs

The number of switches in each sub module is considered equal, that is,

$$n_1 = n_2 = n_3 = \cdots = n_k = n$$

In terms of IGBTs,

$$N_{IGBT,even} = (n_1 + n_2 + n_3 + \cdots + n_k) + 4k$$

$$N_{IGBT,even} = \sum_{i=1}^{k} (n_i + 4) \quad (11)$$

$$N_{IGBT,odd} = (n_1 + n_2 + n_3 + \cdots + n_k) + 5k$$

$$N_{IGBT,odd} = \sum_{i=1}^{k} (n_i + 5) \quad (12)$$

As shown in the preceding equation,

$$k = \frac{N_{IGBTs}}{n+4} \quad For\ even \quad (13)$$

$$k = \frac{N_{IGBTs}}{n+5} \quad For\ odd \quad (14)$$

The number of dc sources *(n)* in each sub-module must be determined. The maximum number of voltage levels can be obtained as follows:

$$N_{level} = (2n+1)^k \quad (15)$$

Using Equations (13), (14), and (15), the number of voltage levels in terms of the IGBTs can be calculate as follows:

$$N_{Level} = \left[(2n+1)^{1/n+4}\right]^{N_{IGBTS}} - even\ n \quad (16)$$

$$N_{Level} = \left[(2n+1)^{1/n+5}\right]^{N_{IGBTS}} - odd\ n \quad (17)$$

Fig. 7 shows the variation of $\boldsymbol{N_{Level}}$ against the number of dc sources *(n)*. The maximum number of output voltage levels can be obtained with a constant number of switches when *n=2* and *n=4* (an even number of dc sources can produce a maximum number of voltage levels with a minimum number of IGBTs, compared with an odd number of dc sources).

B. Optimization of the Proposed Cascaded Topology for the Maximum Number of Levels with a Constant Number of dc Voltage Sources

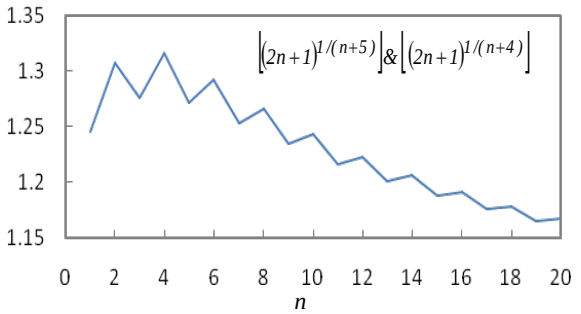


Fig. 7. Variation of $\left[(2n+1)^{1/n+5}\right]$ - *odd n* and $\left[(2n+1)^{1/n+4}\right]$ - *even n* against n

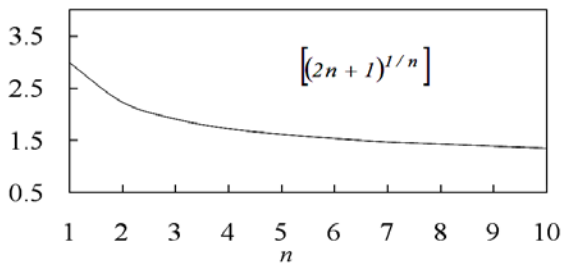


Fig. 8. Variation of $[(2n+1)^{1/n}]$ against n.

As mentioned, each sub-module has an equal number of dc sources, as follows:

$$n_1 = n_2 = .\cdots\cdots = n_k = n$$

The recommended topology cascaded series of sub-module consists of n_i dc voltage sources.

$$Nsource = \sum_{i=1}^{k} n_1 + n_2 + \cdots + n_k \quad (18)$$

The general form of the *k* sub-module dc voltage sources is $N_{Source} = n \times k$

$$N_{Level} = [(2n+1)^{1/n}]^{Nsources} \quad (19)$$

As clearly shown in Fig. 8, the maximum number of voltage steps are obtained from *n=1*. Thus, a topology that considers each unit with one dc voltage source provides the maximum number of output voltage levels with the minimum number of dc sources (i.e., the conventional cascaded multilevel inverter)

C. Optimization of the Proposed Cascaded Converter for the Minimum Number of IGBTs with a Constant Number of Levels

The next objective to optimize the proposed structure to allow it to generate $\boldsymbol{N_{Level}}$ with the minimum number of IGBTs $\boldsymbol{(N_{IGBTs})}$.

$$N_{IGBTs} = ln(N_{Level}) \times \frac{n+4}{ln(2n+1)} - even\ n \quad (20)$$

$$N_{IGBTs} = ln(N_{Level}) \times \frac{n+5}{ln(2n+1)} - odd\ n \quad (21)$$

To keep $\boldsymbol{N_{Level}}$ constant to express the minimum number of IGBTs; (20) and (21) express the required constant IGBTs under each level for odd and even numbers of dc sources,

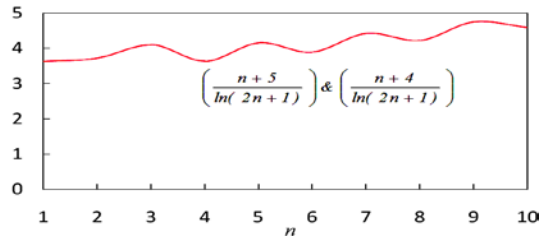


Fig. 9. Variation of $\left(\frac{n+5}{ln(2n+1)}\right)\&\left(\frac{n+4}{ln(2n+1)}\right)$.

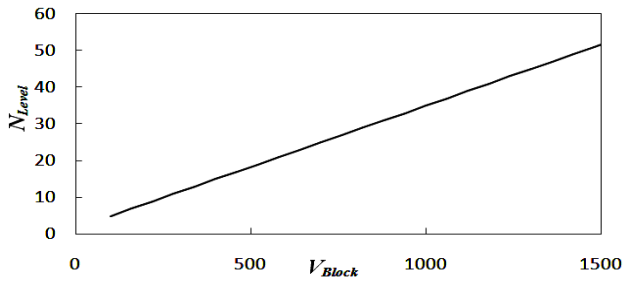


Fig. 10. Number of Levels Vs V_{Block}.

respectively. As illustrated in Fig. 9, the minimum number of IGBTs is required when number of dc sources *n* is even. (i.e., *n=2* and *n=4*).

D. Optimization of the Recommended Cascaded Topology for the Minimum Blocking Voltage of Switches with a Constant Number of Levels

In this section, to determine the minimum value of blocking voltage for the switchesare calculated as follows .

$$V_{Block} = V_{Switch,U} + V_{Switch,HB} = \sum_{i=1}^{k} V_{Switch,U}(k) + \sum_{i}^{k} V_{Switch,H}(k) \quad (22)$$

where $V_{Switch,U}$ and $V_{Switch,HB}$ are the peak voltages of the *Single & Double Source Unit (Level Generator Part)* and the *H-bridge Unit*, respectively.

Single Source Unit:

$$V_{S1,1} = V_{Sk,1} = V_{k,1} \quad (23)$$

Double Source Unit:

$$V_{S1,2} = V_{S1,3} = \cdots\cdots = V_{Sk,j-1} = 2V_{k,1} \quad (24)$$

The peak voltage of the level generator part is the sum of all voltages across each switch.

The generalized formula ($V_{Switch,U}$) :

First unit:

$$V_{Switch,U} = 2\times(n-1)V_{1,1} \quad (25)$$

k^{th} Unit:

$$V_{Switch,U(k)} = 2\times(n_k - 1)V_{k,1} \quad (26)$$

Considering (25) and (26), define the general form for the peak voltage of the level generator unit can be written as follows:

$$\sum_{j=1}^{k} V_{Switch,U(j)} = 2\times(n-1)\sum_{i=1}^{k} V_{i,k} \quad (27)$$

Blocking Voltage for the H -Bridge Unit:

First unit:

$$V_{Switch,H} = 2\times n\times V_{1,1} \quad (28)$$

k^{th} unit:

$$V_{Switch,H(k)} = 2\times n_k \times V_{k,1} \quad (29)$$

Considering (43) and (44), the general form for the peak voltage of the H-bridge unit as follows:

$$\sum_{j=1}^{k} V_{switch,H(j)} = 2n\times\sum_{i=1}^{k} V_{i,1} \quad (30)$$

Therefore, the peak voltage of the proposed cascaded multilevel inverter can be calculated as

$$V_{Block} = \sum_{i=1}^{k} V_{i,1}(2(n-1)+2n) = \sum_{i=1}^{k} V_{i,1}(4n-2) \quad (31)$$

V. Comparison with Other Topologies

To show the capabilities of the proposed topology, the comparison with other recommended topologies in existing literature, as shown in Fig. 11. The cost function (CF) of the multilevel inverter can be determined as:

$$CF = N_{IGBT} + N_{Driver} + N_{Variety} + \beta V^{pu}_{Switch} \quad (32)$$

The multilevel inverter cost can be evaluated by (32). The cost function consists of the following: the number of IGBTs, the number of driver circuits, the variety of dc sources and blocking voltages of switches (per unit base value), and β (weight factor of the blocked-voltage switches). In this section, each parameter of the cost function between the similar topologies and the CHB (trinary configuration) is compared.

A. Comparison of the Required IGBTs and Freewheeling Diodes

This paper aims to reduce the number of IGBTs in multilevel inverters. In a multilevel inverter, the IGBT is one of the factors that determine total cost. An increase in IGBTs leads to an increase in cost, a large installation area, a complex switching pattern, and difficulty in controlling switches.

The recommended topologies in [15] and [17] have been used with bidirectional switches (composed of two IGBTs). On the contrary, the proposed topology, [14], [16], and [18] are composed of one IGBT. The comparison of different topologies against the proposed topology has been presented in Fig. 12. An even number of dc sources synthesizes a higher number of output voltage levels than an odd number of dc sources. Clearly, the even dc source of the proposed topology and [R18] requires minimal IGBTs. In addition, [R18] requires *n* number of power diodes for *n* dc sources, which can lead to a poor efficiency in the multilevel inverter (e.g., voltage spikes at output voltages). A comparison of the proposed topology and the CHB trinary configuration is shown in Fig. 13. The proposed topology and the CHB trinary configuration requires

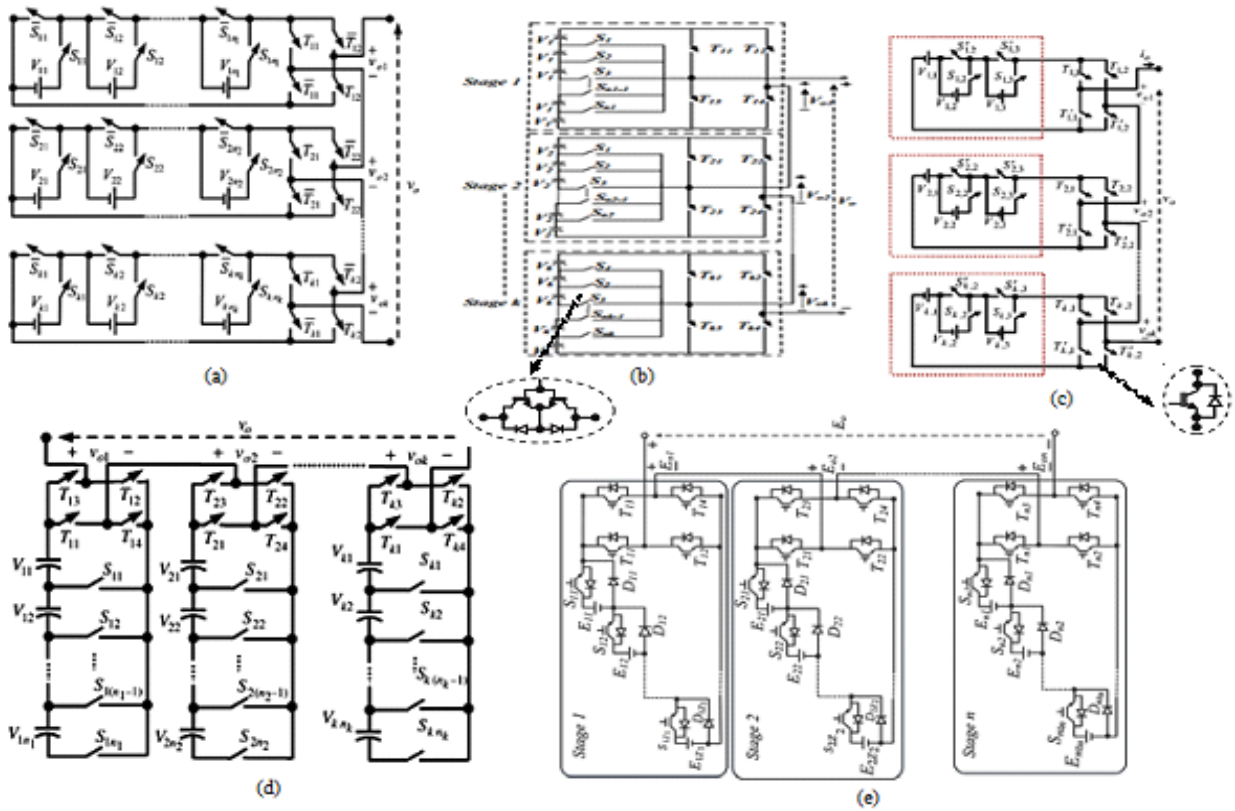


Fig. 11. Cascaded structure of the recommended topologies presented in literature; (a) presented in [14], named [R14], (b) presented in [15], named [R15], (c) presented in [16], named [R16], (d) presented in [17], named [R17], (e) presented in [18], named [R18]. All topologies consider that $V_{1i}=V_{11}=V_{dc}, V_{2i}=V_{21}=V_{11}+2\sum_{i=1}^{n}V_{1i}$, $V_{ki}=V_{k1}=\prod_{i=1}^{k-1}(2n_i+1)V_{dc}$.

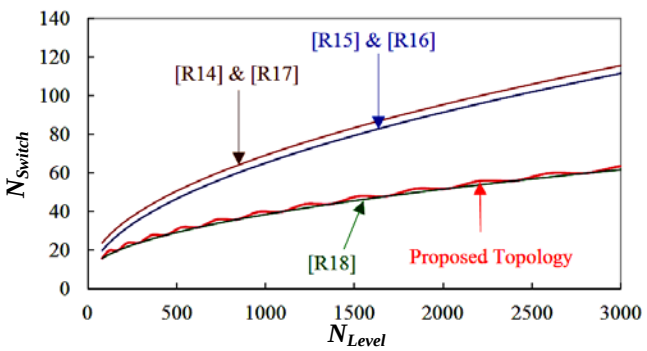


Fig. 12 Comparison of number of levels and switches

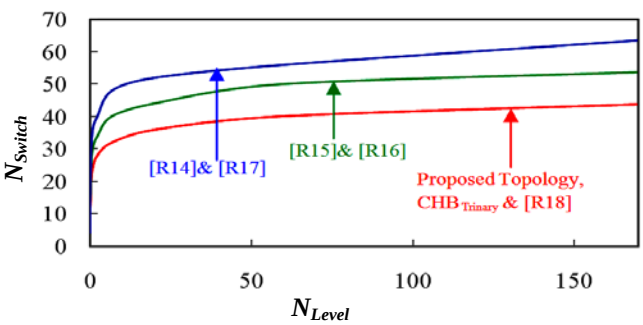


Fig. 13. Comparison of number of switches with other topologies (trinary configuration).

the same number of IGBTs to generate the same output voltage level.

B .Comparison of the Required Gate Driver Circuits

Another important comparison is that between the number of gate driver circuits. These gate driver circuits consist of low power electronics devices for producing a high current drive in high power electronic devices. The use of few gate driver circuits leads to low efficiency. Each bidirectional and unidirectional switch requires only one gate driver circuit. Fig. 14 shows the comparison of the number of gate driver circuits against the number of levels in the proposed and in the recommended topologies.

In this figure, [R15] uses minimal gate driver circuits. However, the proposed topology requires less number of IGBTs than [R15].

C. Comparison of the Blocking Voltage of Switches

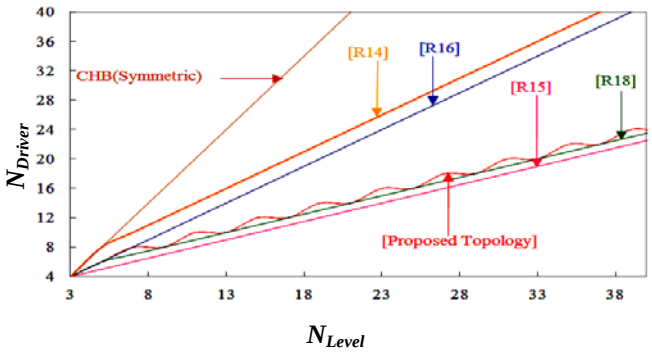


Fig. 14. Comparison of number of driver circuits.

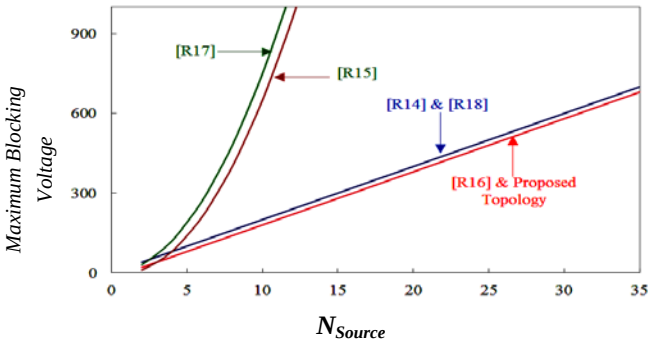


Fig. 15. Comparison of maximum blocking voltages in different topologies.

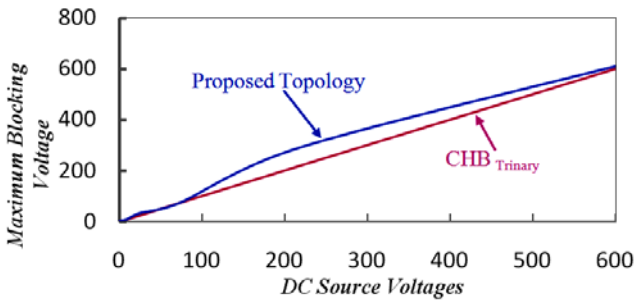


Fig. 16. Comparison of maximum blocking voltages.

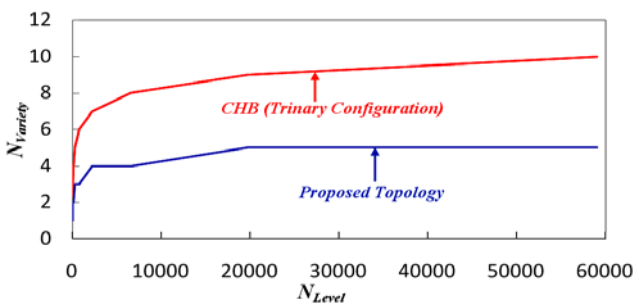


Fig. 17. Comparison of number of levels and number of dc source voltage varieties.

The maximum blocking voltage is another criterion for finding an optimum multilevel inverter topology. The maximum number of voltage levels can be achieved with a constant number of IGBTs. In the proposed topology, each sub-multilevel inverter has four dc sources. Therefore, the maximum blocking voltage at the level generator switch depends on the S_{kj}, (V_{max}, S_{kj}) switch and can be calculated as

$$V_{max},S_{kj} = 2(9^{k-1} \times V_{dc}) \tag{33}$$

Since,

$$k = log_{(2n+1)} N_{Level} \tag{34}$$

With consideration for ***n=4*** and the preceding expressions, the maximum blocked voltage by ***SS-unit*** and ***DS-unit*** switches are

$$V_{max},S_{k1} = \left(\frac{N_{Level}}{9}\right) * V_{dc} \tag{35}$$

$$V_{max},S_{k2} = \left(\frac{N_{Level}}{9}\right) * 2V_{dc} \tag{36}$$

(35) and (36) are considered single and double dc source switches, respectively. The current rating of all the switches is equal to the load current; this is not the case for voltage. In the proposed topology, both V_{dc} and $2V_{dc}$ voltage rating switches are required. The cost of the double voltage rating switch can be determined as

$$\beta = \frac{Switch\ rated\ 2V\ and\ I_o}{Switch\ rated\ V\ and\ I_o} \tag{37}$$

For a $\beta \le 2$, the cost of $2V_{dc}$ switches is less than the V_{dc} switches. For a $\beta>2$, the cost of $2V_{dc}$ is higher than the V_{dc}. The proposed topology and that presented in [16] require less total blocking voltage than other topologies. To reconfirm the above statement, Fig. 15 shows that the proposed topology requires the minimum total blocking voltage against the number of levels. In this comparison, the blocking voltage of the level generator switch of the sub-multilevel inverters are considered.

The maximum blocking voltage of the H-bridge switches are equal to that in the proposed topology and that presented in [14]-[18]. Thus, the maximum blocking voltage of the proposed topology and of the CHB (trinary configuration) is also compared. As shown in Fig. 16, the maximum blocking voltage of the proposed topology and CHB trinary configuration has an equal value at odd number of dc source.

D. Comparison of the Variety of DC Source Voltages

The variety of dc sources is another important parameter that determines the cost of multilevel inverters. Fig. 17 shows the number of levels against the number of varieties of dc sources. The proposed topology and recommended topologies in [14]-[18] require the minimum variety of dc sources—less than that required by the CHB (trinary configuration). The proposed cascaded structure has less IGBTs and has the minimum of blocking voltages compared with other topologies. Based on all the aforementioned comparison, can conclude that with an even number of dc sources, the proposed topology requires few IGBTs, achieves the minimum gate driver, has low blocking voltage and low dc source variety, and achieves the maximum output voltage level.

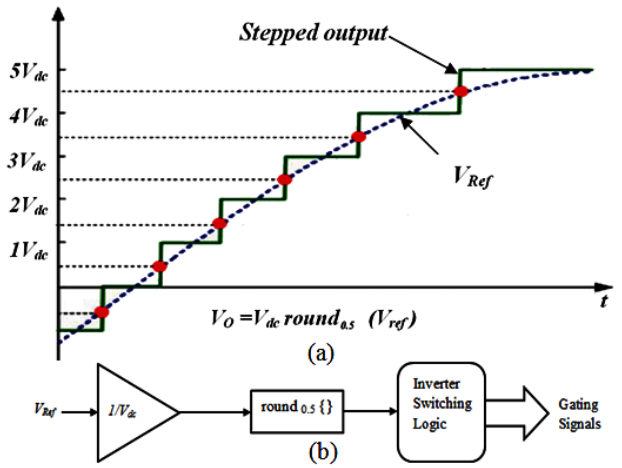


Fig. 18. Nearest level selection. (a) Level synthesis. (b) Control diagram.

Using (31), all the parameters are compared with similar topologies and found that the cost of the proposed topology is lower than the cost of the other typologies.

VI. Simulation And Experimental Results

To analyze the performance of the recommended cascaded structures, the simulation and experimental results for a 41-level topology is presented and the results are analyzed.

For both simulations (which were performed using MATLAB–Simulink) and the hardware test, load values were set at R=100 Ω and L =100 mH, with an output frequency of 50 Hz. Several modulation strategies have been introduced for multilevel inverters including the sinusoidal Pulse Width Modulation (SPWM) [23], [24], space vector PWM [25], selective harmonic elimination [26], hybrid modulation [27], hysteresis modulation [28], and fundamental frequency switching [29]. For the recommended structure, the fundamental switching method is implemented because low switching frequency (nearest level control method, or NLM) is preferable for high power applications [30], as shown in Fig. 18. The nearest level of the constant is compared with the reference signal; and appropriate pulses are generated.

Used herein is the conventional NLM, which generates steps using the basic concept of the rounding-off technique, as shown in Fig. 18(b). This method is suitable for the increased number of output voltage levels. This method is easily performed using the round {} function and the integer closest to x. As an additional convention, given that this method is similar to the half-height method, half-integers are always rounded-off to the nearest integer numbers. The largest possible error is then limited by *Vdc/2* [31]. To analyze the performance of any new multilevel converter, consider the major index is total harmonic distortion (THD), which can calculate the quantity of harmonics presented in the output waveform.

In general, the THD can be calculated as follows:

$$THD = \sqrt{\frac{\sum_{h=odd}^{\infty} V_{oh}}{V_{o1}}} = \sqrt{\frac{V_{o,rms}}{V_{o1}} - 1} \tag{38}$$

In (38), h (odd order of harmonics) =3, 5, 7, … and V_{o1} is the fundamental output voltage of $V_{oh\text{-}n}$ order harmonic; and $V_{o,rms}$-is the *rms* value of the output voltage. The magnitude of V_{o1} and $V_{o,rms}$ can be calculated using the following:

$$V_{o,rms} = \frac{2\sqrt{2}\,V}{\pi} \times \sqrt{\sum_{h=odd}^{\infty} \left(\sum_{j=1}^{N_{Level}} \frac{\cos(h\theta_j)}{h} \right)^2} \tag{39}$$

$$V_{o1} = \frac{2\sqrt{2}\,V}{\pi} \times \sum_{j=1}^{N_{Level}} \cos(\theta_j) \tag{40}$$

where $\boldsymbol{\theta_1}$, $\boldsymbol{\theta_2}$, $\boldsymbol{\ldots\theta_{NLevel}}$ are switching angles and are calculated as

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{Level}}\right) \quad j = 1,2,3....N_{Level} \tag{41}$$

For reducing voltage spikes and for limiting *dv/dt* (voltage stress across the switches), snubber circuits are preferable. In this paper, the required voltage rating of the level generator unit switches is low because separate dc sources are connected with series/parallel switches. The H-bridge unit (polarity changer), however, should withstand the sum of the all the dc source voltages present in the level generator. Thus, in the process of designing the proposed multilevel inverter, high voltage rating of a snubber circuit to be designed. Different snubber circuits are presented in [32]; the basic RC snubber circuit is suitable for the level generator (in low voltage switches) because the RC dissipates much current due to the nature of the resistor, and because a RCD snubber clamp circuit is suitable for the H-bridge side (in high voltage switches). The losses in a RCD snubber clamp circuit are low, but this type of circuit may require many components. Nonetheless, the prototype model described in this paper is developed using a RC snubber circuit.

E. 49-Levels of the Proposed Cascaded Topology

Shown in Figs. 19 and 20 are the proposed cascaded structure of a 49-level inverter circuit diagram and the output results, respectively. As discussed, the maximum output voltage is generated by Algorithm-7, causing this algorithm to be implemented in the hardware experiment. The control fundamental switching technique is implemented in a FPGA Spartan XE3S250E controller. To implement the 49-level proposed cascaded inverter with 6 dc voltage sources, 16 IGBTs (BUP400D) and 12 IGBT drivers (HCPL316j) are used. In the present structure, each source is connected with a series/parallel switch.

Parameters, like magnitudes of the dc source voltages and load values, in the simulation and in the experiment are the same. The dc source magnitudes, *4 V* for *k=1* and *28 V* for *k*=2,

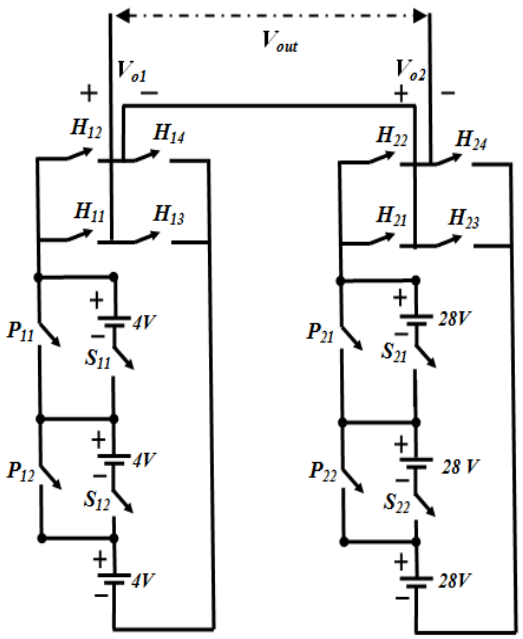
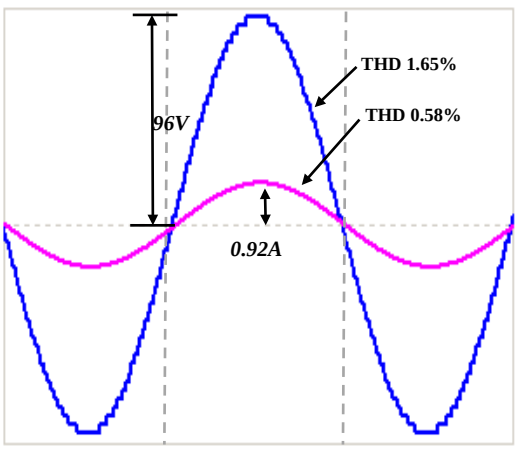
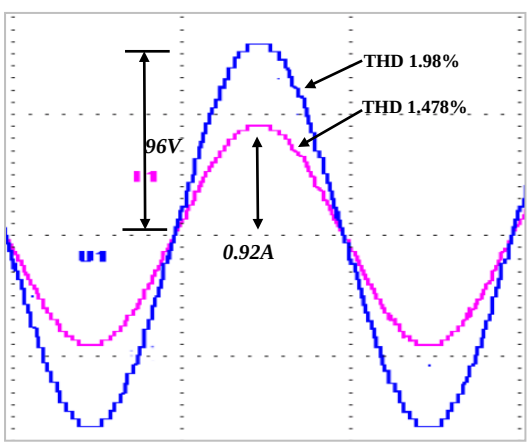


Fig. 19. 49-level inverter based on the proposed topology for k=2 and n=3.



(a)



(b)

Fig. 20. Simulation and experimental results of 49-level sub-multilevel inverter. (a) Simulation output voltage and current waveforms, respectively. (b) Experimental output voltage and current waveforms, respectively.

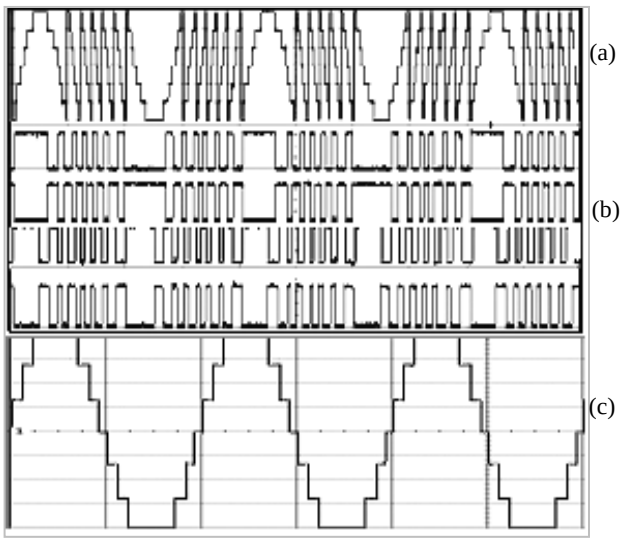


Fig. 21 Experimental blocking voltage of different switches for 49-level sub multilevel inverter. (a) First sub-multilevel inverter h-bridge switches. (b) First sub-multilevel inverter level generator switches. (c) Second sub-multilevel inverter H-bridge switches.

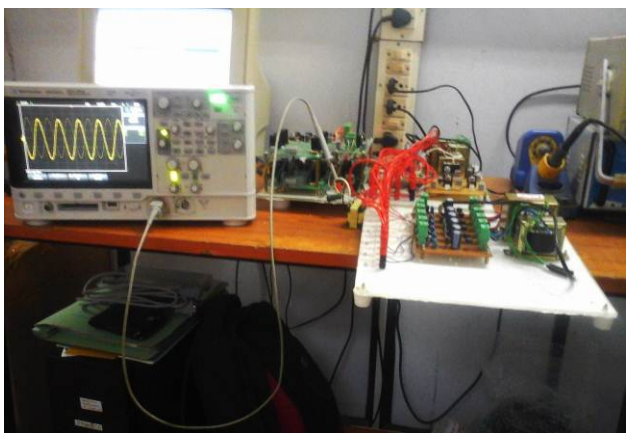


Fig. 22. Prototype hardware.

and these input sources are provided through step-down transformers, along with a rectifier and a voltage regulator unit. The maximum output voltage is 96 V and the load values are *R=100* Ω and *L=100 mH*. Shown in Figs. 20(a) and (b) are the experimental voltage and current waveforms with THDs of 1.98% and 1.478%, respectively, which are based on the load parameters. These results are close to the simulation voltage and current waveforms (as shown in Fig. 19(a)) with THDs of 1.65% and 0.58%, respectively. As the number of levels increases, both voltage and current THDs are reduced using fundamental switching techniques. The high inductive load is used, acting as a filter; the load and current becomes close to a sinusoidal waveform. The blocked voltage of each switch (both V_{dc} and $2V_{dc}$ switches) in the level generator unit and the H-bridge unit switches are presented in Fig. 21; a photograph of the hardware used in the laboratory as prototype inverter model is shown in Fig. 22.

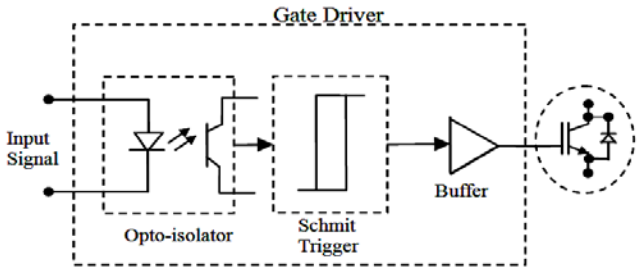


Fig. 23. Gate driver circuit and switching mechanism for switch $(S_j \& P_j)$.

The switching mechanism for the unidirectional switches is shown in Fig. 23.

These circuits consist of an opto-isolator (for isolating the switch from the controller (FPGA)), a Schmitt trigger (used to convert analog signal to digital pulses), and a buffer. Opto-isolators can work with a wide range of input signal pulse widths, but a separate, isolated power supply is required for each switching device. For isolation, either a pulse transformer or opto-isolators can be used. The opto-isolator-based driver is used in this prototype model.

VII. Conclusion

New symmetric cascade multilevel inverter structures are proposed. The maximum number of output voltage is obtained with minimal IGBTs and reduced dc voltage sources. Various new algorithms are provided to generate even and odd stepped waveforms. The proposed topology requires few power electronics components and costs less than other topologies. The best algorithms are selected and optimized for different goals such as the maximum number of output voltage levels for the minimum number of IGBTs, gate driver circuits, blocking voltage, and reduced dc sources. The proposed symmetric cascaded structure inverter is suitable for medium- and high-voltage applications. The cascaded structure is verified by simulation and experimental results. To ensure a dynamic response of the proposed topology, and to serve as future work, we shall conduct a study related to industrial drives or FACTS device applications.

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Jagabar Sathik Mohd. Ali was born in Madukkur, Tamil Nadu, India, in 1979. He received an undergraduate degree in electronics and communication engineering from Madurai Kamaraj University, Madurai, India, in 2002, and a Master's degree in power electronics and drives from Anna University, Chennai, India, in 2004. He is currently working toward a Ph.D. degree from the Faculty of Electrical Engineering, Anna University, India. In 2011, he joined the Department of Electrical and Electronics Engineering, J.J. College of Engineering and Technology, Tiruchirappalli, India. His major areas of interest include analysis and control of power electronic converters and renewable energy systems.

Ramani Kannan was born in Vedaranyam in 1982. He graduated from Bharathiar University, Coimbatore, in 2004, and post-graduated from Anna University, Chennai, in 2006. He obtained a Ph.D. degree in electrical engineering from Anna University in 2012. Since January 2006, he has worked as an associate professor at the Department of EEE, K. S. Rangasamy College of Technology, Tiruchengode. He has 56 published works in international/national conferences and journals. His research interests involve power electronics, inverters, modeling of induction motors, and optimization techniques. He currently guides undergraduate and postgraduate Students and supervises Ph.D. scholars in Anna University. He is a member of the ISTE, IETE, and IEEE and has received the CAYT award from AICTE, New Delhi. He is currently part of many editorial boards and acts as editor-in-chief of international journals and IEEE Conferences.