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A Family of Non-Isolated Photovoltaic Grid Connected Inverters without Leakage Current Issues

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Abstract

Transformerless solar inverters have a higher efficiency than those with an isolation link. However, they suffer from a leakage current issue. This paper proposes a family of single phase six-switch transformerless inverter topologies with an ac bypass circuit to solve the leakage current problem. These circuits embed two unidirectional freewheeling current units into the midpoint of a full bridge inverter, to obtain a freewheeling current path, which separates the solar panel from the grid in the freewheeling state. The freewheeling current path contains significantly fewer devices and poor performance body diodes are not involved, leading to a higher efficiency. Meanwhile, it is not necessary to add a voltage balancing control method when compared with the half bridge inverter. Simulation and experiments are provided to validate the proposed topologies.

Key words: Common-mode voltage, Leakage current, Non-isolated inverter, Photovoltaic

I. INTRODUCTION

In photovoltaic (PV) power systems, transformerless inverters exhibit great advantages in terms of reliability, efficiency, structure, cost, and other aspects. However, these non-isolated inverters suffer from some drawbacks, such as a common-mode voltage or ground leakage current issue between the grid and PV systems [1]. From the safety and electromagnetic interference reduction point of view, most counties have strict rules for the leakage current of grid-connected inverters in the form of national standards. For example, according to the German standard DIN VDE 0126-1-1, for transformerless PV inverters connected to the grid, if the leakage current to ground (peak value) is greater than 300mA, then disconnection is necessary within 0.3s [2]. Therefore, in recent years, the leakage current issue has become one of the hot areas of researches for non-isolated grid-connected PV inverters [3]-[9].

Currently, based on the full bridge structure, an effective way to solve the leakage current problem is to add an auxiliary circuit to force the freewheeling current to change its flowing path. This makes the solar panel separate from the grid in the freewheeling stage. From the above approach, several structures have been proposed. A H5 inverter proposed by SMA Solar Technology AG was introduced in [3]. This structure uses fewer devices and minimizes cost. However, freewheeling diodes have a serious reverse recovery problem. As a result, it is difficult to further enhance the efficiency. Papers [10]-[12] introduce a full bridge inverter with a dc bypass circuit, which exhibits a low current ripple in the ac side and a reduced converter loss. In this case, a voltage balance control is needed due to the midpoint by voltage dividing of the dc link capacitor. However, the influence of this control was not analyzed or solved in these papers. It can be found that the difficulty of control is increased. Papers [13]-[15] present several six-switches (H6) inverter topologies with an ac bypass circuit. With the bipolar modulation scheme, the common-mode (CM) voltage and leakage current have been restrained by sequential control, which results in a unipolar modulation effect. However, the topologies presented in papers [14], [15] have body diodes in the current path, which limits their performance.

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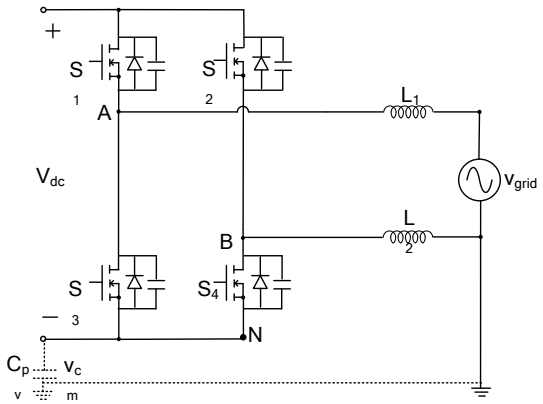


Fig.1. Single phase full-bridge inverter.

In view of the above issues, this paper proposes a family of H6 inverter topologies with an ac bypass circuit, in which two unidirectional freewheeling cells are embedded between the midpoint of the full bridge inverter to obtain a freewheeling path, which separates the solar panel from the grid in the freewheeling stage. In these topologies, there are fewer devices and poor-performance body diodes are not involved in the freewheeling path, which is useful for obtaining a high efficiency. Meanwhile, voltage balance control is not required. Discussions and verifications are given in the following sections.

II. Leakage Current Analysis of the Transformerless Inverter

A traditional single-phase full bridge inverter (H4) is employed here for the leakage current analysis, as shown in Fig. 1, where V_{dc} is the input DC voltage, v_{grid} is the grid voltage, and v_{AN} and v_{BN} are the pulse voltages between the branch midpoint and the DC bus minus terminal N, respectively. C_{pv} is the PV module stray capacitance. The CM voltage v_{cm} and current i_{cm} of the inverter could be given by the following equation:

$$v_{cm} = 0.5(v_{AN} + v_{BN}) \tag{1}$$

$$i_{cm} = C_{PV}\frac{dv_{cm}}{dt} \tag{2}$$

Where the CM current is the ground leakage current, and is proportional to the CM voltage change rate. Hence, the pulse voltage is the excitation source of the leakage current.

In order to minimize the leakage current, the CM voltage change rate should be decreased as low as possible. If the CM voltage can be kept constant, the leakage current is eliminated. For the full bridge inverter in Fig.1, two modulation strategies, unipolar and bipolar, are commonly used in the industry.

With the unipolar modulation scheme, taking the positive grid half-cycle as an example, when S_1 and S_4 are on, the CM voltage is given by:

$$v_{cm}=0.5(v_{dc}+0)=0.5v_{dc} \tag{3}$$

When S_1 is turned off, and S_3 and S_4 are on, the CM voltage is:

$$v_{cm}=0.5(0+0)=0 \tag{4}$$

If the bipolar modulation scheme is used, in the positive grid half-cycle, when S_1 are S_4 are on, the CM voltage is:

$$v_{cm} = 0.5(v_{AN} + v_{BN})=0.5(v_{dc}+0)=0.5v_{dc} \tag{5}$$

When S_1 and S_4 are turned off, and S_2 and S_3 are on, the CM voltage is:

$$v_{cm} = 0.5(0+v_{dc}) =0.5v_{dc} \tag{6}$$

From (3)-(6), it is found that for the unipolar modulation scheme, the CM voltage changes between $0.5v_{dc}$ and 0 at the switching frequency, producing a large leakage current. For the bipolar modulation scheme, the CM voltage is almost constant. Thus, the leakage current problem is avoided. However, from the switching loss, current ripple and filter size view point, it is better to use the unipolar modulation scheme. Therefore, in order to combine the advantages of the two schemes, the circuit structure should be changed. In this paper, a freewheeling path is added between the leg midpoint A and B for achieving the above objectives.

III. Circuit Configuration and Working Principle Analysis of the Proposed Topologies

A. Circuit Configuration

A family of non-isolated PV grid-connected inverters without a leakage current issue is presented, as shown in Fig. 2. This family contains four topologies with the freewheeling branches located in different positions. In Fig. 2, S_1-S_6 are switches, D_1-D_2 are freewheel diodes, L_1 and L_2 are grid filter inductors.

B. Operation Principles

As an example for a detailed analysis, one of the proposed H6 inverter topologies and its sequential logic diagram are shown in Fig. 3, where G_1- G_6 are the drive signals of the switches S_1-S_6. G_1-G_4 are obtained by sinusoidal pulse width modulation (SPWM) in the positive/negative half-cycle. S_5 and S_6 work according to the grid frequency.

Fig. 4 gives the simulation waveforms of the proposed topology under a full load, and its operation modes are shown in Fig. 5. The working principles of the proposed non-isolated PV grid-connected inverters are illustrated in Fig. 3 to Fig. 5.

Mode I: In the positive half-cycle, as shown in Fig. 5(a), S_5 is always on; S_1 and S_4 are active; and S_2, S_3 and S_6 are always off. When S_1 and S_4 are on, the grid is charged with input voltage and current flows through S_1, L_1, L_2 and S_4. In this mode, the output voltage is given by:

$$v_{AB}=+V_{dc} \tag{7}$$

Mode II: S_1 and S_4 are off, as shown in Fig.5 (b). To maintain an inductor current, S_5, L_1, L_2 and D_1 provide a freewheeling path. The output voltage is:

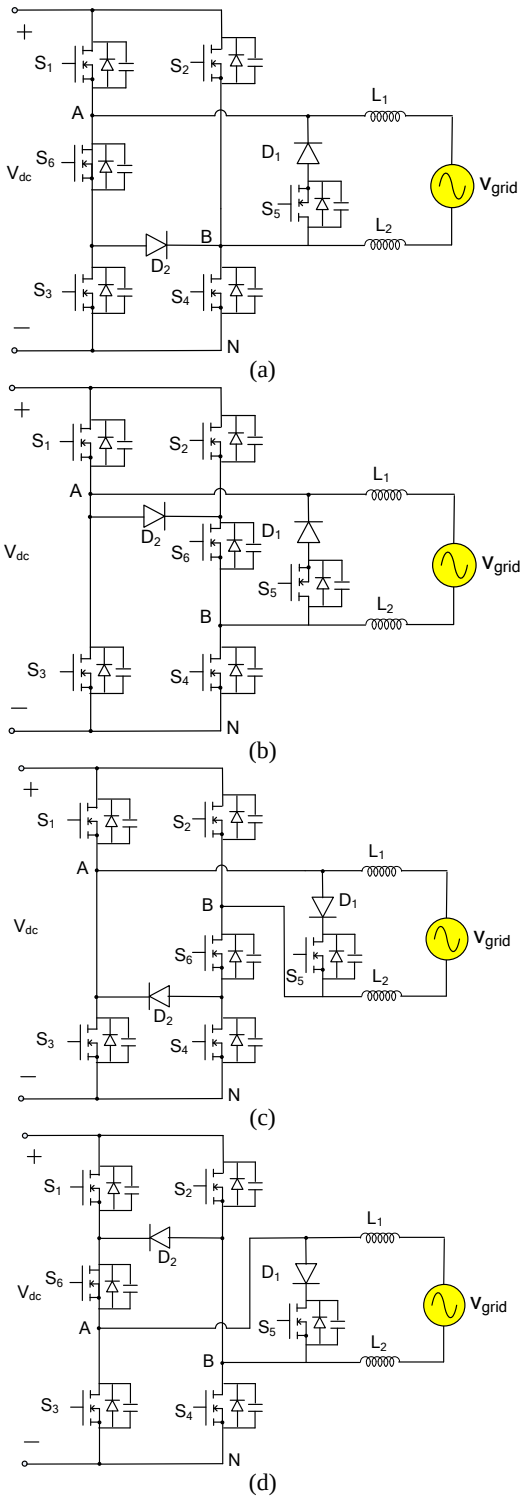


Fig. 2. A family of non-isolated PV grid-connected inverters without leakage current issue.

$$v_{AB}=0 \tag{8}$$

Mode III: In the negative half-cycle, as shown in Fig.5 (c), S_6 is always on; S_2 and S_3 are active; and S_1, S_4 and S_5 are always off. When S_2 and S_3 are on, the grid is charged with input voltage and current flows through S_2, L_1, L_2 and S_6. In this mode, the output voltage is given by:

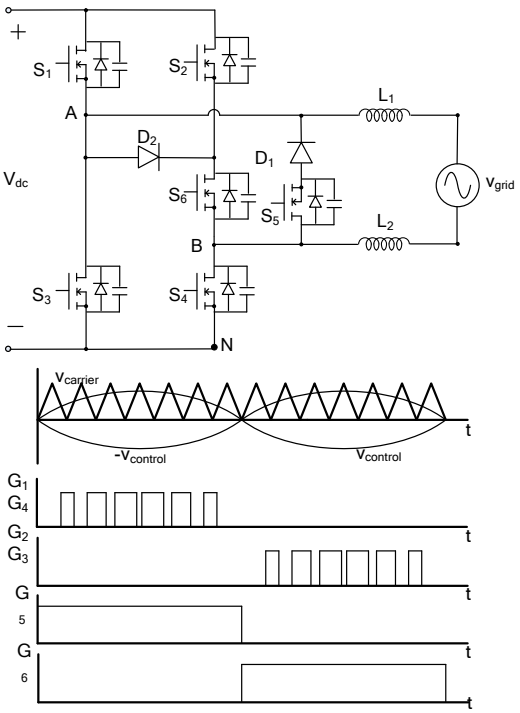


Fig. 3. The proposed H6 inverter and logic diagram.

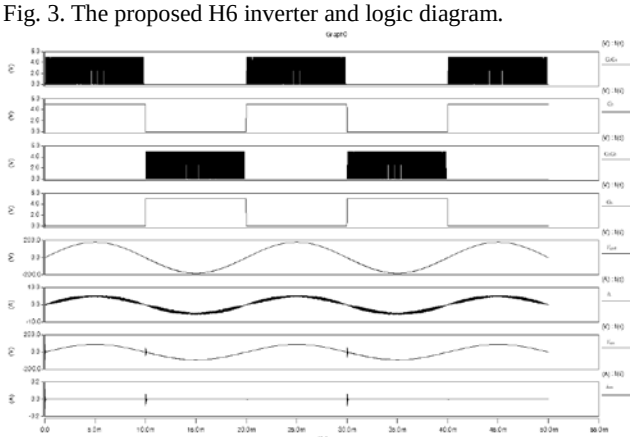


Fig. 4. Simulation of the proposed H6 inverter.

$$v_{AB}=-V_{dc} \tag{9}$$

Mode IV: S_2 and S_3 are off, as shown in Fig.5 (d). To maintain an inductor current, S_6, L_1, L_2 and D_2 provide a freewheeling path. The output voltage is:

$$v_{AB}=0 \tag{10}$$

As can be found from the above analysis, this modulation scheme behaves similar to the unipolar modulation scheme in terms of the output voltage of the inverter. There is a 1, 0 modulation in the positive half-cycle, and a -1, 0 modulation in the negative half-cycle, which is also verified by the simulation waveforms in Fig. 4.

For the CM voltage, in the positive half-cycle, when S_1 and S_4 are on, V_{dc} is the output voltage from clamped point A to the DC ground and the voltage from clamped point B to the DC ground is 0 (neglect the switch voltage drop). Thus, the CM voltage during this period is:

$$v_{cm}=0.5(v_{dc}+0)=0.5v_{dc} \tag{11}$$

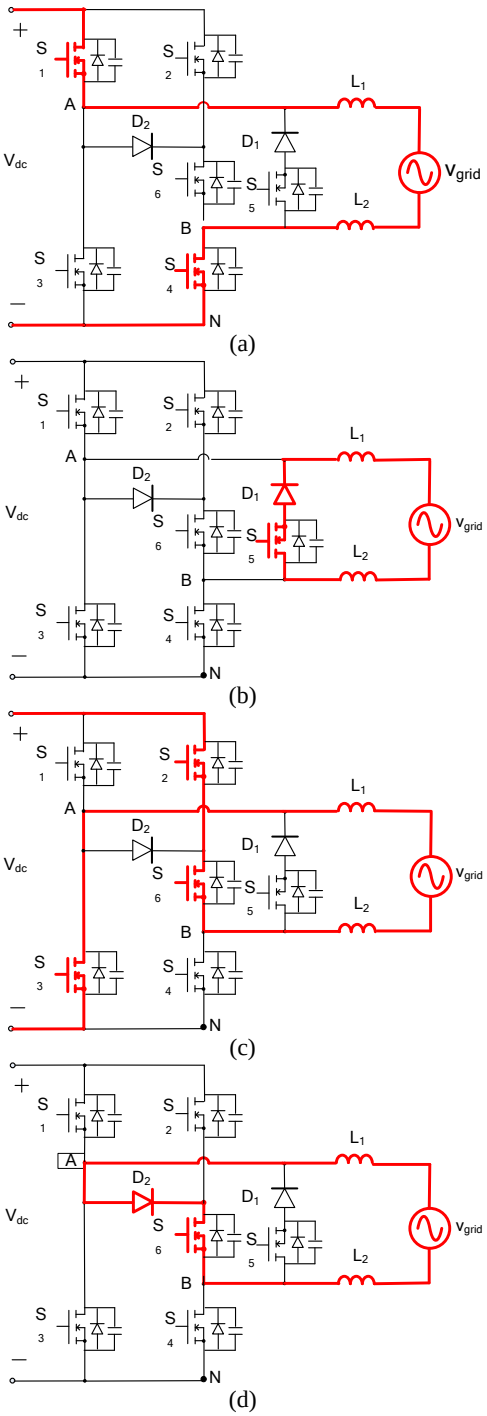


Fig. 5. Operation modes of the proposed H6 inverter.

When S_1 and S_4 are off, D_1 and S_5 are in the freewheeling state. At this time, S_1 and S_3 are in the off state and the voltage balance can be realized. The voltage from clamped point A to the dc ground is one half of the output voltage. When S_2 and S_4 are in the off state, the voltage balance can also be realized and the voltage from clamped point B to the dc ground is one half of the output voltage. During this period, the CM voltage is:

$$v_{cm}=0.5(0.5v_{dc}+0.5v_{dc})=0.5v_{dc} \quad (12)$$

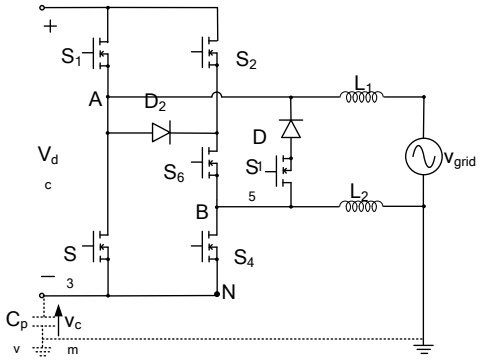


Fig. 6. CM voltage analysis of the proposed H6 inverter.

If the input voltage V_{dc} is unchanged, the CM voltage can be kept constant. The analysis of the negative half-cycle is similar to that of the positive half-cycle, and is not discussed here.

Consequently, the CM voltage produced by the leg midpoint output voltage to the DC bus minus terminal does not vary and is kept constant at half of the input voltage. As shown in Fig.6, the CM voltage formed by the dc bus minus terminal to the ac ground is basically a dc offset superimposed with low frequency components. This causes a small CM current to flow through the equivalent CM capacitor C_{pv} (simulated by a 1nF capacitor), which is far below the limits of 30mA.

The advantages of the proposed topology can be concluded as follows:

1) Except for mode III, for the above states, the current only flows through one or two switching devices, which is beneficial for dynamic loss reduction.

2) The current freewheeling path contains special fast recovery diodes, unlike the body diodes that appear in the traditional full bridge inverter freewheeling path, which solves the recovery problems. Paper [16] illustrates that the performance of diodes has a great influence on the switching losses, and that its forward and reverse recovery processes are the main causes of switching loss. When compared with papers [14], [15], the proposed topology does not have the above problems and it is beneficial for switching loss reduction.

3) It can be observed that the proposed topology has no voltage balance problem.

IV. Analysis of Critical Issues

With a consideration of the analysis shown in previously published papers [16], [17], some additionally selected analysis are added here, such as the control strategy, inductor design and phase-locked-loop (PLL) technique.

A. Grid-Connected Control Strategy

For the proposed H6 topology, the grid current is regulated

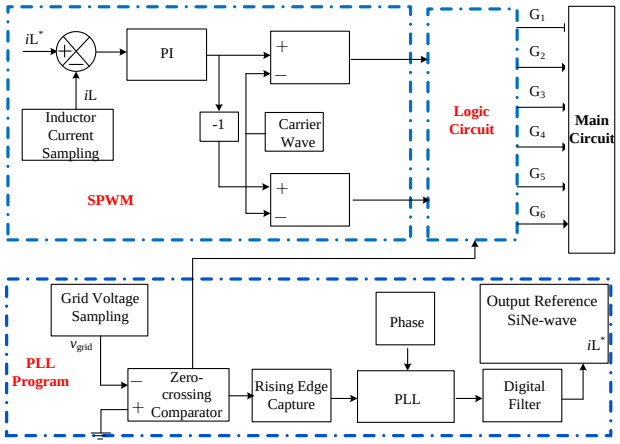


Fig. 7. Control block of the proposed H6 inverter.

according to the grid voltage, and only the active power control is involved here.

The hysteresis current control and the sinusoidal pulse width modulation (SPWM) control are the two main schemes for grid current control. The hysteresis current control is simple and has a good dynamic performance. However, it also has a wide switching frequency range, and it is difficult to design the output filter. Meanwhile the SPWM control has a fixed switching frequency and it is easy to design the output filter. In addition, it only has the harmonics of the carrier frequency, which leads to a smaller harmonics content. Hence, the SPWM is employed in this paper.

Fig. 7 shows the control blocks of the proposed grid-connected inverter. They are composed of a phase-locked loop by software, SPWM parts, and a logic circuit. The PLL circuit generates the AC grid synchronous square wave reference signal. Then, the output of the reference sine wave is obtained by reading the reference sine table with a DSP program. The current loop control scheme is used by the control circuit, and the SPWM signals are obtained by comparing the sine wave with the triangular wave. The logic circuit used to obtain the switch signals G_1 -G_6.

B. Inductor Design

The selection of the grid-connected output inductor needs to be considered with respect to many aspects such as inductor size and current ripple. A bigger inductor leads to a smaller current ripple. However, it also results in a bigger inductor loss and a bigger size. Therefore, an inductor with a current ripple that is less than 10~20% of the rated output current is always chosen.

The inverter switching frequency is higher than that of the grid fundamental frequency. Thus, in a high frequency switching cycle, the grid voltage is almost constant, and the inductor current variation is given by:

$$\Delta i_{\mathrm{L}} = (V_{\mathrm{dc}} - v_{\mathrm{grid}}(N)) \cdot D \cdot T_{\mathrm{s}} / (L_1 + L_2) \tag{13}$$

Where, for a high frequency switching period, D is the duty cycle, and $v_{\mathrm{grid}}(\mathrm{N})$ is the grid voltage.

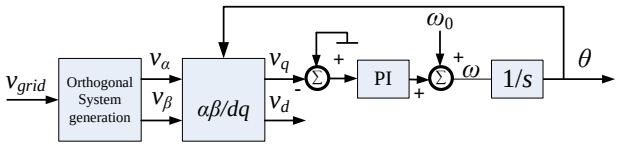


Fig. 8. General structure of a single phase PLL.

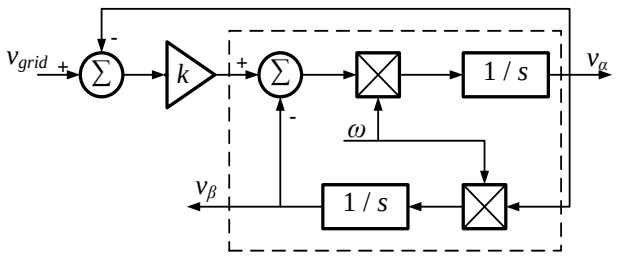


Fig. 9. Method of SOGI constructing orthogonal component.

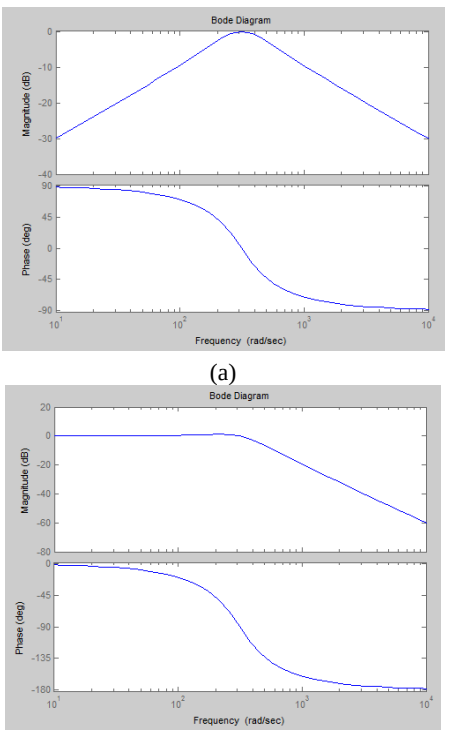


Fig. 10. Bode plots of H_α and H_β. (a) H_α. (b) H_β.

In a high frequency switching period, $v_{\mathrm{grid}}(\mathrm{N})=DV_{\mathrm{dc}}$ is satisfied. By taking this into (12) the following can be obtained:

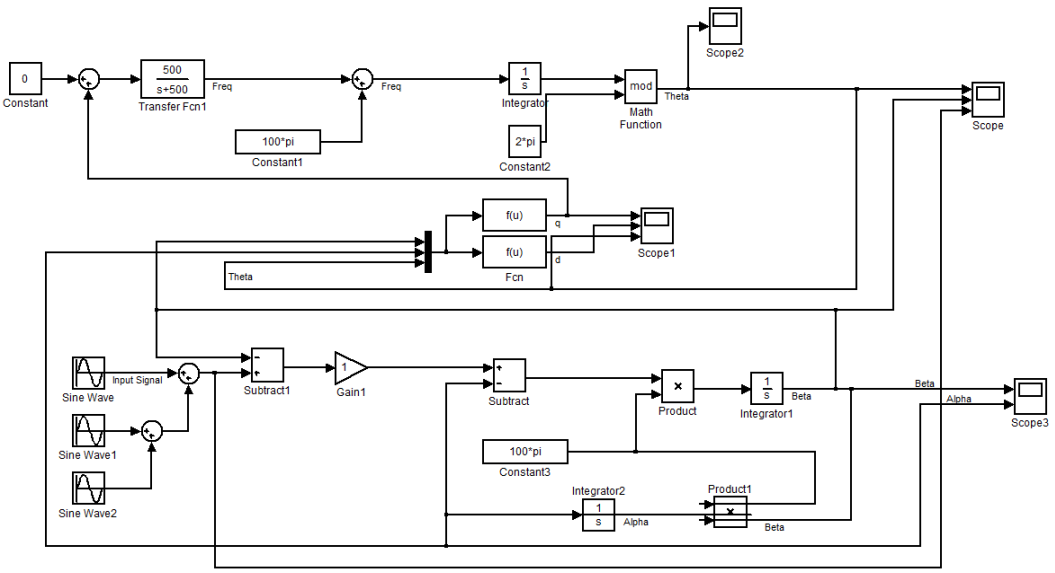
$$\Delta i_{\mathrm{L}} = \frac{(V_{\mathrm{dc}} - V_{\mathrm{grid}}(N)) \cdot V_{\mathrm{grid}}(N) \cdot T_{\mathrm{s}}}{(L_1 + L_2) \cdot V_{\mathrm{dc}}} \tag{14}$$

When $v_{\mathrm{grid}}(\mathrm{N})=V_{\mathrm{dc}}/2$, Δi_{L} reaches its maximum value, that is:

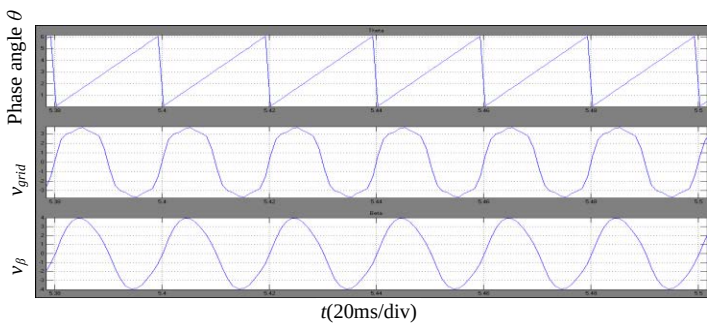
$$\Delta i_{\mathrm{Lmax}} = \frac{V_{\mathrm{dc}} \cdot T_{\mathrm{s}}}{4(L_1 + L_2)} \le (10-20)\% I_{\mathrm{grid}} \tag{15}$$

The output filter inductors must be met by:

$$L_1 + L_2 \ge \frac{0.25 V_{\mathrm{dc}} \cdot T_{\mathrm{s}}}{(10-20)\% I_{\mathrm{grid}}} \tag{16}$$



(a)



(b)

Fig. 11. PLL Simulation based on Matlab. (a) PLL schematic. (b) Simulation result.

C. Phase-Locked Loop Design

An accurate and fast detection of the frequency, and the phase angle of the grid voltage are essential to assure the correct generation of reference signals and to cope with the utility codes, especially for those operated under common utility distortions such as harmonics, voltage sags, frequency variations and phase jumps.

In this paper, a single phase PLL based on the synchronization reference frame is adopted as shown in Fig. 8 [18]. An orthogonal voltage is generated from the second order generalized integrator (SOGI) method as shown in Fig. 9. This generated orthogonal system is filtered without a delay by the same structure due to its resonance at the fundamental frequency. In addition, the PLL here is not affected by line frequency variations.

The closed loop transfer functions of the orthogonal voltage to the grid voltage are given by equations (17) and (18) and are shown in Fig. 10.

$$H_\alpha(s)=\frac{V_\alpha(s)}{V_g(s)}=\frac{k\omega_0 s}{s^2+k\omega_0 s+\omega_0^2} \tag{17}$$

$$H_\beta(s)=\frac{V_\beta(s)}{V_g(s)}=\frac{k\omega_0^2}{s^2+k\omega_0 s+\omega_0^2} \tag{18}$$

Fig. 11(a) gives the complete PLL schematic based on the SOGI. The grid voltage is simulated with an additional harmonic input:

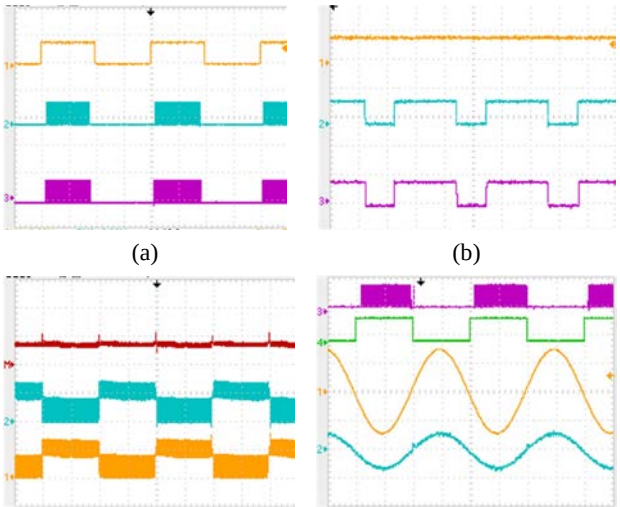
$$V_g=4\sin(\omega_0 t)+0.6\sin(3\omega_0 t)+0.3\sin(5\omega_0 t) \tag{19}$$

Fig. 11(b) further illustrates that the phase angle of the PLL output follows the fundamental component precisely. In addition, the generated V_β with the SOGI method is a pure sinusoidal signal.

V. Experiment Results

In order to verify the proposed topologies, a 400VA prototype was built based on Fig. 3 and experiments were carried out. The experimental parameters of the designed circuit are: input voltage V_{dc}=350VDC, output voltage v_{grid}=220VAC, output frequency f_{ac}=50Hz; input capacitor C_{in}=2000μF, output inductors L_1=L_2=880μH, and output capacitor C_f=4.7μF. A Chroma AC source is used to simulate the grid.

As can be seen from Fig. 12, with the unipolar modulation scheme, the voltages (v_{AN}, v_{BN}) between the leg midpoint and the DC bus minus terminal are three-level voltages and they



(a) (b) (c) (d)

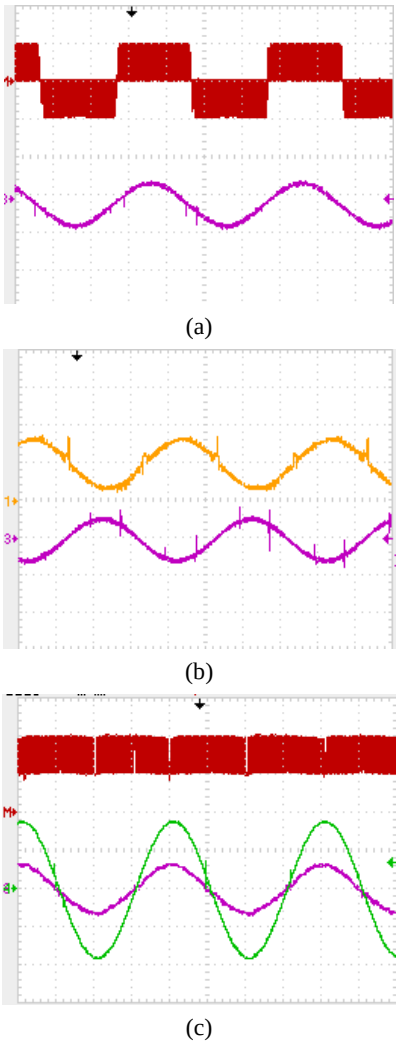
Fig. 12. Output voltage and current waveforms. (a) Drive signals of S_1(CH1:20V/div), S_4(CH2:20V/div) and S_5(CH3:20V/div), respectively (t:10ms/div). (b) Drive signals of S_1(CH1:20V/div), S_4(CH2:20V/div) and S_5(CH3:20V/div), respectively (t:25us/div). (c) Voltages of the leg midpoint and the dc bus minus terminal (CH1 for v_{AN}: 200V/div, CH2 for v_{BN}: 200V/div) and the 2xCM voltage(CHM:400V/div) (t:10ms/div). (d) Drive signals of S_4(CH3: 20V/div), S_1(CH4: 20V/div) and grid voltage(CH1: 200V/div), current (CH2: 5A/div), respectively (t:5ms/div).

exhibit unipolar modulation characteristics. Based on the sum function in the scope (CH1+ CH2), the high-frequency pulses are offset each other after they are superimposed, which makes the CM voltage constant. Therefore, a small leakage current is achieved.

In Fig. 12(c), CM voltage spikes appear when the grid current cross zero, which is in accordance with the simulation, results shown in Fig. 4 of this paper and the ground current in Fig. 6 of reference [19]. The CM voltage is slightly changed, because the leg midpoint voltage cannot be compulsively clamped to half of the input voltage once the current is in the discontinuous mode.

Fig. 13(a) shows the differential-mode (DM) voltage of the proposed H6 topology. It is a three-level waveform and it exhibits a unipolar modulation feature. Fig. 13(b) illustrates the ground potential formed between the DC bus minus and the grid minus of the proposed H6 topology, which is the voltage across the equivalent CM capacitor. It is a low frequency sinusoidal signal. Therefore, the leakage current is well small. For comparison, Fig. 13(c) provides the 2xCM voltage of the H4 topology with unipolar modulation. It can be seen that a large high frequency CM noise occurs. As a result, the leakage current is larger than that of the H6 inverter.

In addition, a high efficiency is achieved with the selected H6 topology. The maximum efficiency is about 98.0% as can be seen from Fig. 14.



(a) (b) (c)

Fig.13. DM and CM voltage of inverters. (a) DM voltage of the proposed H6 topology, (CHM: 400V/div), grid current (CH3: 5A/div) (t:5ms/div). (b) The ground potential of the proposed H6 topology v_{EN} voltage (CH1: 200V/div), grid current (CH3: 5A/div) (t:5ms/div). (c) The 2xCM voltage of the H4 topology with unipolar modulation, where upper switches both operate with line frequency (CHM: 200V/div), grid voltage (CH1: 200V/div), current (CH2:5A/div), respectively (t: 5ms/div).

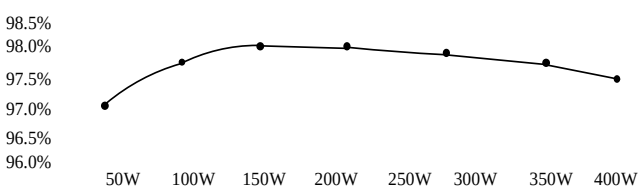


Fig. 14. Efficiency curve.

VI. CONCLUSIONS

A family of H6 inverter topologies with a bypass circuit is proposed based on the full bridge structure. The proposed topology has unipolar PWM output waveforms and eliminates the high frequency pulsates of the CM voltage. Hence, the CM voltage only varies at a low frequency (grid

frequency), leading to a very low level leakage current, which can be neglected.

When compared with previous studies on methods for minimizing leakage current, the proposed structure does not have body diodes in the current path. In addition, voltage dividing capacitors and voltage balance control are not necessary. The above advantages are beneficial for improving both the reliability and the conversion efficiency.

Simulation and experimental results verify the practicality of the proposed topologies and good performance has been reached. The proposed circuit minimizes the leakage current and has high-quality output voltage waveforms for the grid. In addition, a high conversion efficiency is obtained.

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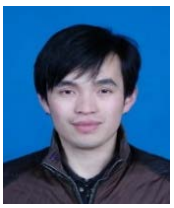

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