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A Dual Buck Three-Level PV Grid-Connected Inverter

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Abstract

The use of a PV grid-connected inverter with non-isolated topology and without a transformer is good for improving conversion efficiency; however, this inverter has become increasingly complicated for eliminating leakage current. To simplify the complicated architecture of traditional three-level dual buck inverters, a new dual Buck three-level PV grid-connected inverter topology is proposed. In the proposed topology, the voltage on the grounding stray capacitor is clamped by large input capacitors and is equal to half of the bus voltage; thus, leakage current can be eliminated. Unlike in the traditional topology, the current in the proposed topology passes through few elements and does not flow through the body diodes of MOSFET switches, resulting in increased efficiency. Additionally, a multi-loop control method that includes voltage-balancing control is proposed and analyzed. Both simulation and experimental results are demonstrated to verify the proposed structure and control method.

Key words: Grid-connected inverter, Leakage current, Non-isolated topology, Photovoltaic

I. INTRODUCTION

Photovoltaic grid-connected inverter systems usually have a line frequency transformer, the reasons for which are as follows. 1) Voltage requirement can be easily matched. Most existing inverter topologies are of the buck type and cannot work under the condition where photovoltaic voltage is lower than the DC bus voltage; the transformer is required to boost voltage level. 2) The transformer is used to achieve electrical isolation, to improve reliability, and to meet safety requirements. However, the presence of a transformer has an adverse impact on system efficiency, which is a key aspect of photovoltaic grid-connected inverters. Line frequency transformers are normally bulky, cumbersome, and energy-consuming; and high frequency transformer isolation schemes make systems more complicated than they already are. Hence, non-isolated structures have been increasingly employed in photovoltaic grid-connected systems. However, without electrical isolation, this topology suffers from several new issues such as leakage current problems, which degrade system safety.

Grounding parasitic capacitors are relatively large due to the large area of photovoltaic arrays [1]. In the presence of electrical isolation, the parasitic capacitor is separated from the line side and has an insignificant impact. Once the transformer is removed, the parasitic capacitor is directly connected to the line side, and a closed loop is formed in the inverter circuit system, from the parasitic capacitor to the grid. The voltage on the parasitic capacitor can be regarded as a common-mode output voltage. Due to the high amplitude of common-mode voltage (at least half of input high voltage for a classic full bridge circuit), which varies with switching frequency, a large leakage current (also called common-mode current) is generated in the parasitic capacitor, endangering personal safety and becoming a crucial issue of non-isolated photovoltaic grid-connected inverters.

Nowadays, single phase low power (below 5 kW) photovoltaic grid-connected devices are mainly employed in residential applications. Thus, research on leakage problems is mainly focused on single phase power systems. As expressed in [2], if the unipolar-modulating method is employed, a

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full-bridge inverter system would have a common-mode voltage that varies with switching frequency; whereas, when the bipolar-modulating method is used, the common-mode voltage is constant and is equal to half of the bus voltage. In half-bridge inverters, the voltage of grounding parasitic capacitance is clamped at half of the bus voltage by large capacitors in a capacitive voltage divider at the input and is almost stable. Hence, in terms of removing leakage current, a half-bridge inverter, or a full-bridge inverter operating under a bipolar-modulating model, would suffice. For increasing efficiency, reducing voltage stress of devices, and minimizing filters, however, the differential mode output voltage waveform at the bridge middle point must usually follow a unipolar modulation. Thus, improvement of the bridge structure for a full-bridge inverter is necessary; and a few new topologies have been proposed. The new techniques used in [3]-[11] can be summarized as follows. By adding active devices or a circuit as auxiliary switches to modify the structure in a full-bridge inverter where the main switches still operate under bipolar modulating condition, the solar panel in an inverter system can be separated from the grid. This is achieved by the change of current path via the action of auxiliary switches. The output voltage at the bridge middle point is a three-level voltage. By introducing a capacitive voltage divider to the modulating circuit structure in a full-bridge inverter, the common-mode output voltage is only half of the bus voltage. A half-bridge inverter with three voltage levels was proposed in [2] and [12]. That architecture maintained a constant voltage on the grounding parasitic capacitor in a half-bridge inverter, while multilevel voltage technology was used to reduce voltage stress and to improve the output of the bridge middle point.

Leakage current can be effectively eliminated in all these proposed architectures. However, hardware cost in those architectures is somewhat increased. Although the H5 structure [3] has the minimum number of devices, the current flows through too many devices, especially through the body diode of switches at free-wheeling stage, resulting in severe reverse-recovery problems. Furthermore, independent control with a high-frequency switch mode is required for the additional device. These requirements lead to increased complexity of the system and have a negative effect on system efficiency and reliability. Other topologies have similar issues. Large capacitors in a capacitive voltage divider at the input were employed in the half-bridge topologies in [5], [8], [11], and [13]; however, the control method for voltage balancing was not stated therein. Therefore, further study on non-isolated photovoltaic grid-connected inverters without leakage current is required.

All the aforementioned studies in existing literature are based on bridge circuits. The dual Buck inverter (DBI) is a new inverter structure which has appeared in recent years [14]-[19]. Due to the combination of two bucks and a unidirectional direct converter (parallel connected at the output side and similar to the half-bridge inverter at the input side), as in unidirectional direct converters, the DBI has no direct conducting path on the bridge circuit and has no involvement in the operation of the body diode. Although the DBI is similar to the half-bridge inverter in that it requires high-input voltage and has a bipolar output voltage at the bridge middle point, the DBI remains to be a good candidate as a highly reliable and efficient inverter. Hence, researchers have proposed some improved multilevel dual Buck structures for further study. In the present paper, a new dual buck three-level grid-connected inverter is proposed and a comprehensive control strategy that includes maximum power point tracking (MPPT) and voltage balancing is presented. Both simulation and experimental results are given to verify this new inverter architecture and to compare it with the other aforementioned topologies.

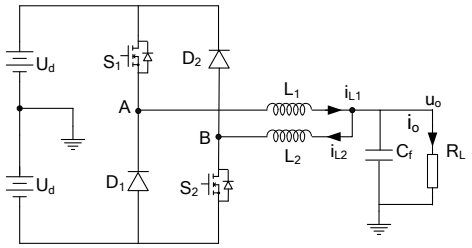

Fig. 1. Dual buck half-bridge inverter.

II. Proposed Dual Buck Three-Level PV Grid-Connected Inverter without Leakage Current

A. Topology Analysis

Fig. 1 shows the DBI circuit topology, which adopts half-load cycle-period operation modes (i.e. during the positive half load cycle period of the output current, switch S_1, freewheeling diode D_1, filter inductor L_1, and filter capacitor C_f form buck circuit 1; during the negative half load cycle period of the output current, switch S_2, freewheeling diode D_2, filter inductor L_2, and filter capacitor C_f operate as buck circuit 2, while buck circuit 1 is not operational). As shown in Fig. 1, u_o is output voltage; i_L is inductor current, which is i_{L1} for the current of inductor L_1 in the positive half load cycle period and i_{L2} for the current of inductor L_2 in the negative half load cycle period; u_A is the bridge-arm output voltage of buck circuit 1 at node A; and u_B is the bridge-arm output voltage of buck circuit 2 at node B.

The operation waveforms of the DBI are shown in Fig. 2. The current cannot possibly flow through the bridge arm, and the body-diodes of switches S_1 and S_2 are not involved in the operation. However, the power switch of the DBI suffers from high-voltage stress. We assume that U_d is the input dc-bus voltage; thus, the voltage across power devices is $2U_d$. The output voltage waveform is bipolar and contains many harmonics.

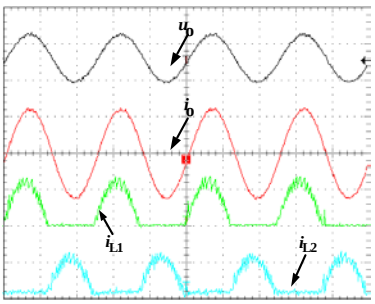

Fig. 2. Operation waveforms of the DBI.

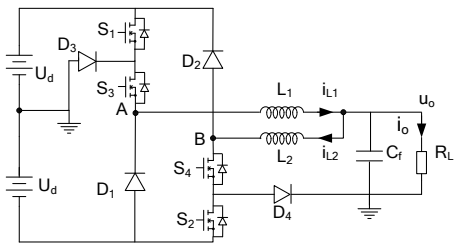

Fig. 3. Topology I of the dual buck three-level inverter.

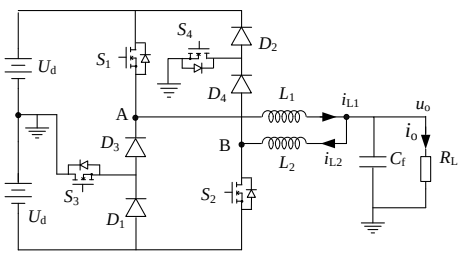

Fig. 4. Topology II of the dual buck three-level inverter

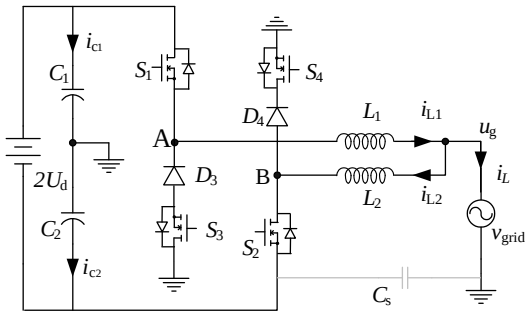

Fig. 5. Three-level dual Buck PV grid-connected inverter

Stated in [16] is the dual buck three-level inverter topology illustrated in Fig. 3. In this structure, switches S_1 and S_2 of the DBI are replaced by the combined switch circuits, S_1&S_3&D_3 and S_4&S_2&D_4, respectively. Shown in Fig. 4 is another dual buck three-level topology presented in [17], wherein the diodes D_1 and D_2 of the DBI are replaced by the combined switch circuits, D_1&D_3&S_3 and D_4&D_2&S_4, respectively. The half load-cycle operation mode of the DBI is retained in the proposed architecture in that, buck circuit 1 works with inductor current i_L in the positive half load cycle period and buck circuit 2 works under negative inductor current i_L in the half load cycle period. The operation modes of three-level topology I and three-level topology II are detailed in Tables I and II, respectively. Both topologies implement a three-level output with the same number of devices used.

For grid-connected applications, the dual buck three-level

TABLE I
OPERATION MODES OF DUAL BUCK THREE-LEVEL INVERTER TOPOLOGY I

Operation Modes		Modes	S_1	S_3	S_2	S_4	D_1	D_3	D_2	D_4	i_L	Bridge output	Output level
$i_L = i_{L1} > 0$ Buck 1	$u_o > 0$	I	**on**	**on**	off	off	off	off	off	off	$i_{L1}\uparrow$	$u_A = +U_d$	+1
		II	off	**on**	off	off	off	**on**	off	off	$i_{L1}\downarrow$	$u_A = +0$	+0
	$u_o < 0$	III	off	**on**	off	off	off	**on**	off	off	$i_{L1}\uparrow$	$u_A = -0$	−0
		IV	off	off	off	off	**on**	off	off	off	$i_{L1}\downarrow$	$u_A = -U_d$	−1
$i_L = -i_{L2} < 0$ Buck 2	$u_o < 0$	V	off	off	**on**	**on**	off	off	off	off	$i_{L2}\uparrow$	$u_B = -U_d$	−1
		VI	off	off	off	**on**	off	off	off	**on**	$i_{L2}\downarrow$	$u_B = -0$	−0
	$u_o > 0$	VII	off	off	off	**on**	off	off	off	**on**	$i_{L2}\uparrow$	$u_B = +0$	+0
		VIII	off	off	off	off	off	off	**on**	off	$i_{L2}\downarrow$	$u_B = +U_d$	+1

TABLE II
OPERATION MODES OF DUAL BUCK THREE-LEVEL INVERTER TOPOLOGY II

Operation Modes		Modes	S_1	S_3	S_2	S_4	D_1	D_3	D_2	D_4	i_L	Bridge output	Output level
$i_L = i_{L1} > 0$ Buck 1	$u_o > 0$	I	**on**	off	off	off	off	off	off	off	$i_{L1}\uparrow$	$u_A = +U_d$	+1
		II	off	**on**	off	off	off	**on**	off	off	$i_{L1}\downarrow$	$u_A = +0$	+0
	$u_o < 0$	III	off	**on**	off	off	off	**on**	off	off	$i_{L1}\uparrow$	$u_A = -0$	−0
		IV	off	off	off	off	**on**	**on**	off	off	$i_{L1}\downarrow$	$u_A = -U_d$	−1
$i_L = -i_{L2} < 0$ Buck 2	$u_o < 0$	V	off	off	**on**	off	off	off	off	off	$i_{L2}\uparrow$	$u_B = -U_d$	−1
		VI	off	off	off	**on**	off	off	off	**on**	$i_{L2}\downarrow$	$u_B = -0$	−0
	$u_o > 0$	VII	off	off	off	**on**	off	off	off	**on**	$i_{L2}\uparrow$	$u_B = +0$	+0
		VIII	off	off	off	off	off	off	**on**	**on**	$i_{L2}\downarrow$	$u_B = +U_d$	+1

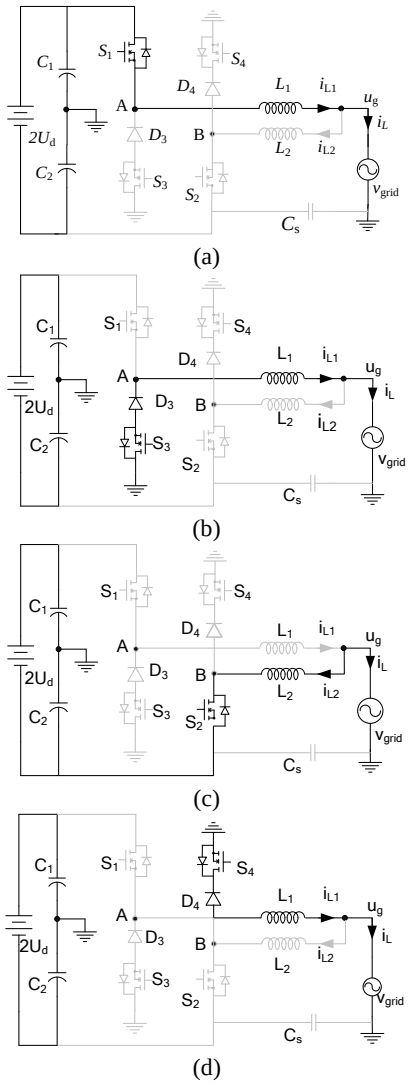

Fig. 6. Operation modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

inverter topology always has i_L=i_{L1}>0, u_o>0, or i_L=-i_{L2}<0 during normal operation and does not require the operating modes, III, IV, VII, and VIII in Tables 1 and 2. Thus, diodes D_1 and D_2 can be removed, simplifying the dual buck three-level grid-connected inverter. With the removal of diodes D_1 and D_2, Topology I (Fig. 3) can be a dual buck three-level structure applicable under grid-connected situations. Similarly, as Fig. 4 illustrates, another grid-connected dual Buck three-level structure based on topology II can be obtained; this structure, illustrated in Fig. 5, is the new topology proposed and presented in this paper. The line cycle has four main modes of operation.

Model I: As shown in Fig. 6(a); S_1 is turned on and the output of bridge arm A is +U_d; inductor current i_{L1} increases and no current flows in the S_3, D_3 branch; C_1 is discharged, u_{C1} declines, and u_{C2} rises because u_{C2}=2U_d-u_{C1}.

Model II: As shown in Fig. 6(b); S_1 is turned off, freewheeling current i_{L1} flows through S_3, D_3 and the output of

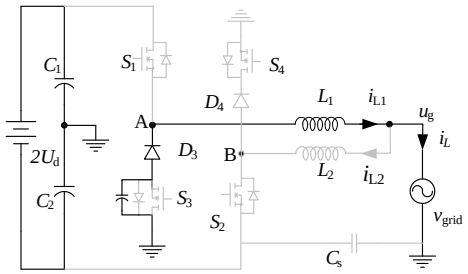

Fig. 7. Zero-crossing distortion.

bridge arm A is clamped at 0; u_{C1} and u_{C2} do not change.

Model III: As shown in Fig. 6(c); S2 is turned on, the output of bridge arm B is -Ud, and iL2 increases; no current flows in branch S4, D4; C2 is discharged, uC2 declines, and uC1 rises because uC1=2Ud-uC2.

Model IV: As shown in Fig. 6(d); S1 is turned off, iL2 flows from S4, D4; the output of bridge arm B is 0; uC1 and uC2 do not change.

B. Analysis of Zero-Crossing Distortion

As shown in the preceding analysis, the switches work at half cycle mode. In the actual circuits, the driving signals of S_1 and S_2 are not completely ideal, and dead time can be observed. For example, in the positive half cycle, when both S_1 and S_3 are turned-off, switches S_2 and S_4 are not turned-on, and the inductor current does not decrease to zero, the inductor current will flow through the parasitic capacitors of the devices (Fig. 7), causing LC resonance and leading to zero-crossing distortion. However, only two zero-crossing points can be observed and the dead time can be shortened to the largest amount possible. In addition, the zero-crossing current is minimal; thus, the zero-crossing distortion is not very serious, the influence of which can be ignored.

C. Analysis of Input Capacitors

The variety rate of $2U_d$ is significantly less than the variety rate of u_{C1} and u_{C2}, which are related to the switching frequency; thus, the equation, $i_{C1}+i_{C2}C_1/C_2=0$, can be approximated. In accordance with Kirchhoff's current law, $i_{C1}+i_L=i_{C2}$ can be obtained; thus, currents of capacitors C_1 and C_2 are

$$i_{C1}=\frac{-C_1}{C_1+C_2}i_L \tag{1}$$

$$i_{C2}=\frac{C_2}{C_1+C_2}i_L \tag{2}$$

where $i_L=\sqrt{2}I_L\sin(\omega t+\theta)$, and the voltage on C_2 can be obtained as:

$$u_{C2}=\frac{1}{C_2}\int_0^t i_{C2}d\tau+U_{C20}=\frac{\sqrt{2}I_L}{\omega(C_1+C_2)}[\cos\theta-\cos(\omega t+\theta)]+U_{C20} \tag{3}$$

D. Analysis of Leakage Current

Given the photovoltaic array output voltage, $2U_d$, the

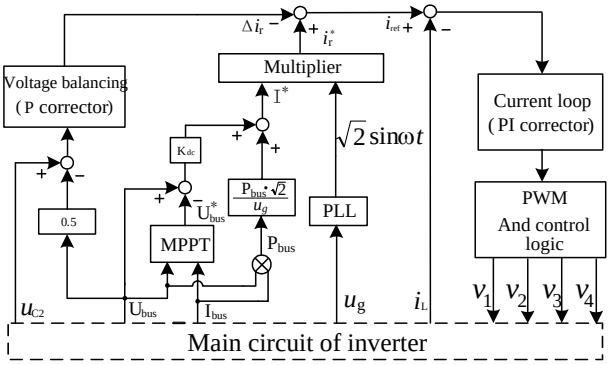

Fig. 8. Control block diagram.

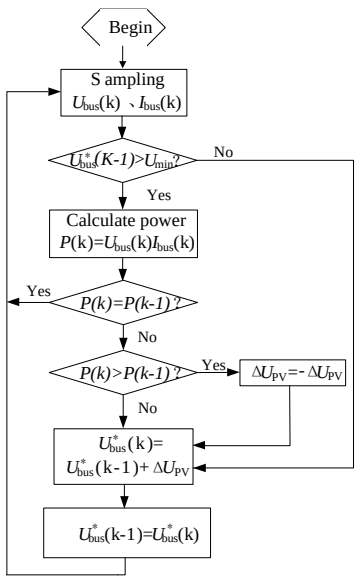

Fig. 9. Control algorithm of MPPT.

grounding parasitic capacitor C_s of the photovoltaic array exists between the negative bus and the ground. The current of grounding parasitic capacitance is also the leakage current:

$$i_{CS} = C_S \frac{\Delta u_{CS}}{\Delta t} \tag{4}$$

where u_{CS} is the voltage across C_S. As shown in Fig. 5, the voltage across C_S is also the voltage across output capacitor C_2.

$$\begin{aligned} u_{CS} = u_{C2} &= \frac{1}{C_2}\int_0^t i_{C2} d\tau + U_{C20} \\ &= \frac{\sqrt{2} I_L}{\omega(C_1 + C_2)}[\cos\theta - \cos(\omega t + \theta)] + U_{C20} \end{aligned} \tag{5}$$

Using equations (4) and (5), the leakage current can be obtained as:

$$i_{CS} = \frac{\sqrt{2} I_L C_S}{(C_1 + C_2)} \sin(\omega t + \theta) \tag{6}$$

As demonstrated, the proposed topology is similar to that of the half-bridge inverter, and the voltage of grounding parasitic capacitance is clamped by large input capacitors. As shown in equation (6), the leakage current is related to the input capacitors, the grounding parasitic capacitor, and inductor current; the capacitance of the grounding parasitic capacitor can get as high as approximately 200 nF/kW in inferior environments such as rainy and damp environments [18] capacitance that is much less than that of the input capacitor. Therefore, the leakage current is insignificant and can be ignored.

III. Control Strategy

Fig. 8 shows the inverter control block diagram, designed to simultaneously implement grid connection, MPPT, and voltage balancing functions, which is composed of three parts—the voltage balancing loop, current loop, and current reference circuit.

From equation (1), the average voltage on capacitors C_1 and C_2 can be obtained from integration and can be expressed as

$$\bar{u}_{C1} = U_{C10} - \frac{\sqrt{2} I_L}{\omega(C_1 + C_2)} \cos\theta \tag{7}$$

$$\bar{u}_{C2} = U_{C20} + \frac{\sqrt{2} I_L}{\omega(C_1 + C_2)} \cos\theta \tag{8}$$

where U_{C10} and U_{C20} are the initial voltages of capacitor C_1 and C_2, respectively. Assuming $U_{C10} = U_{C20} = U_d$, we then obtain voltage deviation as

$$\Delta\bar{u} = \bar{u}_{C2} - \bar{u}_{C1} = \frac{2\sqrt{2} I_L}{\omega(C_1 + C_2)} \cos\theta \tag{9}$$

The voltage balancing loop is the outer loop. In accordance with the mechanism for unbalancing input voltage generation [19], [20], the capacitor voltage feed forward scheme is introduced (Fig. 8). As shown in equation (9), the unbalanced voltage is related with the grid current and, to a certain extent, has a proportional relationship with the sum of the two capacitances. As indicated by the input capacitor voltage deviation, the current loop not only regulates the inductor current but also solves the voltage unbalancing problem (Fig. 8).

The number of solar panels in the string is based on ensuring that dc voltage is higher than the ac voltage peak at all times; thus, the used solar-panels consists of sixteen PV panels [21]. The perturbation and observation algorithm is adopted to implement MPPT (Fig. 9). Evidently, the input bus voltage changes within a wide range and will not be less than U_{min} (which is set as 350 V). Additionally, the power feed-forward scheme is adopted to generate the reference current. Using the input power feed-forward scheme, we improve the dynamic of the PV system. The dc voltage controller ensures a quick response of the PV system under a sudden change in the input power.

IV. Key Parameters Design

A. Filter Inductor Design

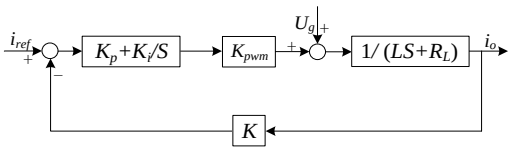

Fig. 10. Control block diagram of the proposed inverter.

From equation (9), C_1 and C_2 can be determined if the allowable voltage difference on capacitors is known. Moreover, this allowable value is also required for defining inductance in the output filter. As indicated in the analysis, the two inductors of the three-level dual buck photovoltaic grid-connected inverter work symmetrically, one in the positive half load cycle period and the other in the negative half load cycle period. The operation in the positive half load cycle period is investigated in detail. In a high-frequency switching cycle, grid voltage is nearly constant; and inductor current can be expressed as:

$$U_{\mathrm{d}} - u_{\mathrm{g}}(K) = L_1 \frac{\Delta i_{\mathrm{L1}}}{DT_{\mathrm{s}}} \tag{10}$$

where D is the high-frequency duty cycle and $u_g(K)$ is grid voltage at the switching period. Given that

$$\frac{u_{\mathrm{g}}(K)}{U_d} = D \tag{11}$$

Thus,

$$\Delta i_{\mathrm{L1}} = \frac{(U_{\mathrm{d}} - u_{\mathrm{g}}(K))u_{\mathrm{g}}(K)T_{\mathrm{s}}}{L_1 U_{\mathrm{d}}} \tag{12}$$

and the possible maximum current ripple value can be expressed as

$$\Delta i_{\mathrm{L1max}} = \frac{U_{\mathrm{d}}T_{\mathrm{s}}}{4L_1} \tag{13}$$

By considering the magnetic component's volume size, weight, losses, and other factors, current ripple can be set at 10%–20% of the rated output current and the inductance value of L_1 can be calculated. Similarly, choke inductor L_2, working at negative half load cycle period, can also be determined. In addition, the LCL filter can be applied in the proposed inverter, which will minimize its inductors.

B. Input Capacitor Design

As shown in equation (5), the fluctuation of u_{C1} and u_{C2} are equal and can be obtained as:

$$\Delta u_{\mathrm{C1}} = \Delta u_{\mathrm{C2}} = \frac{2\sqrt{2}I_L}{\omega(C_1 + C_2)} \tag{14}$$

Input capacitors are usually connected with equal capacitance, and the voltage ripple is set at less than 5% of the input voltage; thus, the values of C_1 and C_2 can be calculated.

C. Control Parameter Design

In the common grid-connected inverter, the single current loop control is adopted to track the reference current and to maintain the stability of the system; the block diagram of the current loop control for the proposed inverter is shown in Fig. 10. The feedback coefficient of the output current is K, and K_{pwm} is the equivalent proportionality constant.

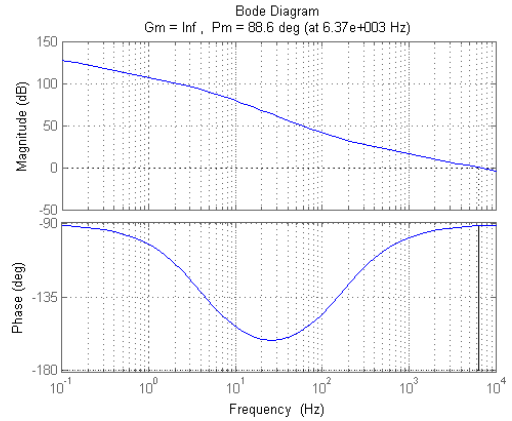

Fig. 11. Bode diagram of the proposed inverter.

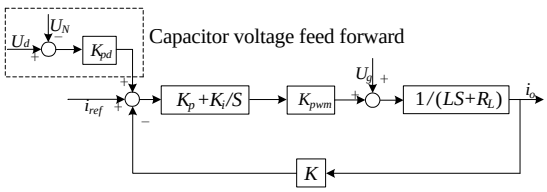

Fig. 12. The improved control block diagram of the proposed inverter.

To make the transient system work properly with minimal overshoot and ringing, we designed the parameters of the current loop PI controller as follows: K_p=1, K_i=10000, and the bode diagram of the proposed inverter is as shown in Fig. 11. As indicated in Fig. 10, the system is stable.

However, in accordance with the analysis (Part III), the capacitance voltage feed forward scheme is adopted to solve the voltage unbalancing problem (Fig. 12). Fig. 13(a) indicates a voltage unbalancing problem and shows that, without the capacitor voltage feed forward control, the inductor current will be finally malformed. Thus, the capacitor voltage feed forward scheme is added and K_{pd} is set as 0.1, contributing to the normal operation of the system, as indicated in the simulation results shown in Fig. 13(b).

V. Simulation and Experimental Verification

To verify the proposed topology and control scheme, we herein present the simulation and experimental results. The parameters of the prototype used in the simulations are as follows: input capacitors $C_1 = C_2 = 1100$ μF; output filtering inductor $L_1 = L_2 = 750$ μH; output voltage u_o = 220 VAC/50 Hz; DC input voltage $U_d = 720$ VDC, and thus $u_{C1} = u_{C2} =$ 360 VDC at steady-state; output power $P_o = 1$ kW; switching frequency f_s =100 kHz. MOSFET switches used are IPW65R037C6 models, and diodes used are DSEI30-06A models.

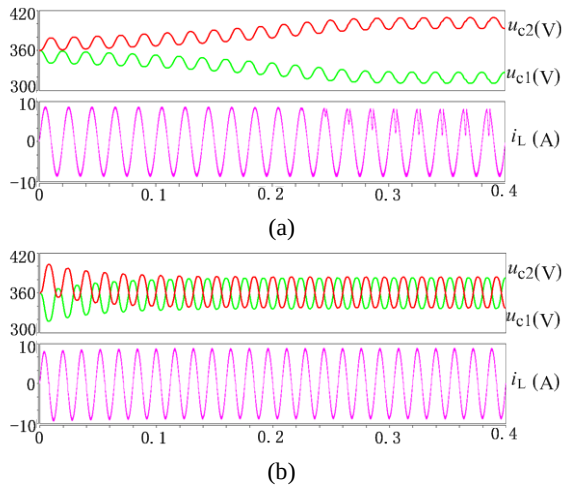

Fig. 13. Test results. (a) Without capacitor voltage feed forward control. (b) With capacitor voltage feed forward control.

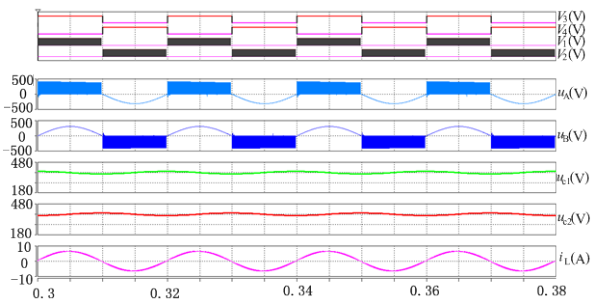

Fig. 14. Simulation waveforms.

Simulation results are illustrated in Fig. 14, where u_g is the grid voltage; inductor current $i_L = i_{L1} + i_{L2}$; u_{C1} and u_{C2} are the input voltages on capacitors C_1 and C_2, respectively; u_A and u_B are the voltages at the bridge arm middle points A and B, respectively; and v_1–v_4 are the driving signals for switches S_1–S_4, respectively.

When i_L=i_{L1}>0, Buck circuit 1 operates in the positive half load cycle period, and u_A is the modulated SPWM voltage waveform, S_2 and S_4 are in the off state, Buck circuit 2 is separated from the grid, i_{L2}=0, and u_B=u_g. When i_L=i_{L2}<0, Buck circuit 2 operates in the negative half load cycle period, u_B is the modulated SPWM modulated voltage waveform, S_1 and S_3 are in off state, Buck circuit 1 is separated from the grid, i_{L1}=0, and u_A=u_g. Therefore, the inverter completes the DC/AC conversion and the input voltage balancing control in the closed-loop. The voltages across the input capacitors C_1 and C_2 are stable.

Under the same output conditions, the proposed inverter is compared with other inverters such as 3L-NPC and DBHBI [22] (Table III).

As shown in Table III, the proposed inverter has more inductors than the 3L-NPC; however, the proposed inverter has no shoot-through problems. Shoot-through problems have significant negative impact on reliability, wherein dead time needs to be set, which will cause distortion of the output. In addition, during dead time, the inductor current flows through the body diode, causing increased loss. The aforementioned analysis indicates that the proposed inverter is in a good position in terms of reliability and efficiency. Moreover, although the proposed inverter has more switches than the DBHBI, the two inverters have an equal number of high-frequency switches; and the voltage stress of the switches and diodes in the proposed inverter is half of that in the DBHBI.

TABLE III
COMPARISON OF THE PROPOSED INVERTER WITH OTHER INVERTERS

Items		3L-NPC	DBHBI	Proposed Inverter
High-frequency Switches	Number	2	2	2
	U_{DS}(max)	360 V	720 V	360 V
	I_D(max)	6.42 A	6.42 A	6.42 A
Low-frequency Switches	Number	2	0	2
	U_{DS}(max)	360 V	N/A	360 V
	I_D(max)	A	N/A	6.42 A
Independent freewheeling diodes	Number	2	2	2
	U_{KA}(max)	360 V	720 V	360 V
	I_A(max)	6.42 A	6.42 A	6.42 A
Filter inductors	Number	1	2	2
	L(μH)	750	750	750
Input capacitors	Number	2	2	2
	C(μF)	1100	1100	1100
Shoot-through problem?		Yes	No	No
Current through body diodes?		Yes	No	No

TABLE IV
COMPARISON WITH OTHER NON-ISOLATED GRID-CONNECTED INVERTERS

Items		H5	HERIC	H6	Proposed inverter
Number of High-frequency Switches		3	4	4	2
Number of Low-frequency Switches		2	2	2	2
Number of Independent Freewheeling Diodes		0	2	2	2
Filter inductors	number	2	2	2	2
	L(mH)	3	3	3	0.75
Switching frequency (kHz)		20	20	20	100
Rate power (W)		1000	1000	1000	1000
Efficiency		96.7%	96.8%	96.9%	96.7%

Experimental results are shown in Fig. 15. Fig. 15(a) shows the voltage waveforms u_B at the bridge arm middle point, grid voltage u_g, inductor current i_L, and the driving signal v_1 of S_1. Fig. 15(b) shows inductor current i_{L2}. Fig. 15(c) shows inductor current i_L, voltage u_{C1} of C_1, and voltage u_{C2} of C_2. Fig. 15(e) demonstrates reference current i_{ref}, driving signal v_1 of S_1,

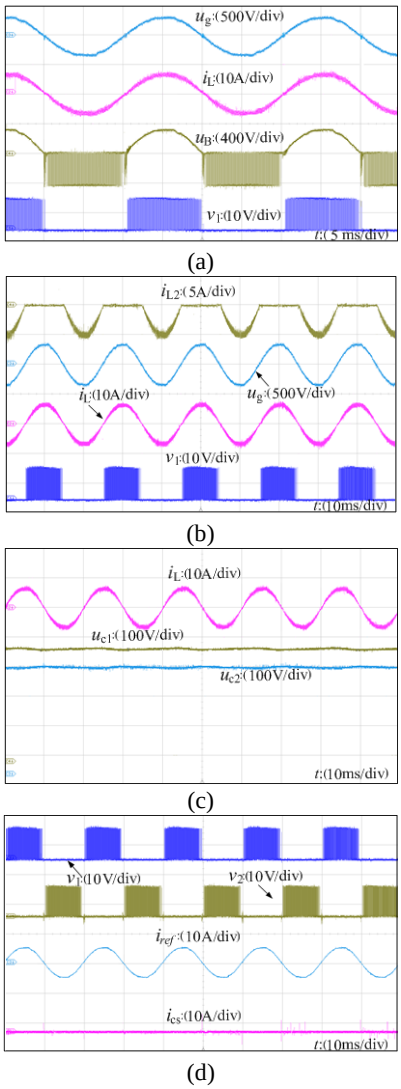

Fig. 15. Test results.

driving signal v_2 of S_2, and leakage current i_{CS}. The aforementioned values match the theoretical analysis and the simulation results well. As indicated in Fig. 15(c), the average voltages of C_1 and C_2 are the same, proving that the capacitor voltage feed forward scheme works. In addition, the voltage ripple is a sinusoidal wave and is consistent with that theorized in the analysis. Fig. 15(d) demonstrates that the voltage of input capacitance is stable, which is due to the effective voltage balancing scheme, and does not vary in the high switching frequency. Furthermore, no leakage current is generated.

The tested efficiency curve is shown in Fig. 16. As clearly shown, high conversion efficiency is achieved. For non-isolated grid-connected inverters, leakage currents cannot be ignored and reduce the reliability and security of the inverters. Many modified topologies based on the bridge-type inverter are proposed to eliminate leakage current by adding devices, which will increase losses. The efficiency results, as compared with other non-isolated grid-connected inverters (H5, HERIC, and H6 [23]), are summarized in

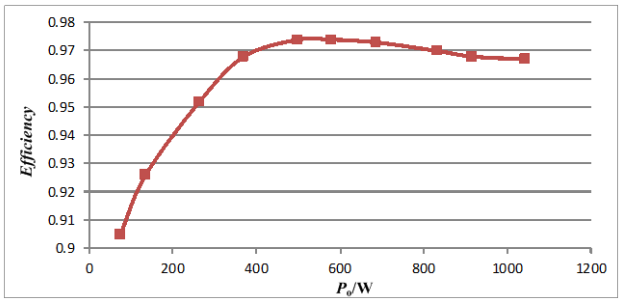

Fig. 16. Efficiency curve.

Table IV. The proposed inverter has only two high-frequency switches, meaning that it has low switching loss. The inductor of the proposed inverter is much less than that of the H5, HERIC, and H6, because of the high switching frequency; however, the efficiencies of all the inverters are almost equal. We can reasonably estimate that when the switching frequency is reduced and the low on-resistance switches are used, the switching loss and conduction loss will be decreased and efficiency will be further increased.

VI. Conclusion

A novel three-level Dual Buck photovoltaic grid-connected inverter is proposed. The output voltage at the bridge arm of the inverter has a unipolar modulated waveform; the voltage on the grounding parasitic capacitor is clamped by large input voltage balancing capacitors and varies slightly in line frequency rather than in high switching frequency. Thus, leakage current is effectively eliminated. Unlike in traditional topologies, current in the proposed typology passes through fewer elements and does not go through the body diodes of MOSFET switches, resulting in higher efficiency. Furthermore, a multi-loop control method that includes voltage-balancing control is proposed and analyzed. Both demonstrated simulation and experimental results are demonstrated to verify the proposed structure and the control method.

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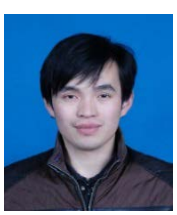

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